

Features

- **Wide Input Voltage Range from 2.7V to 21V**
- **High Current-Limit up to 3.5A**
- **0.5V Reference Voltage with $\pm 3\%$ System Accuracy**
- **50mW Integrated N-FET**
- **Fixed 1.2MHz Switching Frequency**
- **High Efficiency up to 95%**
- **Open-LED Protection**
- **Under Voltage Lockout Protection**
- **ALS Control Input Pin**
- **Over Temperature Protection**
- **Low Shutdown Current: $< 1\mu A$**
- **3mm x 3mm DFN-10 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

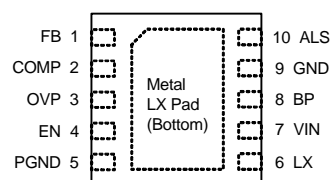
Applications

- **Display Backlighting**
 - Automotive
 - LCD Monitors
 - Notebook Displays
- **Portable Displays**

General Description

The APW7128 is the high power and high efficiency boost converter with an integrated 30V FET ideal for LCD panel backlighting applications. 30V output voltage allows for 8 high-power LEDs in series, and 3.5A inductor current limit allows for more LED strings connected in parallel. The low 0.5V feedback voltage offers higher efficiency in WLED driver applications. The wide input range from 2.7V to 21V made APW7128 a perfect solution for various applications such as LCD monitor and portable devices. The OVP pin monitors the output voltage to protect IC during open load and FB pin short circuit operations. The APW7128 provides the ALS pin to simplify the interface to an ambient light sensor for automatic dimming. The APW7128 is available in the thermally enhanced DFN-10 lead 3mm x 3mm package.

Pin Configuration



APW7128

DFN3x3-10 Top View

Ordering and Marking Information

<p>APW7128 □□□-□□□</p> <p>Assembly Material</p> <p>Handling Code</p> <p>Temperature Range</p> <p>Package Code</p>	<p>Package Code</p> <p>QA: DFN3x3-10</p> <p>Operating Ambient Temperature Range</p> <p>I : -40 to 85°C</p> <p>Handling Code</p> <p>TR : Tape & Reel</p> <p>Assembly Material</p> <p>L : Lead Free Device G : Halogen and Lead Free Device</p>
<p>APW7128 QA: APW 7128 XXXXX</p>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN pin to GND	-0.3 to 30	V
V_{LX}	LX pin to PGND	-0.3 to 30	V
V_{OVP}	OVP pin to GND	-0.3 to 30	V
V_{BP}	BP pin to GND	-0.3 to 6	V
V_{EN}	EN pin to GND	-0.3 to 30	V
V_{ALS}	ALS pin to GND	-0.3 to 6	V
	PGND to GND	-0.3 to 0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_L	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Stresses beyond the absolute maximum rating may damage the device and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Package	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance in Free Air	DFN3x3-10	80	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage, (VIN=BP)	2.7 to 5.5	V
	VIN Supply Voltage, (BP is open)	3.7 to 21V	V
V_{OUT}	Output Voltage	up to 30	V
T_J	Operating Ambient Temperature	-40 to 85	°C
T_A	Operating Junction Temperature	-40 to 125	°C

Electrical Characteristics

$V_{IN}=6V$, $T_A = -40$ to 85°C , unless otherwise specified. Typical values refer to $T_A = 25^\circ\text{C}$.

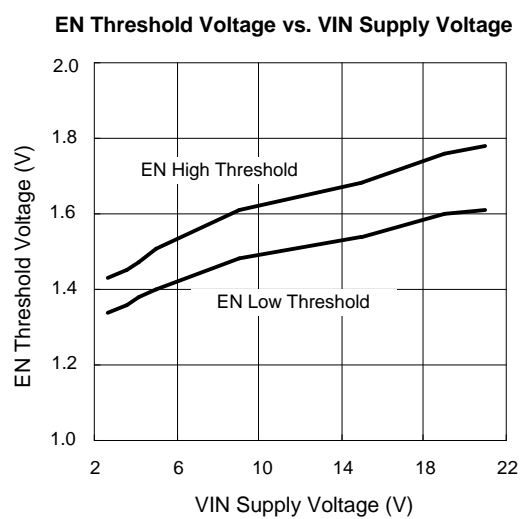
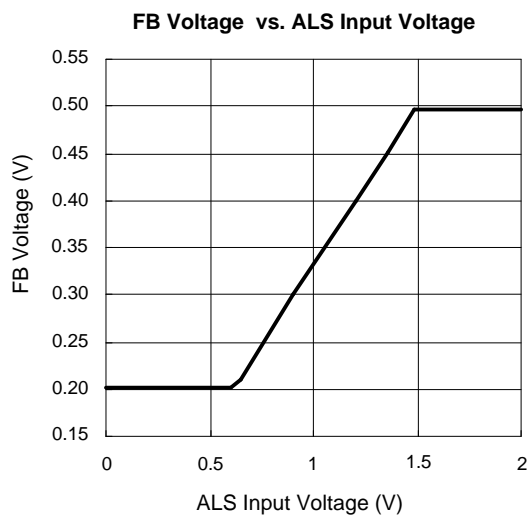
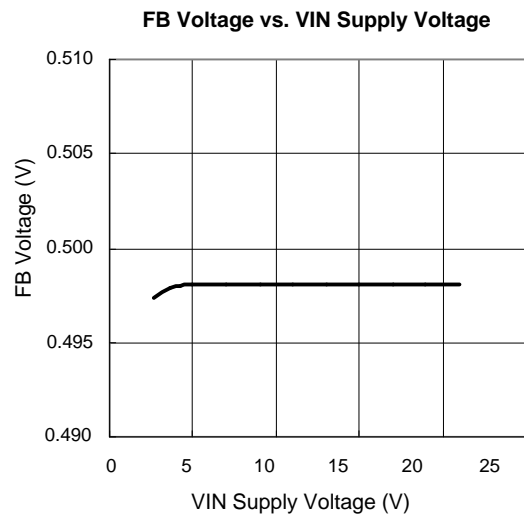
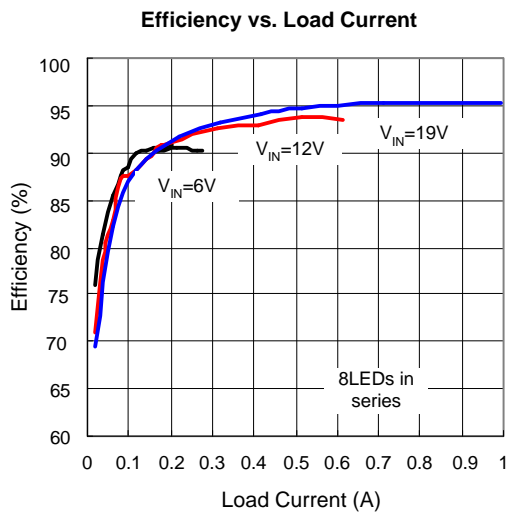
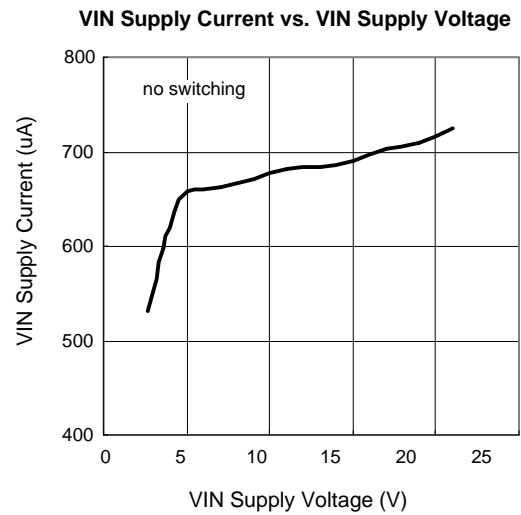
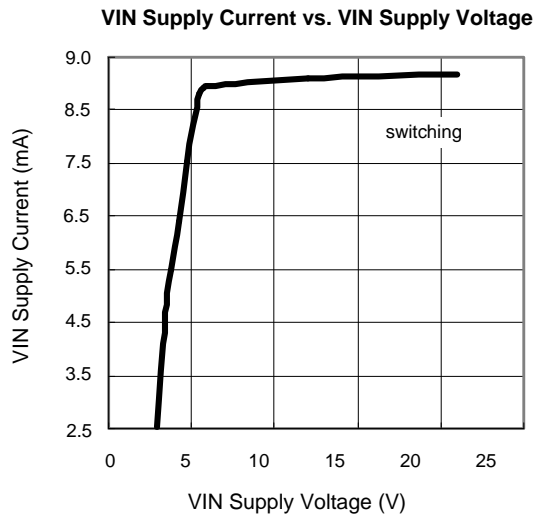
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT SUPPLY CURRENT AND UVLO						
	BP Under Voltage Lockout Threshold	V _{IN} rising	2.4	2.5	2.6	V
	UVLO Hysteresis		-	100	-	mV
I _{VIN}	VIN Supply Current	EN=5V, switching	-	9	15	mA
		EN=0V	-	-	1	uA
ERROR AMPLIFIER						
gm	Error Amplifier Transconductance		-	350	-	uA/V
I _{COMP}	COMP Output Current	sourcing and sinking, V _{COMP} =1.5V	-	50	-	uA
V _{FB}	FB Voltage		485	500	515	mV

Electrical Characteristics (Cont.)

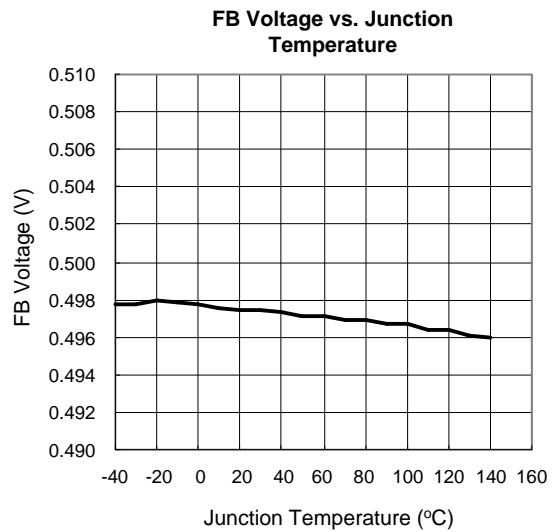
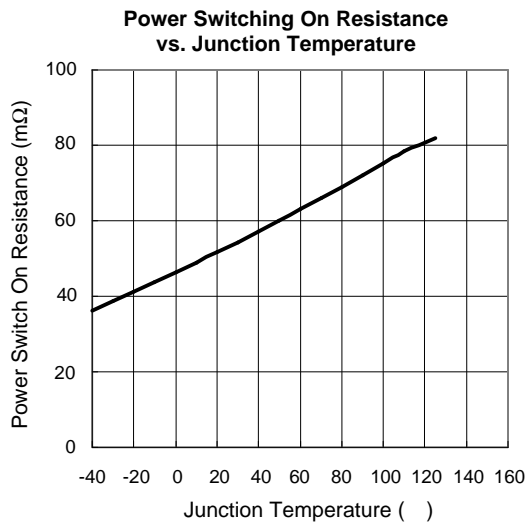
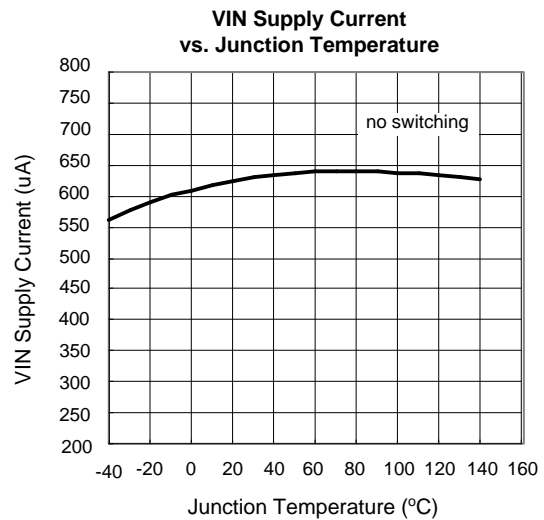
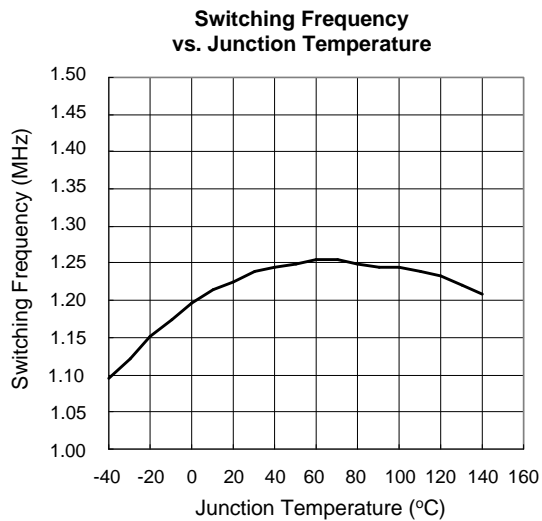
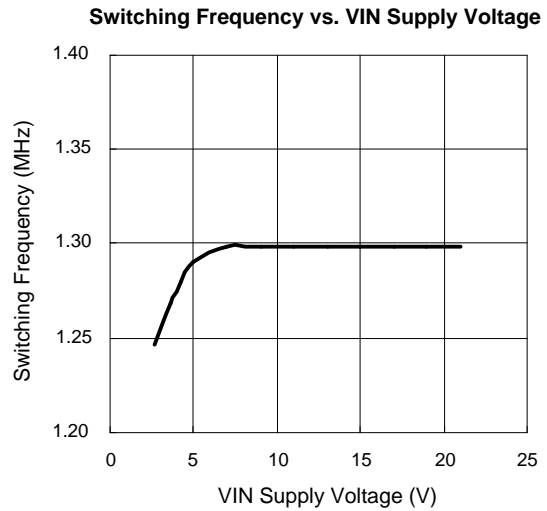
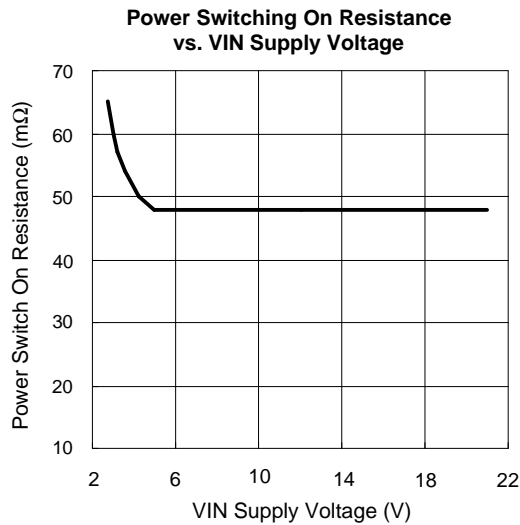
$V_{IN}=6V$, $T_A = -40$ to $85^{\circ}C$, unless otherwise specified. Typical values refer to $T_A = 25^{\circ}C$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Minimum FB Voltage	$V_{ALS}=0.3V$	188	200	212	mV
I_{FB}	FB Input Bias Current		-	-	1	μA
	FB Line Regulation	$V_{IN}=2.7V$ to $21V$	-	0.02	0.04	%/V
INTERNAL POWER SWITCH						
	Power Switch Current-Limit		2.5	3.5	4.5	A
$R_{DS(ON)}$	Power Switch On Resistance		-	50	100	m Ω
	LX Leakage Current	$V_{LX}=30V$	-	-	1	μA
F_{SW}	Switching Frequency		0.9	1.2	1.5	MHz
D_{MAX}	LX Maximum Duty Cycle		92	95	98	%
ALS						
	ALS Ratio	$V_{ALS}=1V$, V_{ALS}/V_{FB}	2.9	3	3.1	V/V
	ALS Pin Leakage	$V_{ALS}=5V$	-	-	1	μA
OUTPUT OVERVOLTAGE PROTECTION						
	Over Voltage Threshold		30	32	34	V
	OVP Hysteresis		2	3	4	V
	OVP Leakage Current		-	-	30	μA
CONTROL LOGIC PIN						
	EN High-Level Input Voltage		2.4	-	-	V
	EN Low-Level Input Voltage		-	-	0.4	V
	EN Leakage Current	$V_{EN}=21V$	-	-	1	μA
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		-	150	-	$^{\circ}C$
	Thermal Shutdown Hysteresis		-	50	-	$^{\circ}C$

Typical Operating Characteristics



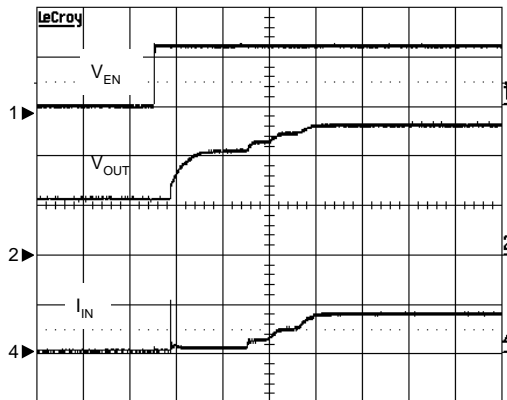
Typical Operating Characteristics (Cont.)



Operating Waveforms

Refer to the typical application circuit. The test condition is $V_{IN}=5V$, $T_A=25^{\circ}C$ unless otherwise specified.

Start-up



$V_{IN}=12V$, $L=10\mu H$, $C_{COMP}=0.22\mu F$

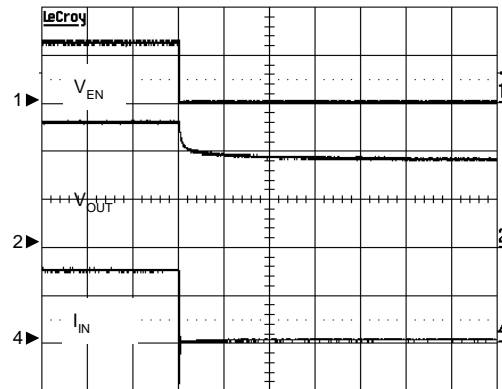
CH1: V_{EN} , 10V/div, DC

CH2: V_{OUT} , 10V/div, DC

CH4: I_{IN} , 500mA/div, DC

TIME: 1ms/div

Shutdown



$V_{IN}=12V$, $L=10\mu H$, $C_{COMP}=0.22\mu F$

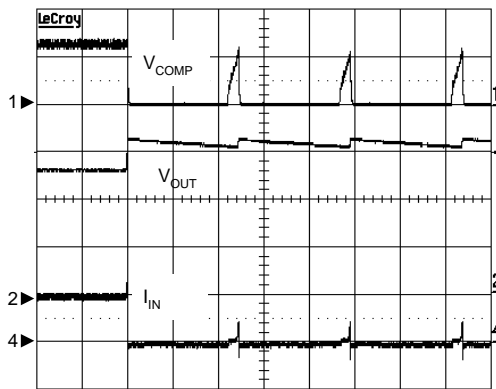
CH1: V_{EN} , 10V/div, DC

CH2: V_{OUT} , 10V/div, DC

CH4: I_{IN} , 500mA/div, DC

TIME: 10ms/div

Overvoltage Protection



Output is open

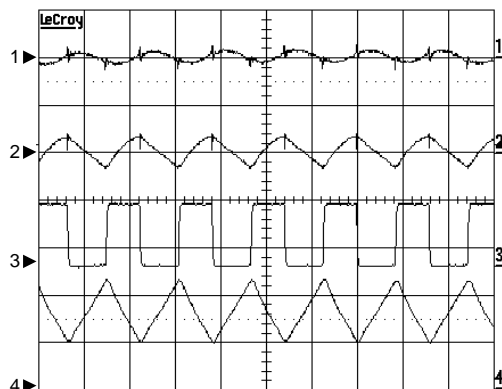
CH1: V_{COMP} , 0.5V/div, DC

CH2: V_{OUT} , 10V/div, DC

CH4: I_{IN} , 100mA/div, DC

TIME: 10ms/div

Switching Waveforms



$V_{IN}=12V$, $L=10\mu F$, $I_{OUT}=160mA$

CH1: V_{IN} , 50mV/div, AC

CH2: V_{OUT} , 200mV/div, AC

CH3: V_{LX} , 20V/div, DC

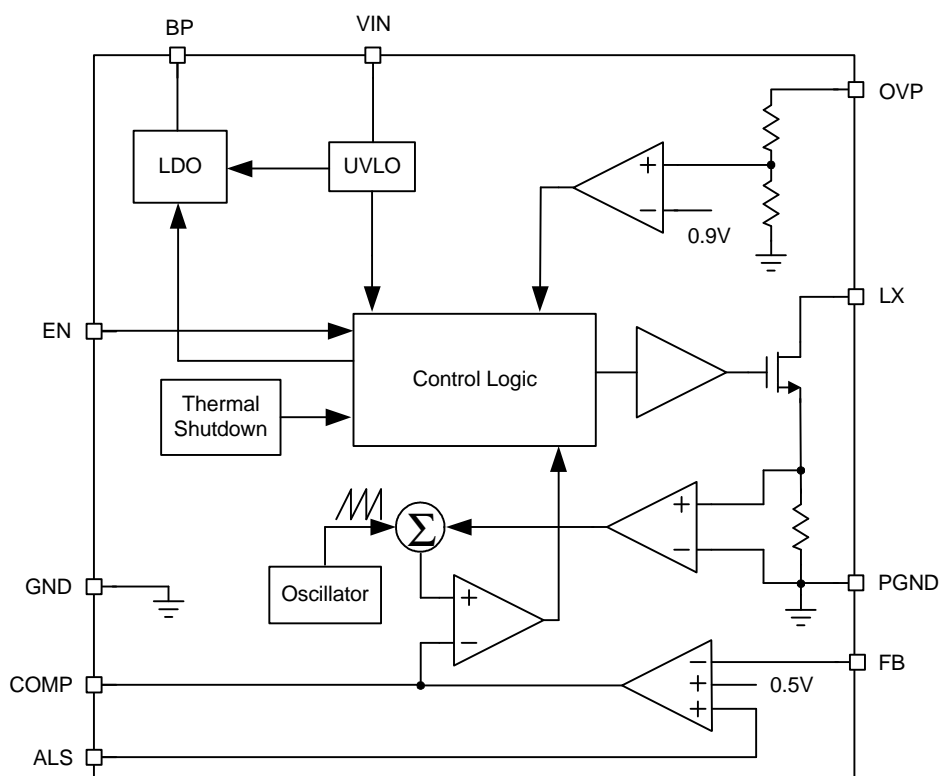
CH4: I_L , 200mA/div, DC

TIME: 0.5us/div

Pin Description

PIN		FUNCTION
NO.	NAME	
1	FB	Regulator Feedback Pin. Connect a current sense resistor to GND to set the LED current.
2	COMP	Error Amplifier Output. Connect a 0.22 μ F capacitor for compensation and soft-start. When EN is pulled low, an internal switch will discharge the COMP voltage to 0V.
3	OVP	Output Over Voltage Monitor Pin. Tie to VOUT for OVP function.
4	EN	Enable Input Pin. Pull EN above 2.4V to enable the device; pull EN below 0.4V to disable the device. The EN pin cannot be left floating.
5	PGND	Power Ground. Source of the internal N-channel power MOSFET.
6	LX	Internal Power MOSFET Drain.
7	VIN	Supply Voltage Input.
8	BP	Output of The Internal 5V Regulator. Connect a 1 μ F bypass capacitor to GND. Do not apply an external load to BP.
9	GND	Signal Ground.
10	ALS	Ambient Light Sensor Input. Allow the light sensor to control the FB voltage for LED dimming. If the ALS function is not used, tie the ALS pin to BP pin.

Block Diagram



Typical Application Circuit

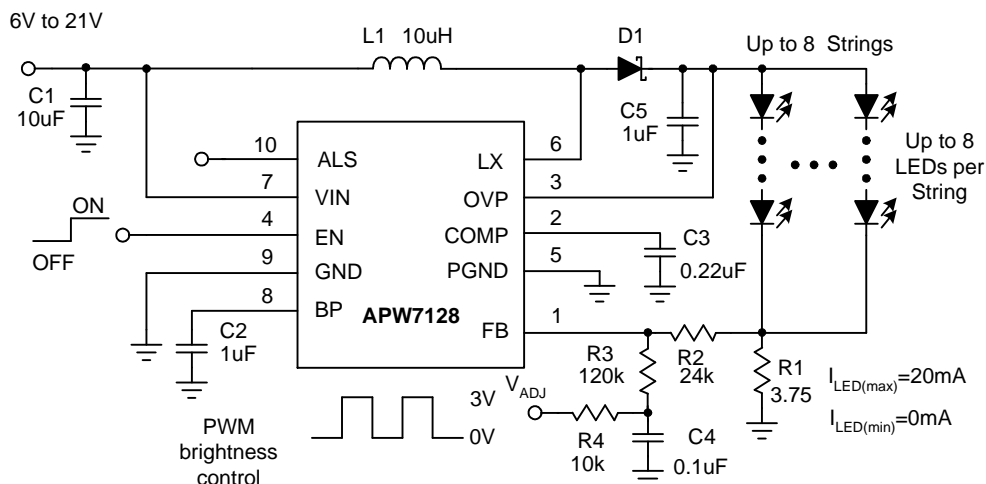


Figure1. Analog Dimming with PWM Voltage

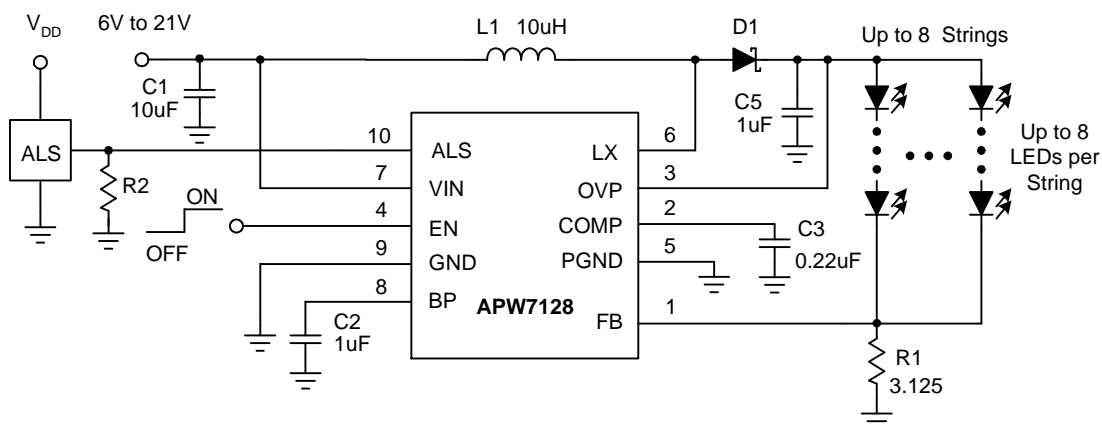


Figure2. Analog Dimming with External ALS Voltage

Designation	Supplier	Part Number	Specification	Website
L1	GOTREND	GTSD53	10uH, 1.33A	www.gotrend.com.tw
C1	Murata	GRM31CR61E106K	X5R, 25V, 10uF	www.murata.com
C2	Murata	GRM155R61A105K	X5R, 10V, 1uF	www.murata.com
C3	Murata	GRM155R60J224KE01	X5R, 6.3V, 0.22uF	www.murata.com
C5	Murata	GRM21BR71H105KA12	X7R, 50V, 1uF	www.murata.com
D1	Zowie	MSCD104	1.0A, 40V	www.zowie.com.tw

Function Description

Output Overvoltage Protection

If the FB pin is shorted to ground or an LED fails open circuit, output voltage in BOOST mode can increase to potentially damaging voltages. An optional overvoltage protection circuit can be enabled by connection of the OVP pin to the output voltage. The device will stop switching if the output voltage exceeds OVP high threshold and re-start when the output voltage falls below OVP low threshold. During sustained OVP fault conditions, V_{OUT} will saw-tooth between the upper and lower threshold voltages at a frequency determined by the magnitude of current available to discharge the output capacitor. Note that the OVP pin must be connected to output voltage for OVP function.

Ambient Light Sensor Interface

The APW7128 provides the ALS pin to simplify the interface to an ambient light sensor. The ambient light sensor detects the ambient light and yields a current which is related to the illuminance. Connect a load resistor from the current output of ambient light sensor to ground to provide an output voltage to ALS pin. The ALS voltage will be divided by an internal divider circuit, and the divided ALS voltage will replace the internal reference voltage. The LED current can be calculated by the following equation:

$$I_{LED} = \frac{1}{3} \times \frac{V_{ALS}}{R2}$$

Note that the maximum FB voltage is set to 0.5V, and minimum FB voltage is set to 0.2V. If the divided ALS voltage is over 0.5V or less 0.2V, the LED current is limited at:

$$I_{LED(MAX)} = \frac{0.5V}{R2} \quad I_{LED(MIN)} = \frac{0.2V}{R2}$$

where R2 is the resistor from FB to GND.

Enable/Disable

Pull the EN above 2V to enable the device and pull EN pin below 0.4V to disable the device. In shutdown mode, the internal control circuits are turned off, the quiescent current is below 1uA.

Thermal Shutdown

When the junction temperature exceeds 150°C, the

internal thermal sensor circuit will disable the device and allow the device to cool down. When the device's junction temperature cools by 50°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed $T_J = +125^\circ\text{C}$.

Internal 5V LDO

The APW7128 provides an internal 5V LDO for the control circuitry, and the output of the internal LDO is BP pin. In normal operation, connect a 1μF or greater capacitor to GND is recommended. The internal LDO cannot supply any more current than is required to operate the APW7128. Therefore, do not apply any external load to BP pin. In applications, where the V_{IN} is less than 5.5V, BP should be tied to VIN through a 10Ω resistor.

Application Information

Connecting more LED strings

The APW7128 can drive 8 LED strings in parallel and up to 8 LEDs per string ($V_F < 3.5V$). Each string must have the same number of LEDs. In the applications that have the same total number of LEDs, more strings and less LEDs in series are more efficiency than less strings and more LEDs in series.

Brightness Control

The method for dimming the LEDs is to apply a PWM voltage through an RC filter into the FB pin.

The RC filter is used to convert the PWM voltage into an analog voltage. The values of the R and C depend upon the frequency of the PWM voltage and the amount of allowable ripple voltage on FB pin. The LED current is proportional to the PWM duty cycle. 0 % duty delivers maximum LED current and 100% duty delivers minimum LED current. The values of R1 and R2 are calculated by the following equations:

$$R2 = \frac{V_{FB} \times (I_{LED(max)} \times R3 + V_{ADJ(low)} - I_{LED(min)} \times R3 - V_{ADJ(high)})}{V_{ADJ(high)} \times I_{LED(max)} + V_{FB} \times I_{LED(min)} - V_{ADJ(low)} \times I_{LED(min)} - V_{FB} \times I_{LED(max)}}$$

$$R1 = \frac{V_{FB} \times (1 + \frac{R2}{R3}) - \frac{R2}{R3} \times V_{ADJ(low)}}{I_{LED(max)}}$$

where:

$I_{LED(max)}$ is the maximum LED current

$I_{LED(min)}$ is the minimum LED current

$V_{ADJ(high)}$ is the maximum PWM voltage level

$V_{ADJ(min)}$ is the minimum PWM voltage level

V_{FB} is the FB pin Voltage

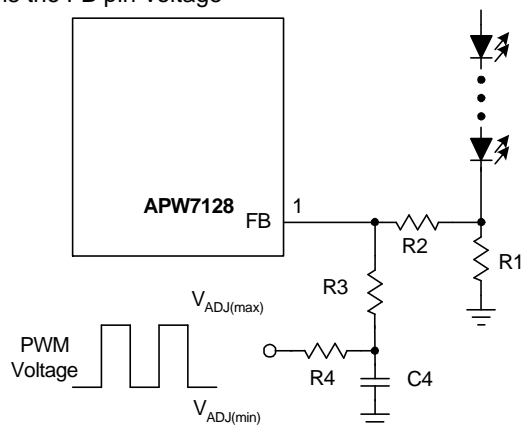


Figure 3. Dimming with the PWM Voltage

Inductor Selection

A larger value of inductor will reduce the peak inductor current, resulting in smaller input ripple current, higher efficiency and reducing stress on the internal MOSFET. However, the larger value of inductor has a large dimension, lower saturation current, and higher series resistance.

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30% to 50% of the maximum input current. Calculate the required inductance value by the equation:

$$L = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\Delta I_L \times F_{SW} \times V_{OUT}}$$

$$\Delta I_L = (30\% - 50\%) \times I_{IN}$$

$$I_{IN} = \frac{V_{OUT} \times I_{LOAD}}{V_{IN} \times \eta}$$

It is necessary to choose an inductor that ensures the inductor saturation current rating to exceed the peak inductor current for the application.

To make sure that the peak inductor current is below the current-limit 2.5A. Calculating the peak inductor current by the following equation:

$$I_{PEAK} = I_{IN} + 0.5 \times \Delta I_L$$

$$I_{PEAK} = \frac{V_{OUT} \times I_{LOAD}}{V_{IN} \times \eta} + \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{2 \times L \times F_{SW} \times V_{OUT}}$$

where

η is the efficiency

Schottky Diode Selection

A fast recovery time and low forward voltage Schottky diode is necessary for optimum efficiency. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse voltage must exceed output voltage.

Application Information (Cont.)

Capacitor Selection

An input capacitor is required to supply the ripple current to the inductor and stabilize the input voltage. Larger input capacitor values and lower ESR provide smaller input voltage ripple and noise. The typical value for input capacitor is 2.2 μ F to 10 μ F.

The output capacitor with typical value 1 μ F to 10 μ F is required to maintain the output voltage. The COMP capacitor with typical value 0.22 μ F to 1 μ F stabilizes the converter and controls the soft-start.

To ensure the voltage rating of input and output capacitors is greater than the maximum input and output voltage.

It is recommended using the ceramic capacitors with X5R, X7R, or better dielectrics for stable operation over the entire operating temperature range.

Layout Consideration

The correct PCB layout is important for all switching converters. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Figure 4 illustrates the layout guidelines; the bold lines indicate these traces that must be short and wide. The capacitors, the diode, and the inductor should be as close to the IC as possible. Keep traces short, direct, and wide. Keep the LX node away from FB and COMP pins. The trace from diode to the LEDs may be longer. The ground return of input capacitor and output capacitor should be tied close to PGND. Use the different ground planes for signal ground and power ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC. The resistor from FB to GND should be close to the FB pin as possible. The metal plate of the bottom must be soldered to the PCB and connected to LX node and the LX plane on the backside through several thermal vias to improve heat dissipation.

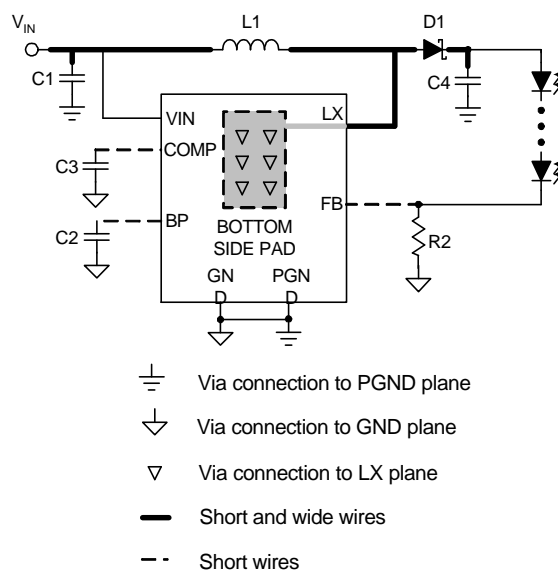
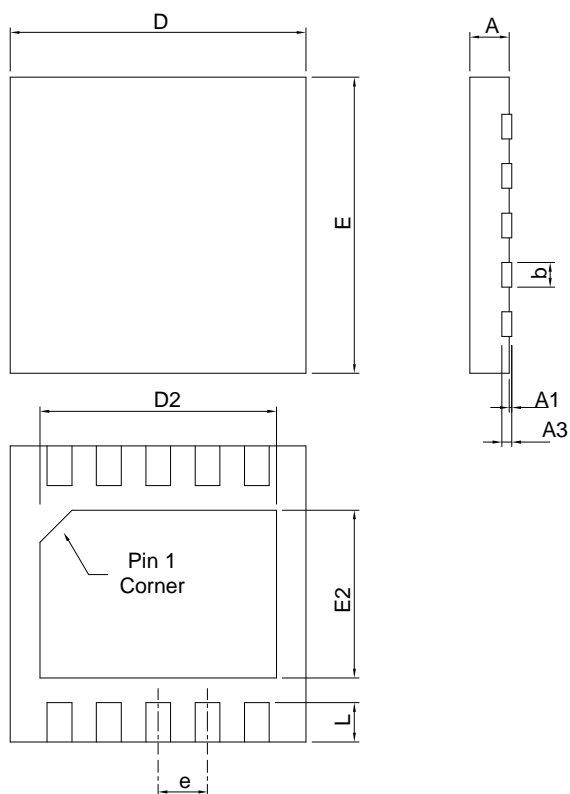


Figure 4. Layout Guidelines

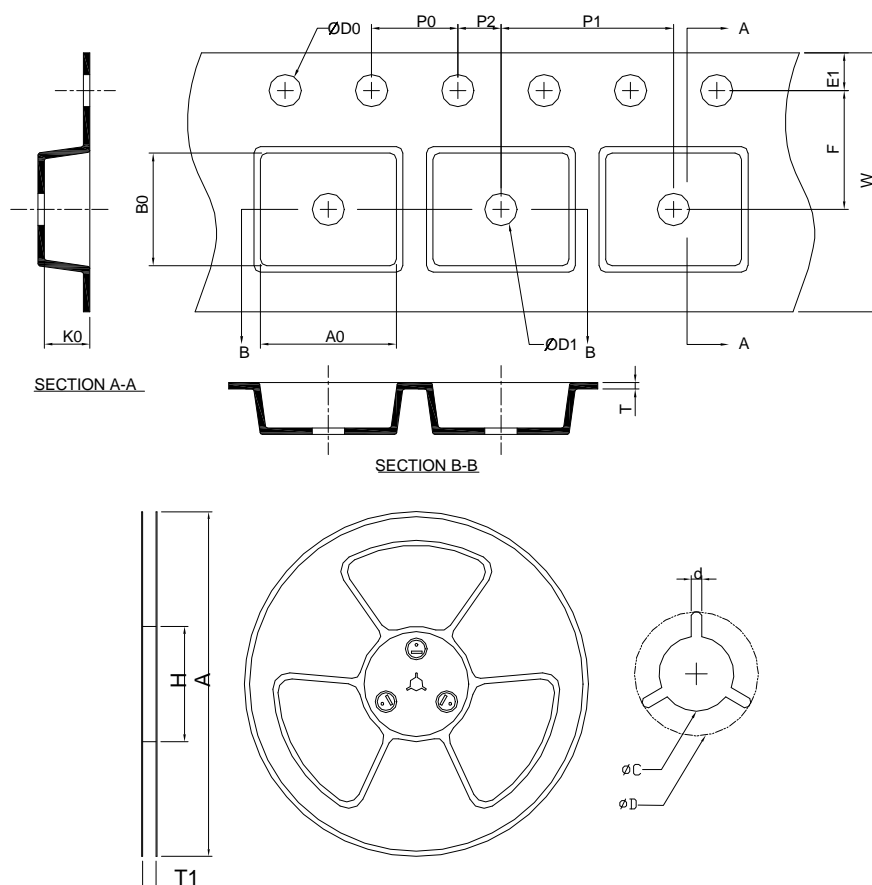
Package Information

DFN3x3-10



DIMENSIONS	DFN3*3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.00 BSC		0.118 BSC	
D2	2.20	2.70	0.087	0.106
E	3.00 BSC		0.118 BSC	
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020

Carrier Tape & Reel Dimensions



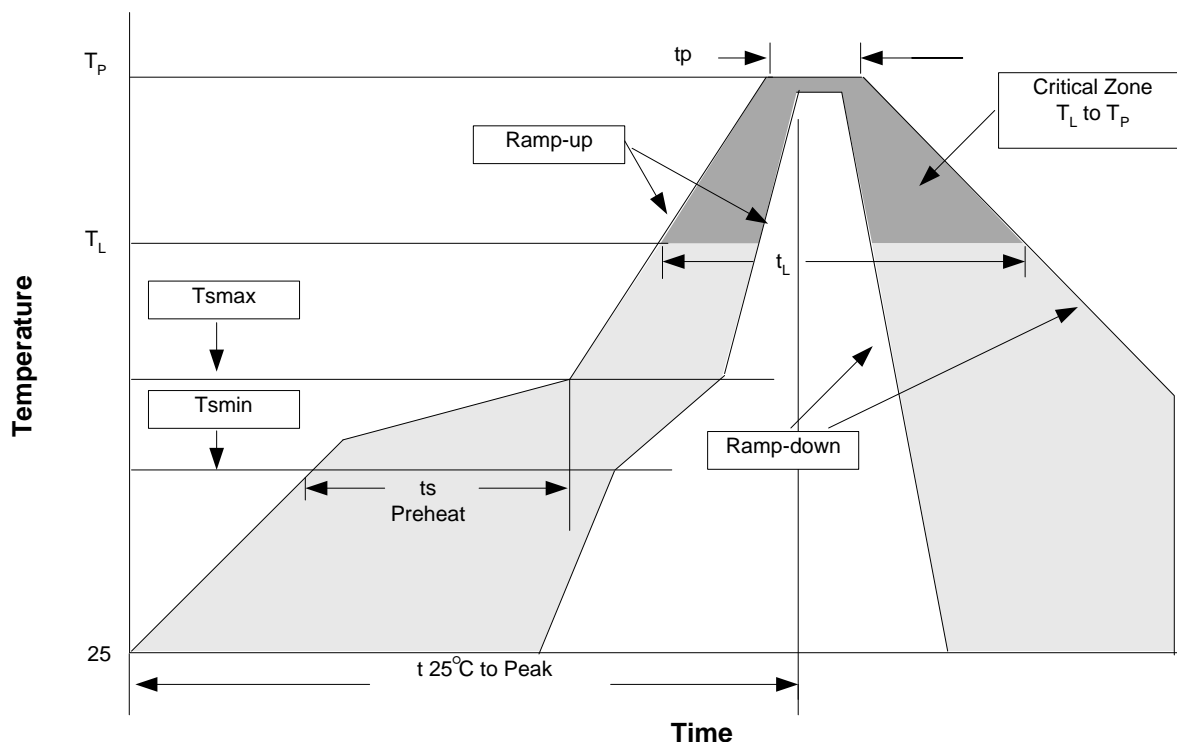
Application	A	H	T1	C	d	D	W	E1	F
DFN3x3-10	178.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.35 ±0.20	3.35 ±0.20	1.30 ±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
DFN3X3-10	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat <ul style="list-style-type: none"> - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (min to max) (t_s) 	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: <ul style="list-style-type: none"> - Temperature (T_L) - Time (t_L) 	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (T_P)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 _{tr} > 100mA

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