

## CMOS 8-Channel Data Selector

High-Voltage Types (20-Volt Rating)

■ CD4512B is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

The CD4512B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ = Full Package Temperature Range)	3	18	V

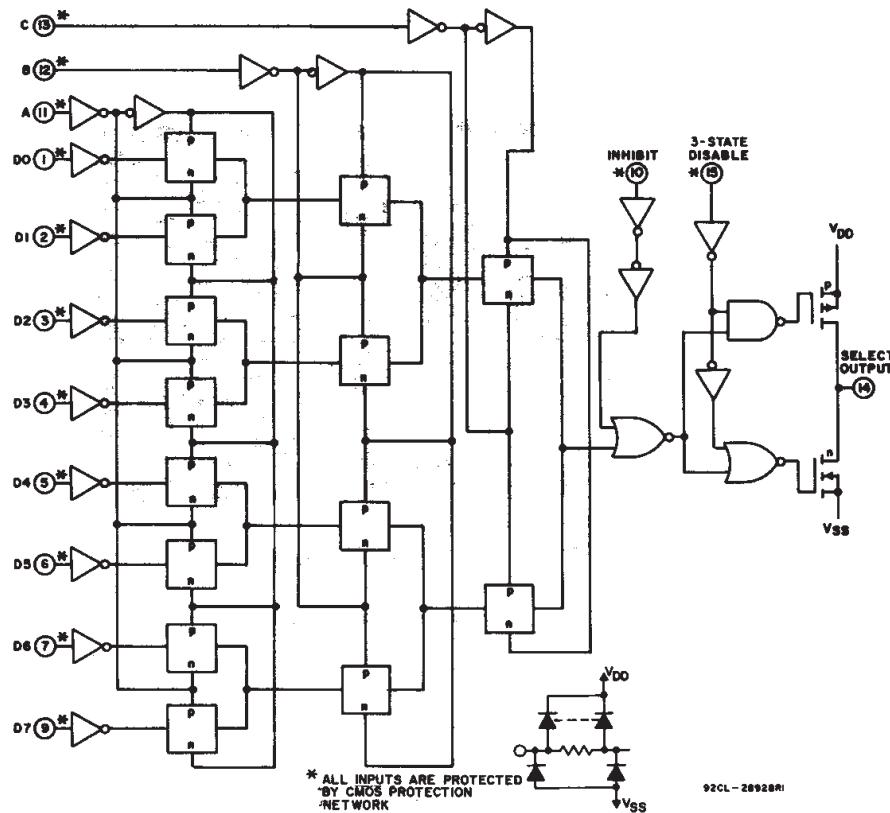


Fig. 1 – Logic diagram.

## CD4512B Types

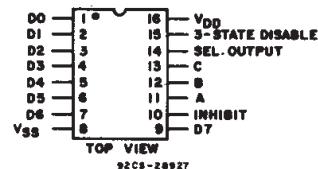
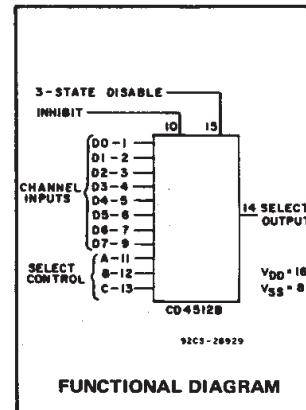
### Features:

- 3-state output
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of  $1 \mu A$  at 18 V over full package-temperature range; 100 nA at 18 V and  $25^\circ C$
- Noise margin (over full package-temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Digital multiplexing
- Number-sequence generation
- Signal gating



TERMINAL ASSIGNMENT

SEL. CONT.	INH	TRUTH TABLE	
		3-STATE DISABLE	SEL OUTPUT
0 0 0	0	0	D0
1 0 0	0	0	D1
0 1 0	0	0	D2
1 1 0	0	0	D3
0 0 1	0	0	D4
1 0 1	0	0	D5
0 1 1	0	0	D6
1 1 1	0	0	D7
X X X	1	0	0
X X X	X	1	High Z

1 = High Level 0 = Low Level

X = Don't Care

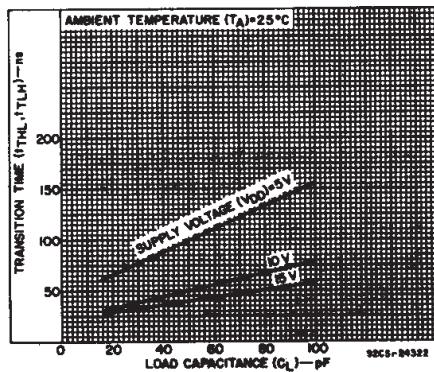


Fig. 2 – Typical transition time as a function of load capacitance.

## MAXIMUM RATINGS, Absolute-Maximum Values:

### DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal) ..... -0.5V to +20V

### INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to V<sub>DD</sub> +0.5V

### DC INPUT CURRENT, ANY ONE INPUT

±10mA

### POWER DISSIPATION PER PACKAGE (P<sub>D</sub>)

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW

### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

### OPERATING-TEMPERATURE RANGE (T<sub>A</sub>)

-55°C to +125°C

### STORAGE TEMPERATURE RANGE (T<sub>STG</sub>)

-65°C to +150°C

### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

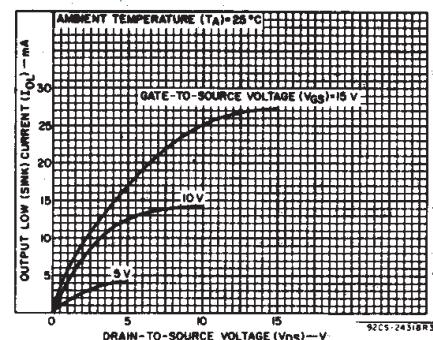


Fig. 3 – Typical output low (sink) current characteristics.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						U N I T S	
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
Quiescent Device Current, I <sub>DD</sub> Max.	–	0,5	5	5	5	150	150	–	0,04	5	μA
	–	0,10	10	10	10	300	300	–	0,04	10	
	–	0,15	15	20	20	600	600	–	0,04	20	
	–	0,20	20	100	100	3000	3000	–	0,08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	–	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	–	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	–	
Output High (Source) Current, I <sub>OH</sub> Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	–	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	–	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	–	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	–	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	–	0,5	5	0,05			–	0	0,05	–	V
	–	0,10	10	0,05			–	0	0,05	–	
	–	0,15	15	0,05			–	0	0,05	–	
Output Voltage: High-Level, V <sub>OH</sub> Min.	–	0,5	5	4,95			4,95	5	–	–	V
	–	0,10	10	9,95			9,95	10	–	–	
	–	0,15	15	14,95			14,95	15	–	–	
Input Low Voltage V <sub>IL</sub> Max.	0,5,4,5	–	5	4,5			–	–	1,5	–	V
	1,9	–	10	3			–	–	3	–	
	1,5,13,5	–	15	4			–	–	4	–	
Input High Voltage, V <sub>IH</sub> Min.	0,5,4,5	–	5	3,5			3,5	–	–	–	V
	1,9	–	10	7			7	–	–	–	
	1,5,13,5	–	15	11			11	–	–	–	
Input Current I <sub>IN</sub> Max.	–	0,18	18	±0,1	±0,1	±1	±1	–	±10 <sup>-5</sup>	±0,1	μA
3-State Output Leakage Current I <sub>OUT</sub> Max.	0,18	0,18	18	±0,4	±0,4	±12	±12	–	±10 <sup>-4</sup>	±0,4	μA

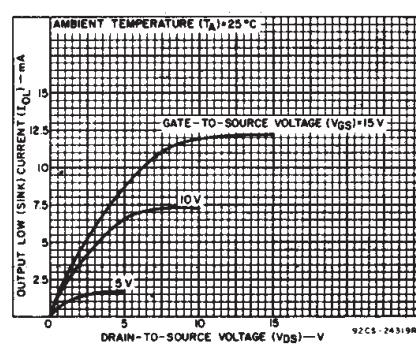


Fig. 4 – Minimum output low (sink) current characteristics.

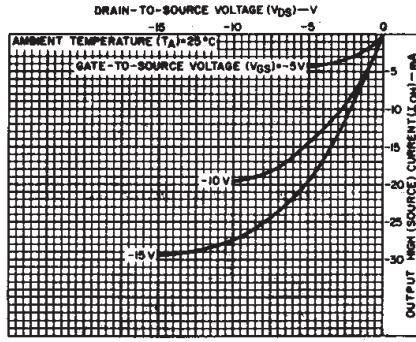


Fig. 5 – Typical output high (source) current characteristics.

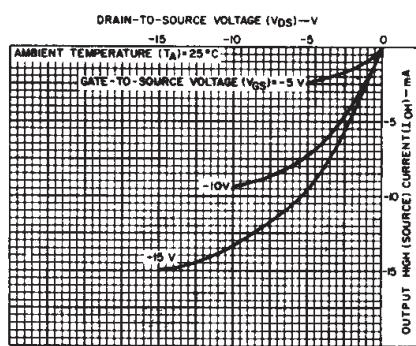


Fig. 6 – Minimum output high (source) current characteristics.

## CD4512B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
	$V_{DD}$ (V)	Typ.	Max.		
Propagation Delay Time, $t_{PHL}, t_{PLH}$ Inhibit to Output	5	140	280		ns
	10	70	140		
	15	50	100		
"A" Select to Output	5	200	400		ns
	10	85	170		
	15	60	120		
Data to Output	5	180	360		
	10	75	150		
	15	55	110		
3-State Disable Delay Time: $t_{PZL}, t_{PLZ}, t_{PHZ}, t_{PZH}$	5	60	120		ns
	10	30	60		
	15	20	40		
Transition Time, $t_{THL}, t_{TLH}$	5	100	200		ns
	10	50	100		
	15	40	80		
Input Capacitance, $C_{IN}$ (Any Input)			5	7.5	pF

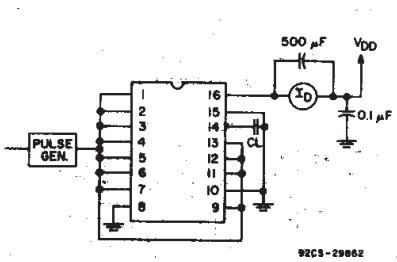


Fig. 9 – Dynamic power dissipation test circuit.

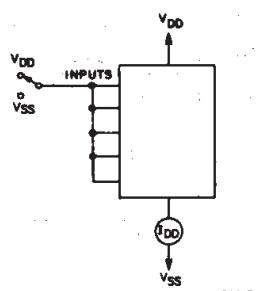


Fig. 10 – Quiescent device current test circuit.

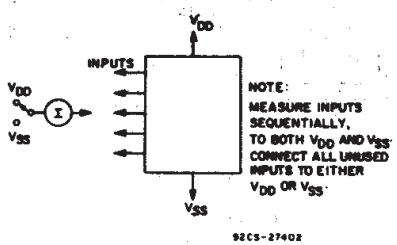


Fig. 11 – Input current test circuit.

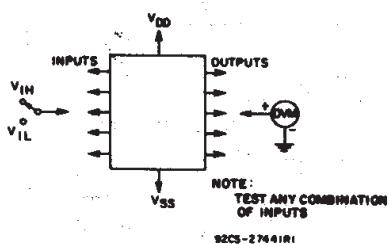


Fig. 12 – Input voltage test circuit.

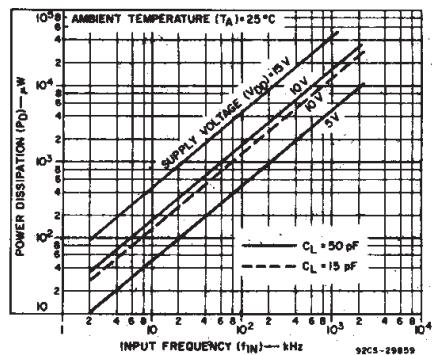


Fig. 7 – Typical dynamic power dissipation as a function of frequency.

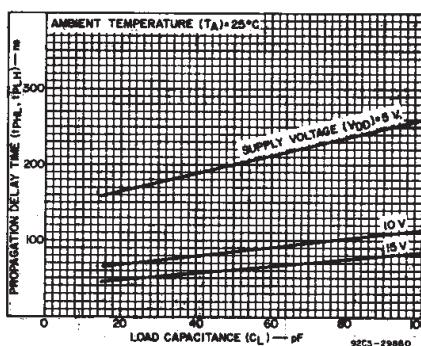
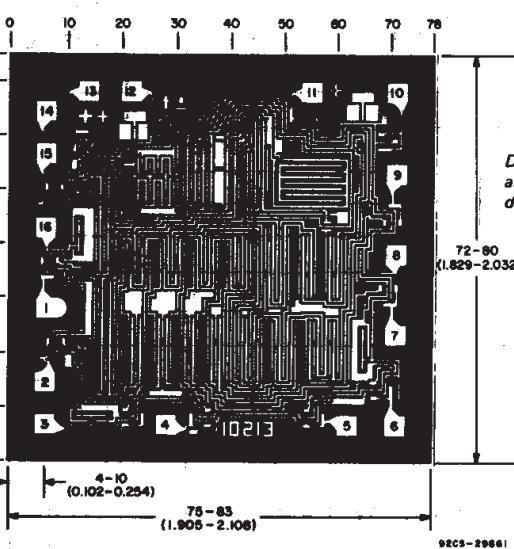


Fig. 8 – Typical propagation delay time as a function of load capacitance ("A" select to output).



Dimensions and pad layout for CD4512BH

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4512BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4512BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4512BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4512BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4512BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4512BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

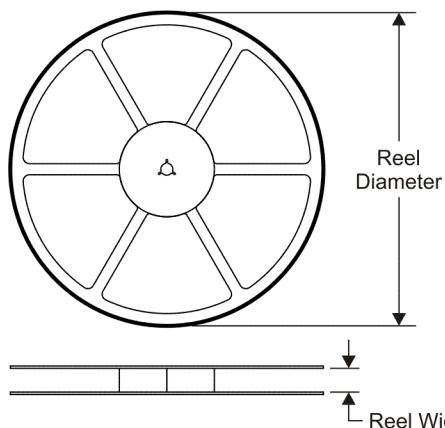
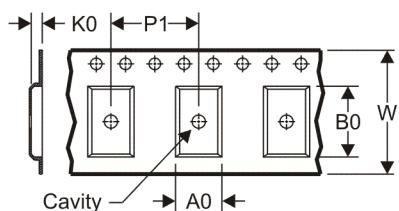
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

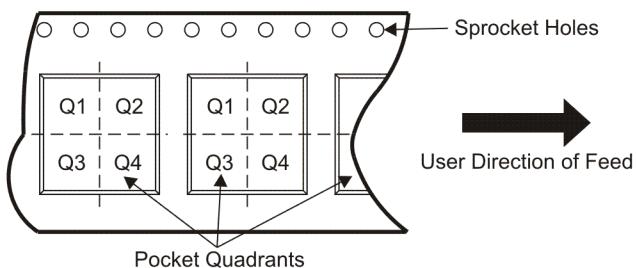
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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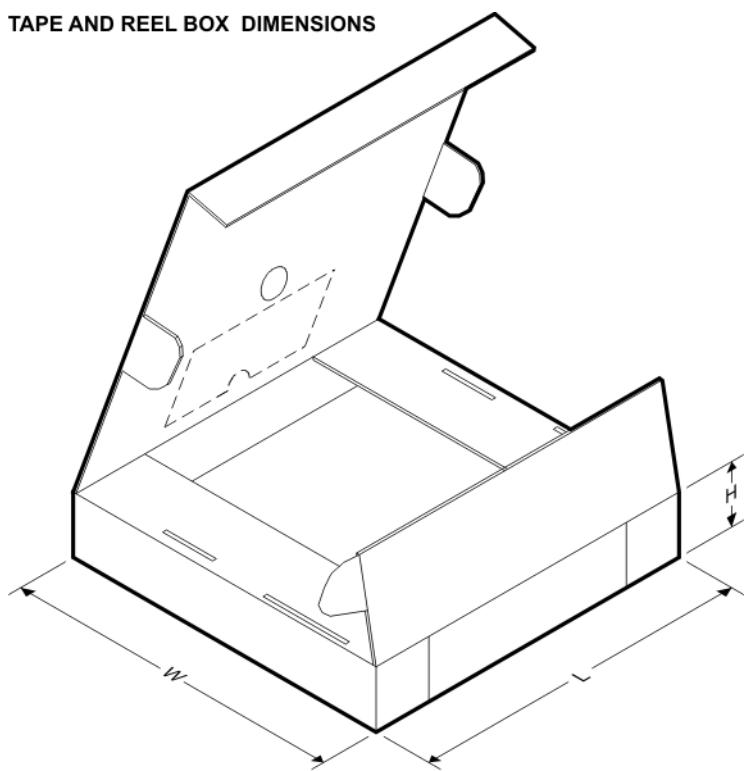
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4512BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4512BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4512BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


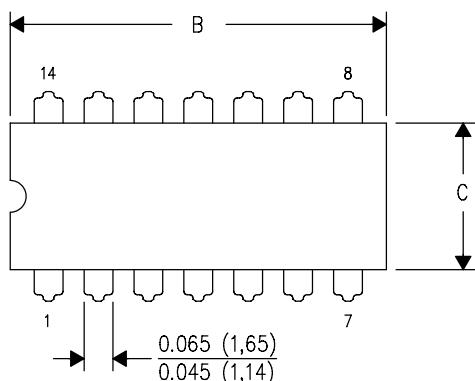
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4512BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4512BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4512BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

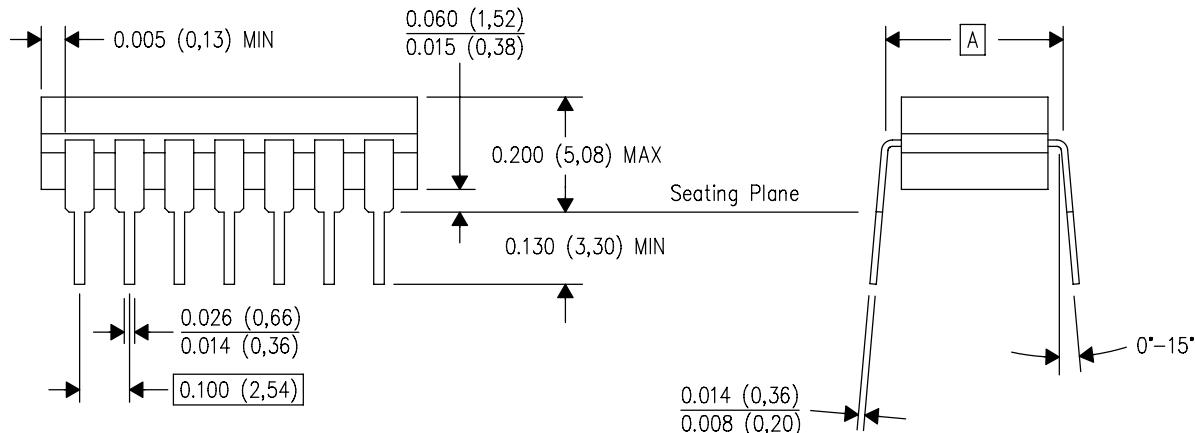
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



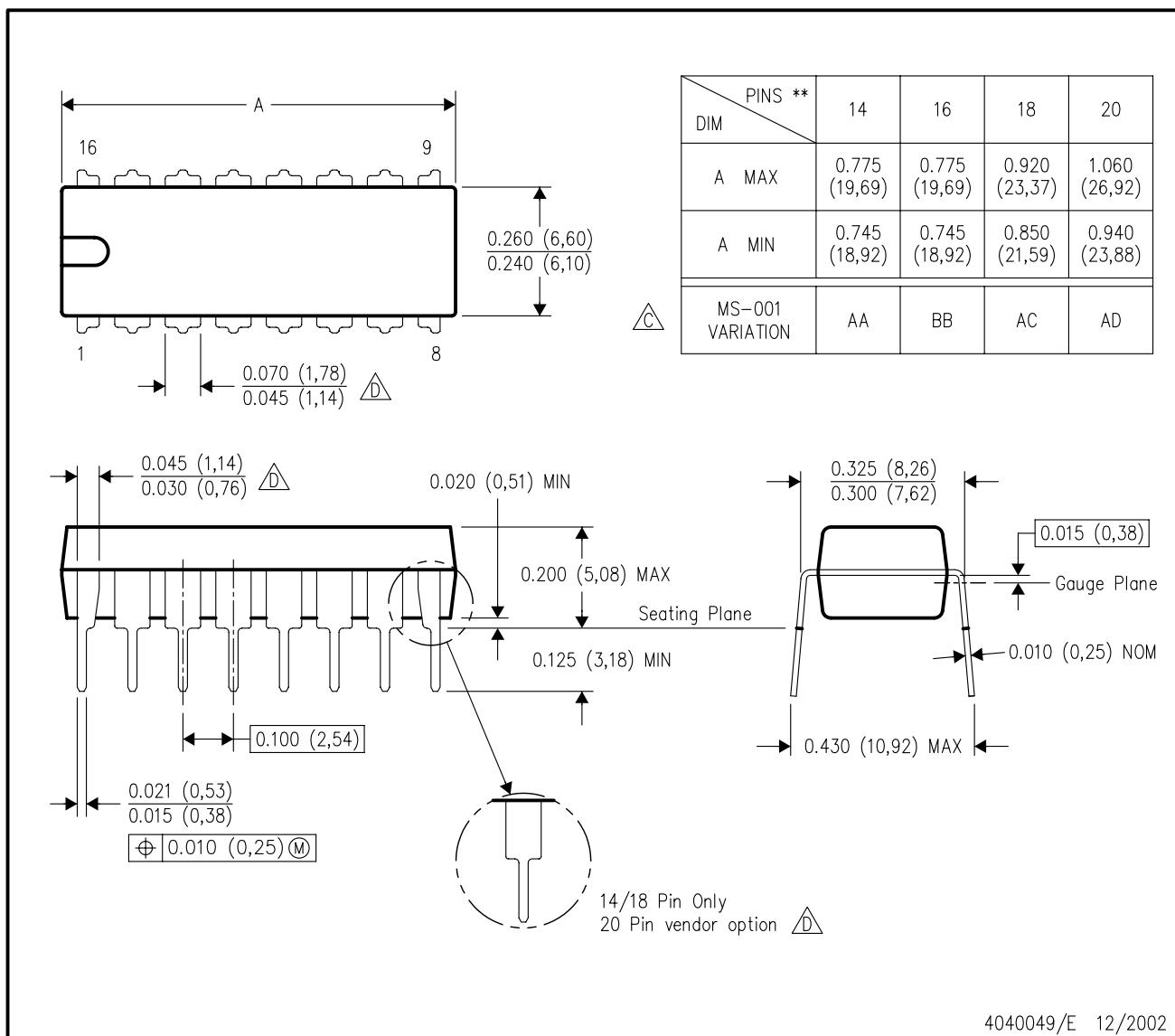
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



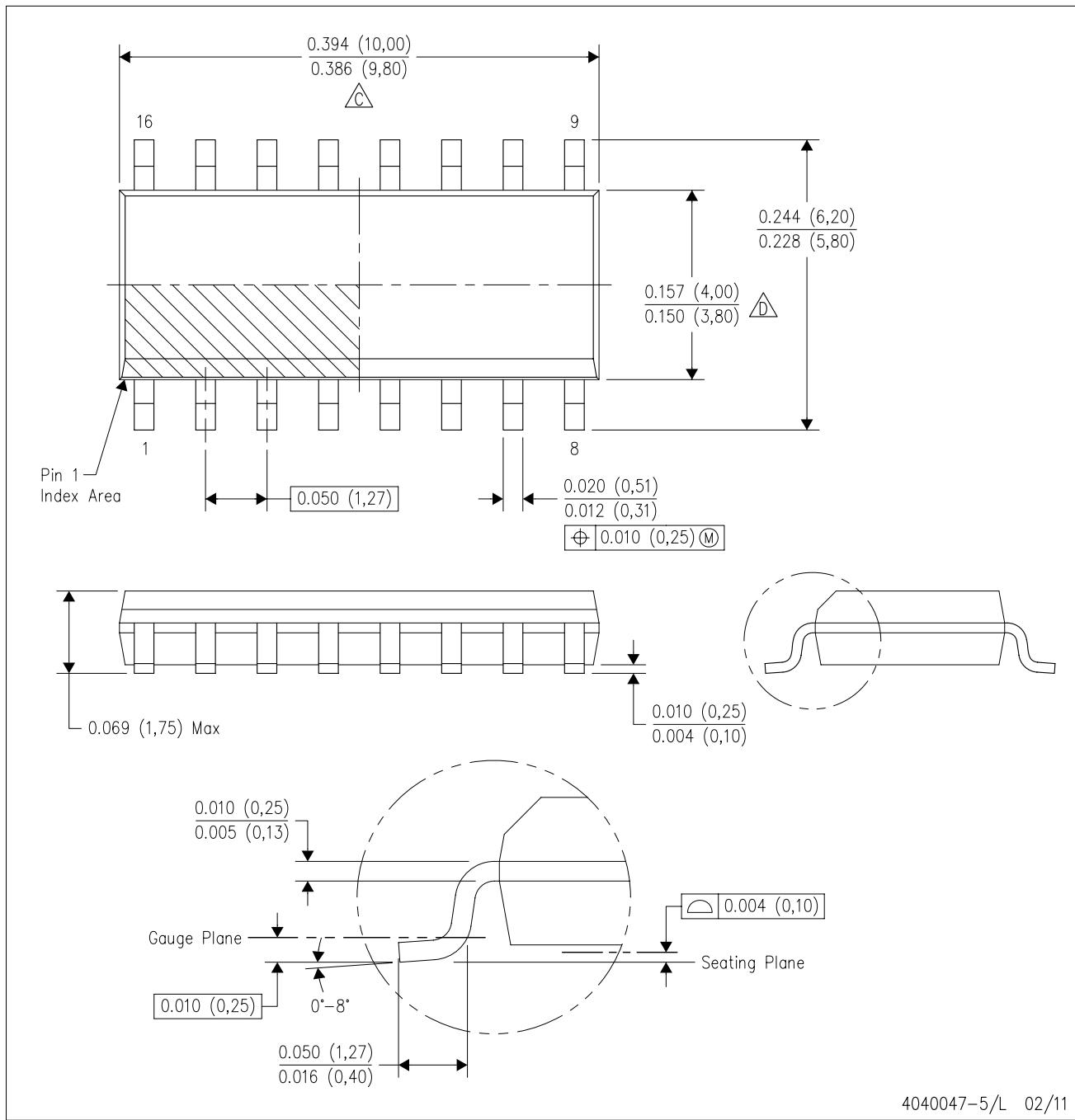
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

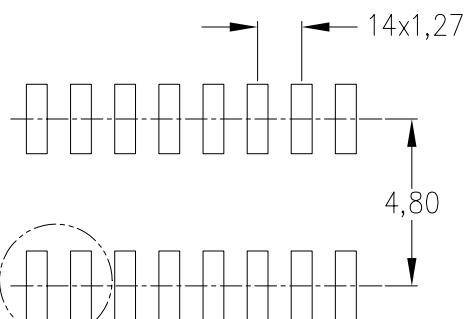
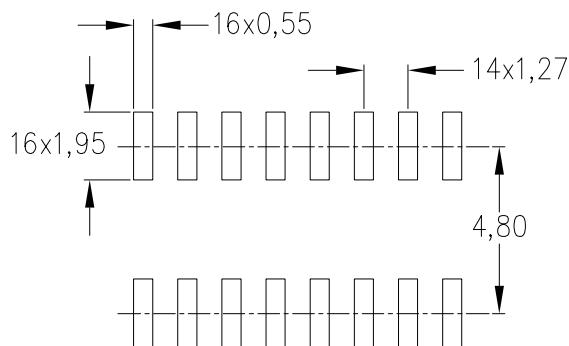
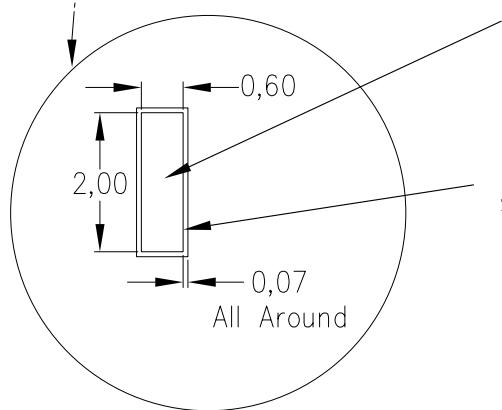
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

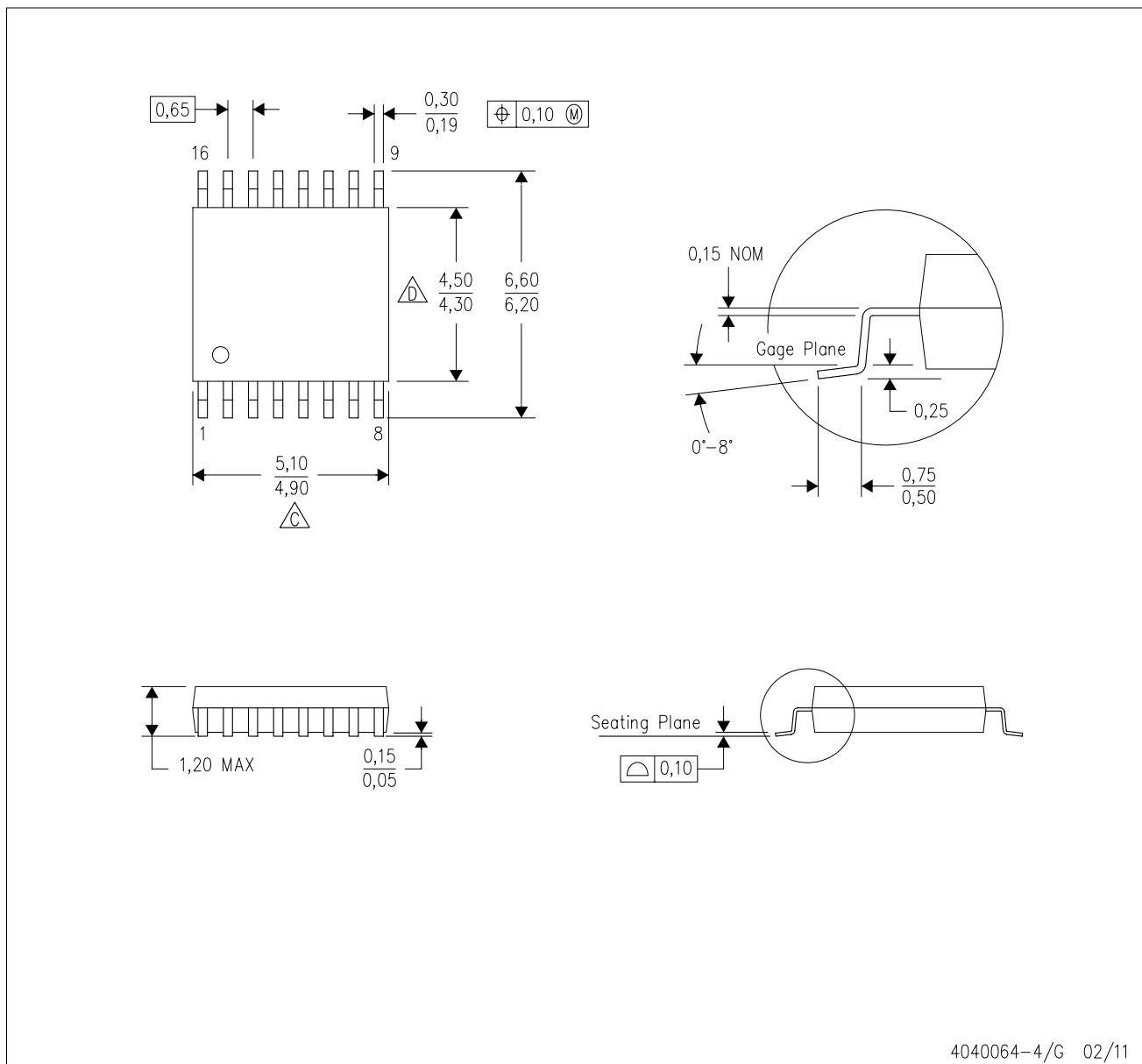
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NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

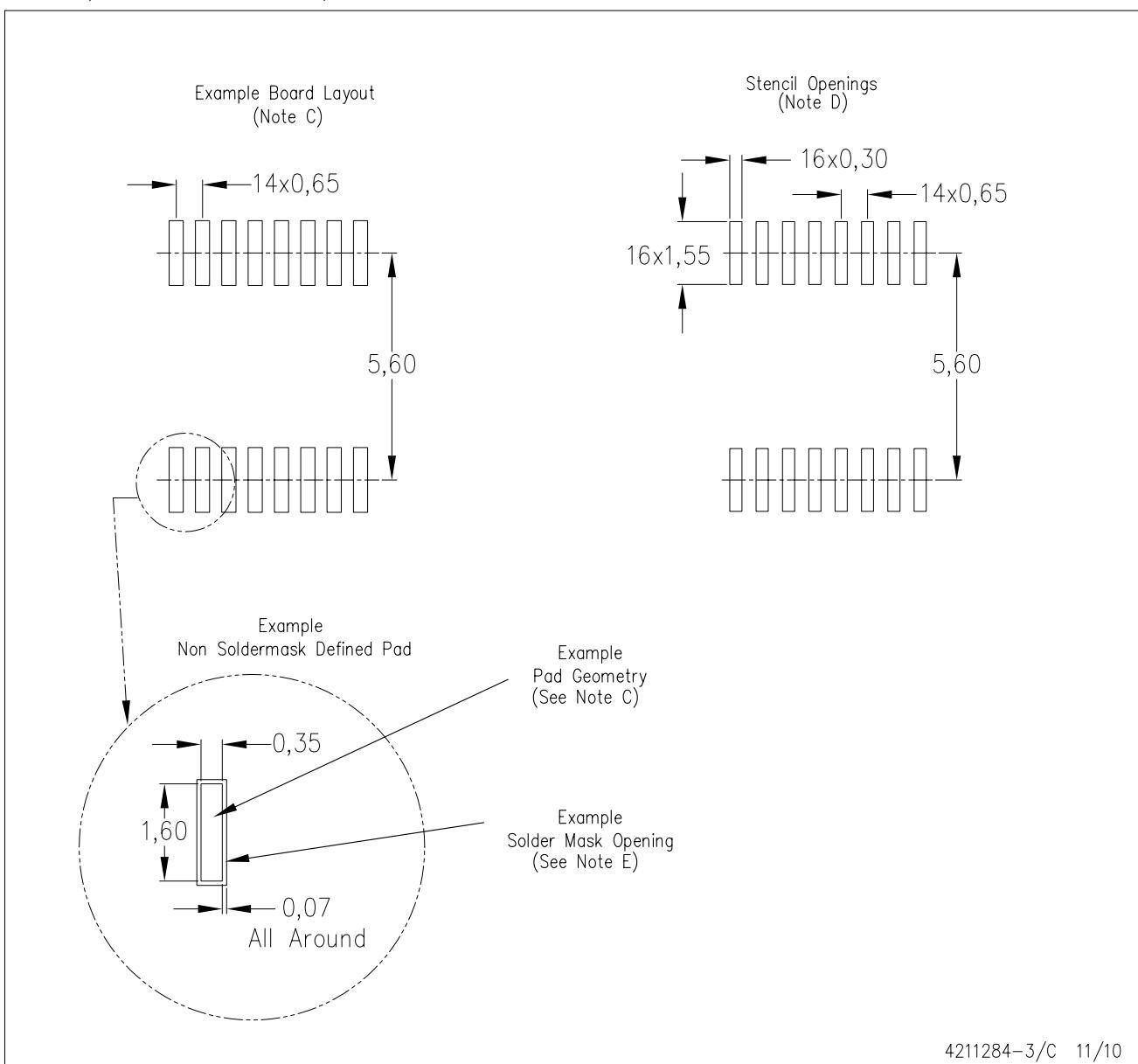
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

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PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/C 11/10

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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