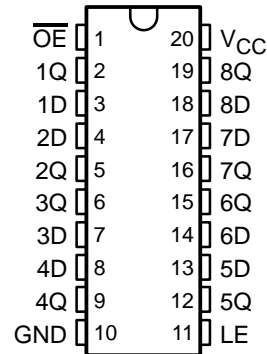


# CD54HC373, CD74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS452A – FEBRUARY 2001 – REVISED APRIL 2003

- 2-V to 6-V  $V_{CC}$  Operation
- Wide Operating Temperature Range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive up to 15 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs

CD54HC373 . . . F PACKAGE  
CD74HC373 . . . E OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The 'HC373 devices are octal transparent D-type latches designed for 2-V to 6-V  $V_{CC}$  operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	PDIP – E	Tube	CD74HC373E	CD74HC373E
	SOIC – M	Tube	CD74HC373M	HC373M
		Tape and reel	CD74HC373M96	
	CDIP – F	Tube	CD54HC373F3A	CD54HC373F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

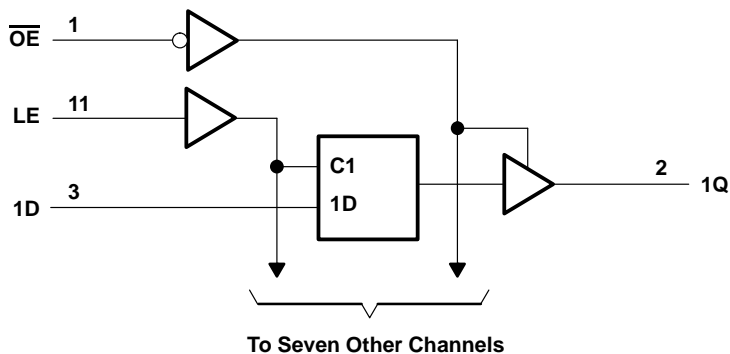
# CD54HC373, CD74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output drain current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous output source or sink current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package	69°C/W
M package	58°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**CD54HC373, CD74HC373**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 4.5 V	3.15	
		V <sub>CC</sub> = 6 V	4.2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 4.5 V	1.35	
		V <sub>CC</sub> = 6 V	1.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
t <sub>t</sub>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	1000	ns
		V <sub>CC</sub> = 4.5 V	500	
		V <sub>CC</sub> = 6 V	400	
T <sub>A</sub>	Operating free-air temperature	-55	125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.9	1.9	V		
			4.5 V	4.4	4.4	4.4			
			6 V	5.9	5.9	5.9			
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	3.7	3.84			
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.2	5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.1	0.1	0.1	V		
			4.5 V	0.1	0.1	0.1			
			6 V	0.1	0.1	0.1			
		I <sub>OL</sub> = 6 mA	4.5 V	0.26	0.4	0.33			
		I <sub>OL</sub> = 7.8 mA	6 V	0.26	0.4	0.33			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±1	±1	μA			
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0	6 V	±0.5	±10	±5	μA			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V	8	160	80	μA			
C <sub>i</sub>			10	10	10	pF			
C <sub>o</sub>			20	20	20	pF			



**CD54HC373, CD74HC373**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$ Pulse duration, LE high	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
$t_{su}$ Setup time, data before LE↓	2 V	50		75		65		ns
	4.5 V	10		15		13		
	6 V	9		13		11		
$t_h$ Hold time, data after LE↓	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

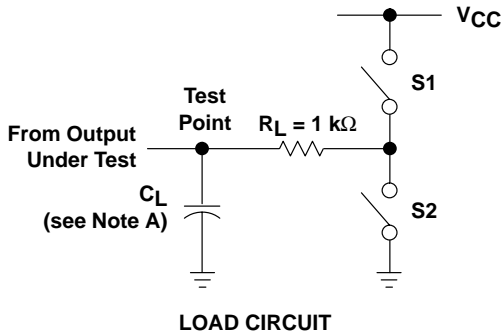
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
	LE	Q	$C_L = 50\text{ pF}$	2 V	175		265		220		
				4.5 V	35		53		44		
				6 V	30		45		37		
$t_{en}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
$t_{dis}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
$t_t$		Q	$C_L = 50\text{ pF}$	2 V	60		90		75	ns	
				4.5 V	12		18		15		
				6 V	10		15		13		

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

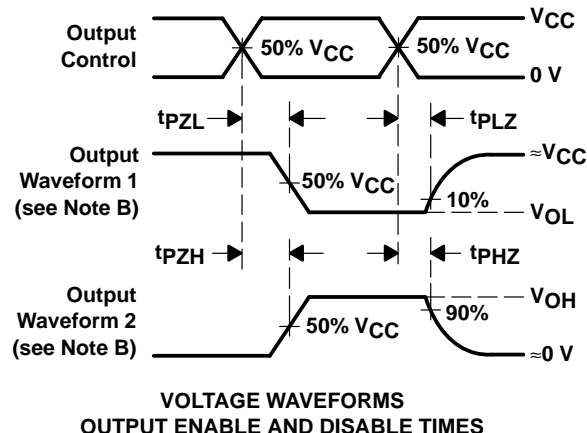
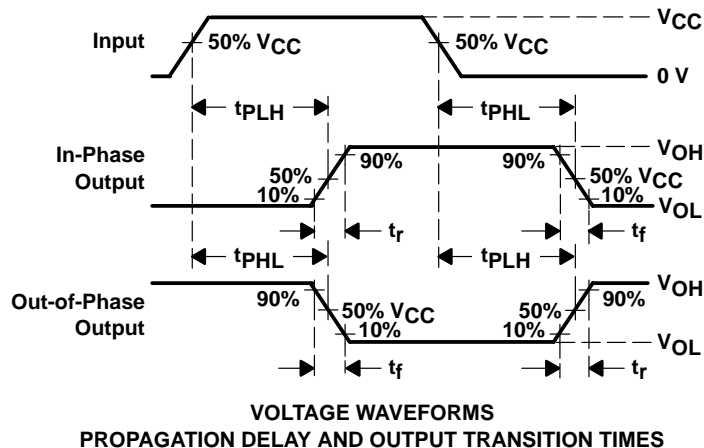
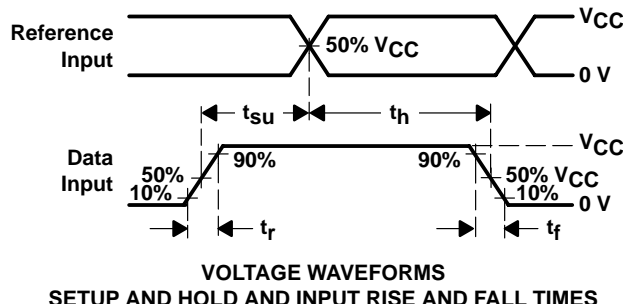
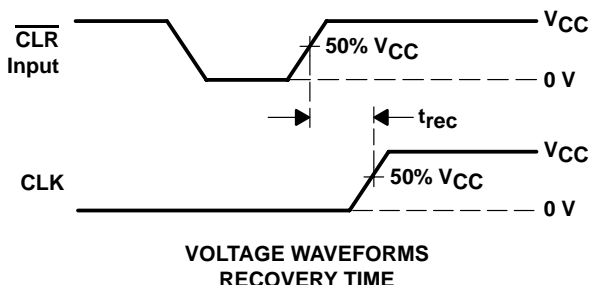
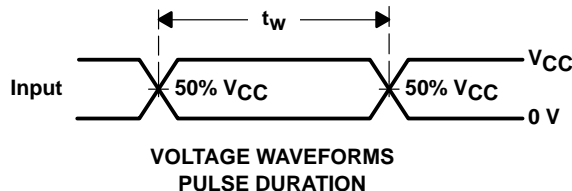
PARAMETER	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	51	pF



PARAMETER MEASUREMENT INFORMATION



PARAMETER	S1	S2
$t_{en}$	tpZH	Open
	tpZL	Closed
$t_{dis}$	tpHZ	Open
	tpLZ	Closed
$t_{pd}$ or $t_f$	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 6\text{ ns}$ ,  $t_f = 6\text{ ns}$ .  
 D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.  
 E. The outputs are measured one at a time with one input transition per measurement.  
 F.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .  
 G.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .  
 H.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .  
 I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002





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