

### Features

- Three-State Outputs
- Separate Output Enable Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC125 and 'HCT125 contain 4 independent three-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high impedance state.

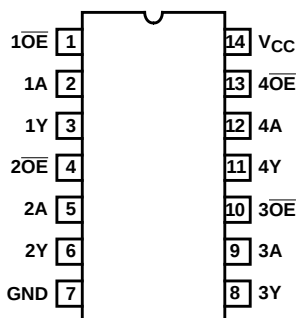
### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC125F3A  | -55 to 125       | 14 Ld CERDIP |
| CD54HCT125F3A | -55 to 125       | 14 Ld CERDIP |
| CD74HC125E    | -55 to 125       | 14 Ld PDIP   |
| CD74HC125M    | -55 to 125       | 14 Ld SOIC   |
| CD74HC125MT   | -55 to 125       | 14 Ld SOIC   |
| CD74HC125M96  | -55 to 125       | 14 Ld SOIC   |
| CD74HCT125E   | -55 to 125       | 14 Ld PDIP   |
| CD74HCT125M   | -55 to 125       | 14 Ld SOIC   |
| CD74HCT125MT  | -55 to 125       | 14 Ld SOIC   |
| CD74HCT125M96 | -55 to 125       | 14 Ld SOIC   |

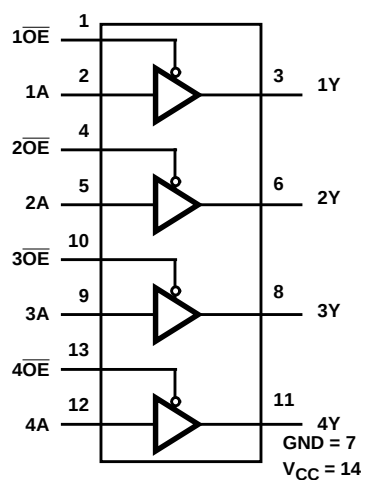
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

CD54HC125, CD54HCT125  
(CERDIP)  
CD74HC125, CD74HCT125  
(PDIP, SOIC)  
TOP VIEW



## Functional Diagram



TRUTH TABLE

| INPUTS |     | OUTPUTS |
|--------|-----|---------|
| nA     | nOE | nY      |
| H      | L   | H       |
| L      | L   | L       |
| X      | H   | Z       |

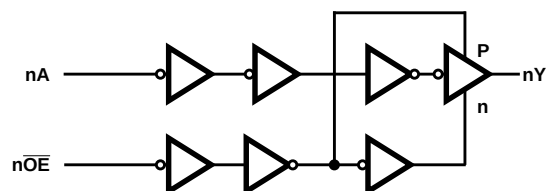
H= High Voltage Level

L= Low Voltage Level

X= Don't Care

Z= High Impedance, OFF State

## Logic Diagram



# CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Drain Current, per Output,  $I_O$   
 For  $-0.5V < V_O < V_{CC} + 0.5V$  .....  $\pm 35mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  .....  $\pm 70mA$

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^{\circ}C/W$ )  
 E (PDIP) Package ..... 80  
 M (SOIC) Package ..... 86  
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
 (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                       |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|---------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                    | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                       |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                     | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                       |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                     | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                       | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                       | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  |                 |                                       | -6                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                       | -7.8                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   |                 |                                       | 6                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                       | 7.8                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or<br>GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |

**CD54HC125, CD74HC125, CD54HCT125, CD74HCT125**

**DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                      | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |          | UNITS   |
|----------------------------------------------------------------|-----------------------------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|----------|---------|
|                                                                |                             | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX      |         |
| Quiescent Device Current                                       | $I_{CC}$                    | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160      | $\mu A$ |
| Three-State Leakage Current                                    | $I_{OZ}$                    | $V_{IL}$ or $V_{IH}$ | -          | 6            | -    | -   | $\pm 0.5$ | -             | $\pm 5$ | -              | $\pm 10$ | $\mu A$ |
| <b>HCT TYPES</b>                                               |                             |                      |            |              |      |     |           |               |         |                |          |         |
| High Level Input Voltage                                       | $V_{IH}$                    | -                    | -          | 4.5 to 5.5   | 2    | -   | -         | 2             | -       | 2              | -        | V       |
| Low Level Input Voltage                                        | $V_{IL}$                    | -                    | -          | 4.5 to 5.5   | -    | -   | 0.8       | -             | 0.8     | -              | 0.8      | V       |
| High Level Output Voltage<br>CMOS Loads                        | $V_{OH}$                    | $V_{IH}$ or $V_{IL}$ | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -        | V       |
| High Level Output Voltage<br>TTL Loads                         |                             |                      | -6         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -        | V       |
| Low Level Output Voltage<br>CMOS Loads                         | $V_{OL}$                    | $V_{IH}$ or $V_{IL}$ | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1      | V       |
| Low Level Output Voltage<br>TTL Loads                          |                             |                      | 6          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4      | V       |
| Input Leakage Current                                          | $I_I$                       | $V_{CC}$ to GND      | 0          | 5.5          | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$  | $\mu A$ |
| Quiescent Device Current                                       | $I_{CC}$                    | $V_{CC}$ or GND      | 0          | 5.5          | -    | -   | 8         | -             | 80      | -              | 160      | $\mu A$ |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$<br>(Note 2) | $V_{CC}$ -2.1        | -          | 4.5 to 5.5   | -    | 100 | 360       | -             | 450     | -              | 490      | $\mu A$ |
| Three-State Leakage Current                                    | $I_{OZ}$                    | $V_{IL}$ or $V_{IH}$ | -          | 5.5          | -    | -   | $\pm 0.5$ | -             | $\pm 5$ | -              | $\pm 10$ | $\mu A$ |

NOTE:

- For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT                | UNIT LOADS |
|----------------------|------------|
| nA, $n\overline{OE}$ | 1          |

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360 $\mu A$  max at 25°C.

# CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

## Switching Specifications Input $t_r, t_f = 6\text{ns}$

| PARAMETER                                        | SYMBOL                              | TEST<br>CONDITIONS    | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|--------------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
|                                                  |                                     |                       |                     | TYP  | MAX | MAX           | MAX            |       |
| HC TYPES                                         |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay Time<br>nA to nY               | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 100 | 125           | 150            | ns    |
|                                                  |                                     |                       | 4.5                 | -    | 20  | 25            | 30             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 8    | -   | -             | -              | ns    |
|                                                  |                                     | CL = 50pF             | 6                   | -    | 17  | 21            | 26             | ns    |
| Enable Delay Time                                | t <sub>PZL</sub> , t <sub>PZH</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 125 | 155           | 190            | ns    |
|                                                  |                                     |                       | 4.5                 | -    | 25  | 31            | 38             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 10   | -   | -             | -              | ns    |
|                                                  |                                     | CL = 50pF             | 6                   | -    | 21  | 26            | 32             | ns    |
| Disable Delay Time                               | t <sub>PLZ</sub> , t <sub>PHZ</sub> | CL = 50pF             | 2                   | -    | 125 | 155           | 190            | ns    |
|                                                  |                                     | C <sub>L</sub> = 50pF | 4.5                 | -    | 25  | 31            | 38             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 10   | -   | -             | -              | ns    |
|                                                  |                                     | CL = 50pF             | 6                   | -    | 21  | 26            | 32             | ns    |
| Output Transition Time                           | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 60  | 75            | 90             | ns    |
|                                                  |                                     |                       | 4.5                 | -    | 12  | 15            | 18             | ns    |
|                                                  |                                     |                       | 6                   | -    | 10  | 13            | 15             | ns    |
| Input Capacitance                                | C <sub>I</sub>                      | -                     | -                   | -    | 10  | 10            | 10             | pF    |
| Three-State Output<br>Capacitance                | C <sub>O</sub>                      | -                     | -                   | -    | 20  | 20            | 20             | pF    |
| Power Dissipation<br>Capacitance<br>(Notes 3, 4) | C <sub>PD</sub>                     | -                     | 5                   | 29   | -   | -             | -              | pF    |
| HCT TYPES                                        |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay Time<br>nA to nY               | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 25  | 31            | 38             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 10   | -   | -             | -              | ns    |
| Output Enable Time                               | t <sub>PZL</sub> , t <sub>PZH</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 25  | 31            | 38             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 10   | -   | -             | -              | ns    |
| Output Disabling Time                            | t <sub>PLZ</sub> , t <sub>PHZ</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 28  | 35            | 42             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 11   | -   | -             | -              | ns    |
| Output Transition Times                          | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 12  | 15            | 18             | ns    |
| Input Capacitance                                | C <sub>I</sub>                      | -                     | -                   | -    | 10  | 10            | 10             | pF    |
| Three-State Output<br>Capacitance                | C <sub>O</sub>                      | -                     | -                   | -    | 20  | 20            | 20             | pF    |
| Power Dissipation<br>Capacitance<br>(Notes 3, 4) | C <sub>PD</sub>                     | -                     | 5                   | 34   | -   | -             | -              | pF    |

### NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per channel.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms

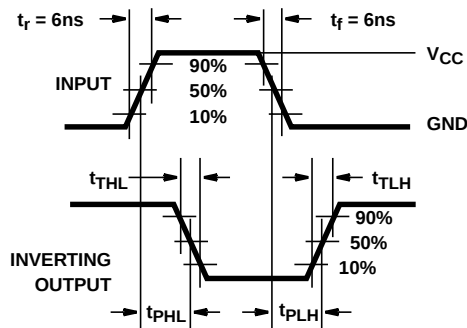


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

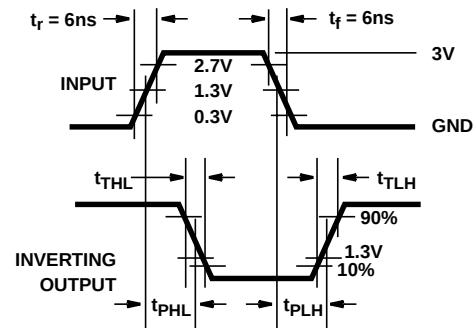


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

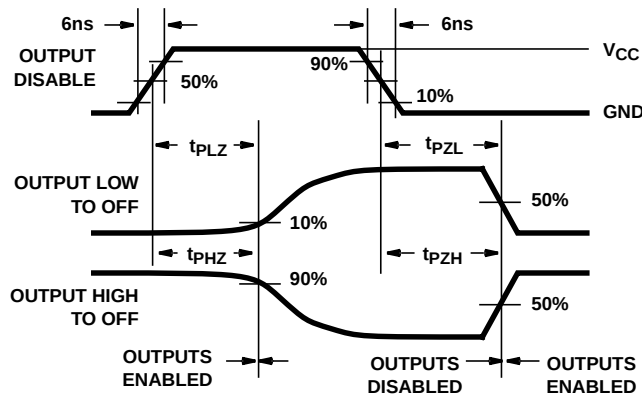


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

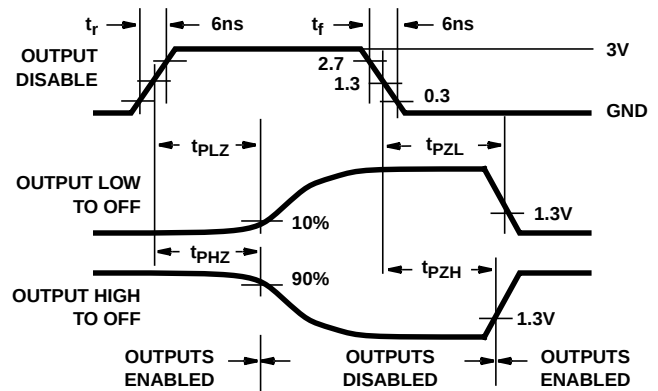
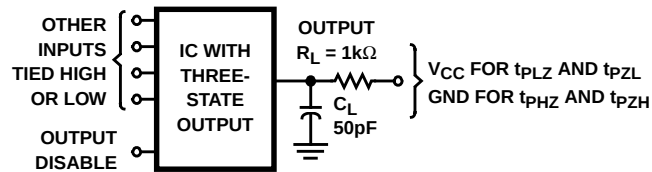


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD54HC125F       | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD54HC125F3A     | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD54HCT125F3A    | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD74HC125E       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HC125EE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HC125M       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125M96     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125M96E4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125M96G4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125ME4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125MG4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125MT      | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125MTE4    | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC125MTG4    | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125E      | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HCT125EE4    | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HCT125M      | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125M96    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125M96E4  | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125M96G4  | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125ME4    | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125MG4    | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125MT     | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125MTE4   | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT125MTG4   | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF CD54HC125, CD54HCT125, CD74HC125, CD74HCT125 :**

- Automotive: [CD74HC125-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC125M96  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC125MT   | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT125M96 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT125MT  | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC125M96  | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| CD74HC125MT   | SOIC         | D               | 14   | 250  | 346.0       | 346.0      | 33.0        |
| CD74HCT125M96 | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| CD74HCT125MT  | SOIC         | D               | 14   | 250  | 346.0       | 346.0      | 33.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



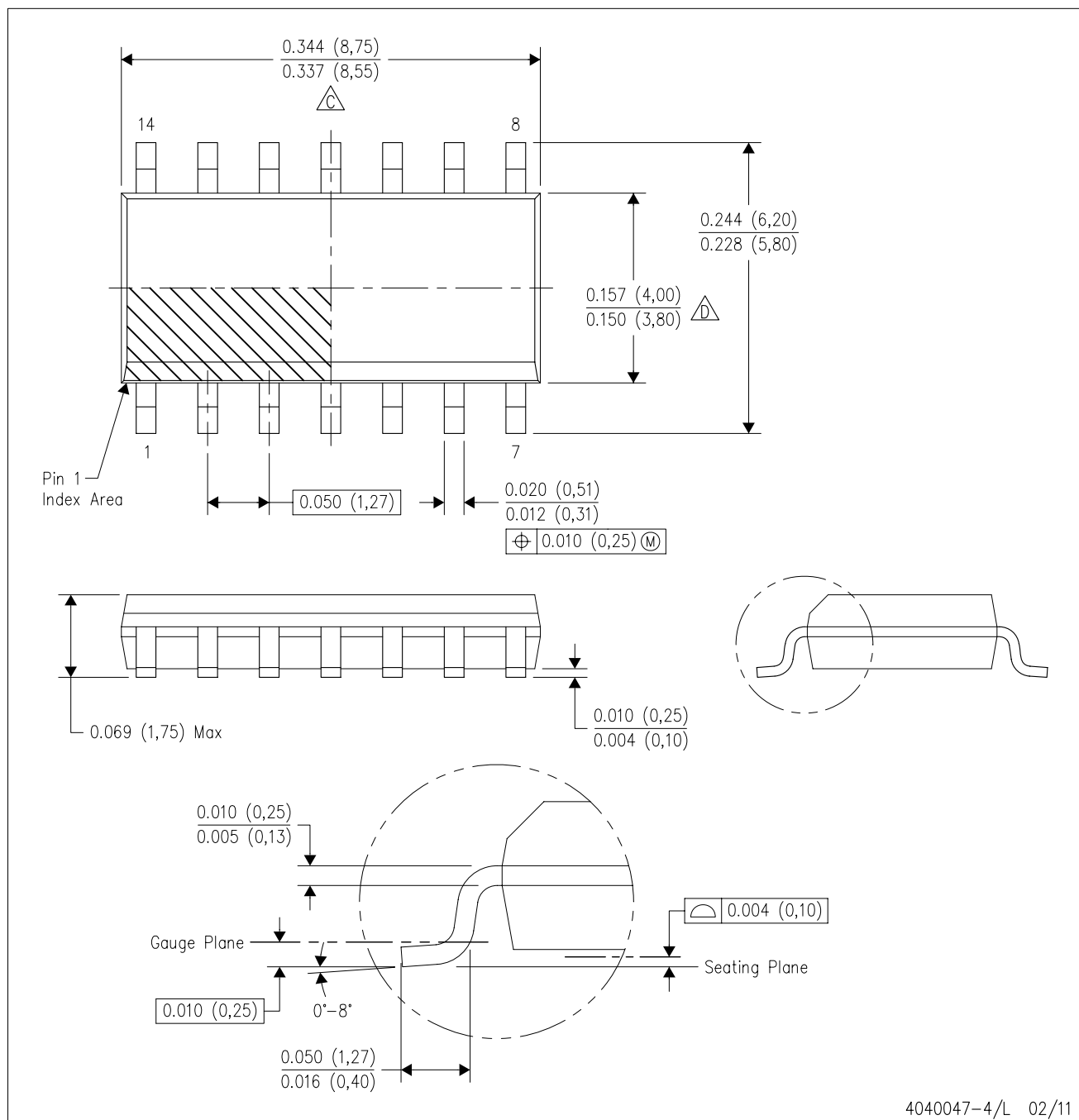
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

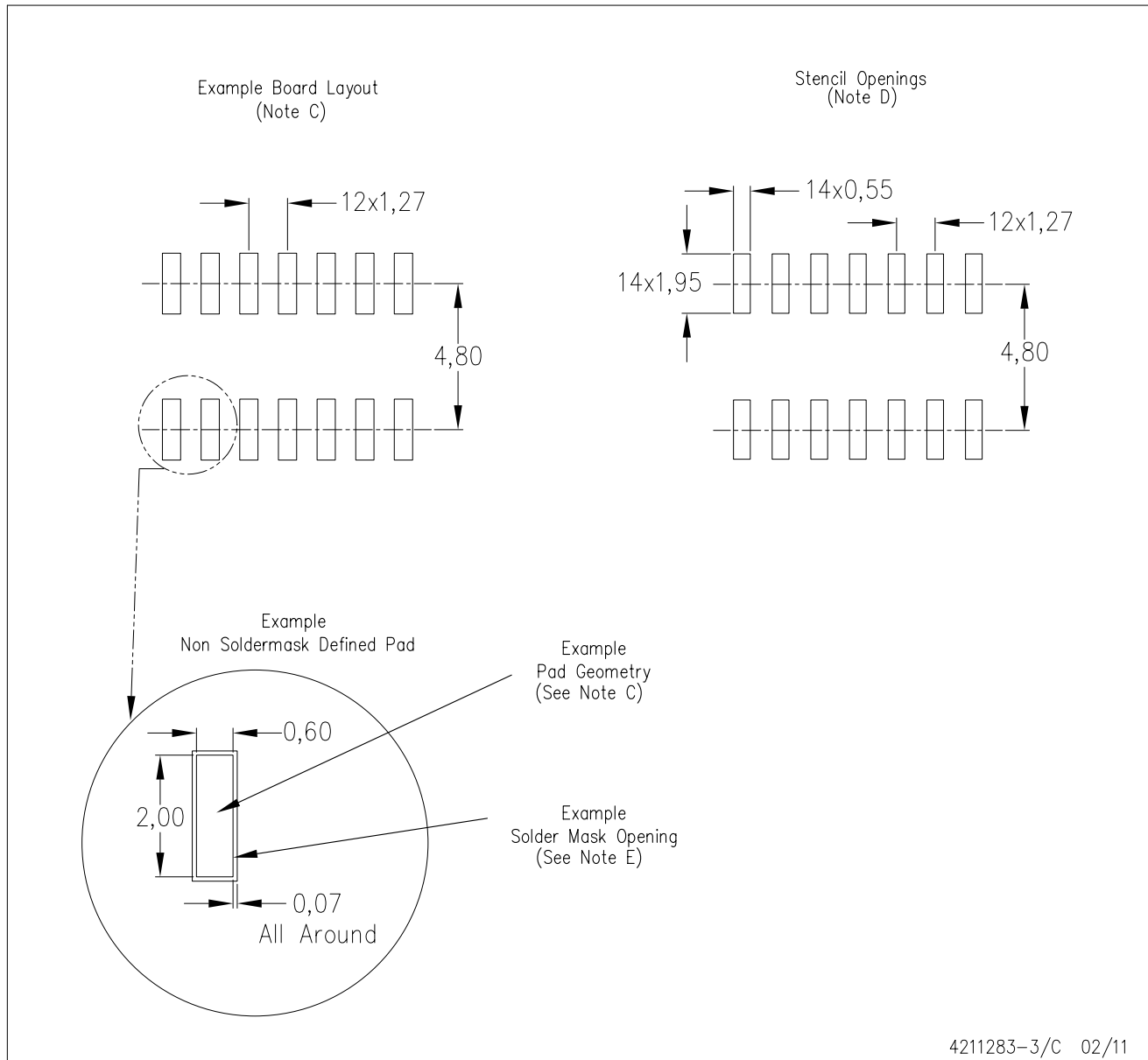
PLASTIC SMALL OUTLINE



4040047-4/L 02/11

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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|                               |                                                                                          |
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