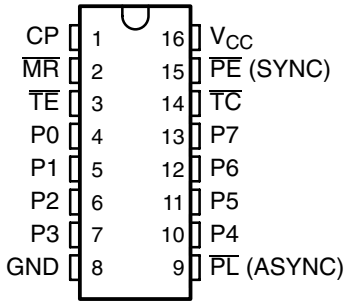
- **Qualified for Automotive Applications**
- **Synchronous or Asynchronous Preset**
- **Cascadable in Synchronous or Ripple Mode**
- **Fanout (Over Temperature Range)**
  - **– Standard Outputs . . . 10 LSTTL Loads**
  - **– Bus Driver Outputs . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 2 V to 6 V**
- **High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V**

M PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC40103 is manufactured with high-speed silicon-gate technology and consists of an 8-stage synchronous down counter with a single output, which is active when the internal count is zero. The device contains a single 8-bit binary counter. Each device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count ($\overline{TC}$) output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the clock (CP) output. Counting is inhibited when the terminal enable ($\overline{TE}$) input is high. $\overline{TC}$ goes low when the count reaches zero, if $\overline{TE}$ is low, and remains low for one full clock period.

When the synchronous preset enable ($\overline{PE}$) input is low, data at the P0–P7 inputs are clocked into the counter on the next positive clock transition, regardless of the state of $\overline{TE}$. When the asynchronous preset enable ($\overline{PL}$) input is low, data at the P0–P7 inputs asynchronously are forced into the counter, regardless of the state of the $\overline{PE}$, $\overline{TE}$, or CP inputs. Inputs P0–P7 represent a single 8-bit binary word for the CD74HC40103. When the master reset ($\overline{MR}$) input is low, the counter asynchronously is cleared to its maximum count of 255_{10}, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except $\overline{TE}$ are high at the time of zero count, the counters jump to the maximum count, giving a counting sequence of 100_{16} or 256_{10} clock pulses long.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC40103QM96Q1	HC40103Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

description/ordering information (continued)

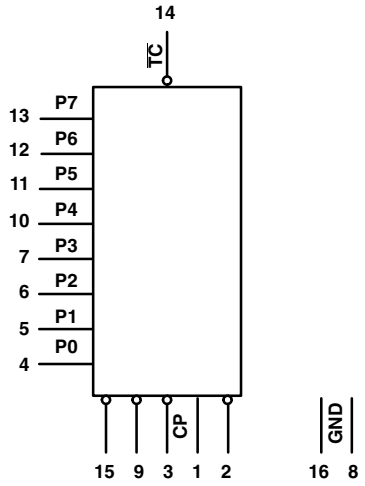
The CD74HC40103 may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either synchronous or ripple mode. These circuits have the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits and can drive up to ten LSTTL loads.

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	Synchronous	Inhibit counter
H	H	H	L		Count down
H	H	L	X		Preset on next positive clock transition
H	L	X	X	Asynchronous	Preset asynchronously
L	X	X	X		Clear to maximum count

NOTE: H = high voltage level, L = low voltage level, X = don't care
Clock connected to clock input
Synchronous operation: changes occur on negative-to-positive clock transitions.
Load inputs: MSB = P7, LSB = P0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V) . . . . . ±20 mA
Source or sink current per output pin, I_O ($V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 73°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		–40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	T_A = 25°C		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	–0.02	2 V	1.9		1.9		V
			–0.02	4.5 V	4.4		4.4		
			–0.02	6 V	5.9		5.9		
		TTL loads	–4	4.5 V	3.98		3.7		
			–5.2	6 V	5.48		5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V		0.1		0.1	V
			0.02	4.5 V		0.1		0.1	
			0.02	6 V		0.1		0.1	
		TTL loads	4	4.5 V		0.26		0.4	
			5.2	6 V		0.26		0.4	
I_I	$V_I = V_{CC}$ or GND			6 V		±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V		8		160	µA
C_{IN}	C_L = 50 pF					10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_w	Pulse duration	CP	2 V	165		250		ns
			4.5 V	33		50		
			6 V	28		43		
		$\overline{PL}$	2 V	125		190		
			4.5 V	25		38		
			6 V	21		32		
		$\overline{MR}$	2 V	125		190		
			4.5 V	25		38		
			6 V	21		32		
f_{max}	CP frequency (see Note 4)		2 V	3		2		MHz
			4.5 V	15		10		
			6 V	18		12		
t_{su}	Setup time	P to CP	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		26		
		$\overline{PE}$ to CP	2 V	75		110		
			4.5 V	15		22		
			6 V	13		19		
		$\overline{TE}$ to CP	2 V	150		225		
			4.5 V	30		45		
			6 V	26		38		
		To CP, $\overline{MR}$ inactive	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
t_h	Hold time	P to CP	2 V	5		5		ns
			4.5 V	5		5		
			6 V	5		5		
		$\overline{TE}$ to CP	2 V	0		0		
			4.5 V	0		0		
			6 V	0		0		
		$\overline{PE}$ to CP	2 V	2		2		
			4.5 V	2		2		
			6 V	2		2		

NOTE 4: Noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, count enables ($\overline{PE}$ or $\overline{TE}$) to clock setup times, and count enables ($\overline{PE}$ or $\overline{TE}$) to clock hold times determine maximum clock frequency. For example, with these HC devices:

$$\text{CP } f_{max} = \frac{1}{\text{CP to } \overline{TC} \text{ prop delay} + \overline{TE} \text{ to CP setup time} + \overline{TE} \text{ to CP hold time}} = \frac{1}{60 + 30 + 0} \approx 11 \text{ MHz}$$

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

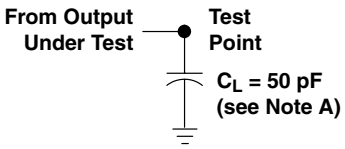
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t_{pd}	CP	$\overline{TC}$ (asynchronous preset)	C_L = 50 pF	2 V			300		450	ns
				4.5 V			60		90	
				6 V			51		77	
			C_L = 15 pF	5 V		25				
		$\overline{TC}$ (synchronous preset)	C_L = 50 pF	2 V			300		450	
				4.5 V			60		90	
				6 V			51		77	
			C_L = 15 pF	5 V		25				
	$\overline{TE}$	$\overline{TC}$	C_L = 50 pF	2 V			200		300	
				4.5 V			40		60	
				6 V			34		51	
			C_L = 15 pF	5 V		17				
	$\overline{PL}$	$\overline{TC}$	C_L = 50 pF	2 V			275		415	
				4.5 V			55		83	
				6 V			47		71	
			C_L = 15 pF	5 V		23				
	$\overline{MR}$	$\overline{TC}$	C_L = 50 pF	2 V			275		415	
				4.5 V			55		83	
				6 V			47		71	
			C_L = 15 pF	5 V		23				
t_t			C_L = 50 pF	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	
f_{max}	CP		C_L = 15 pF	5 V		25				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

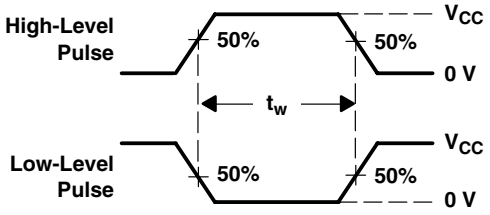
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 5)	25	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption per package.
$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_O)$
f_I = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

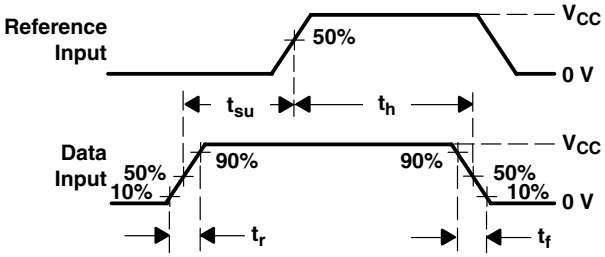
PARAMETER MEASUREMENT INFORMATION



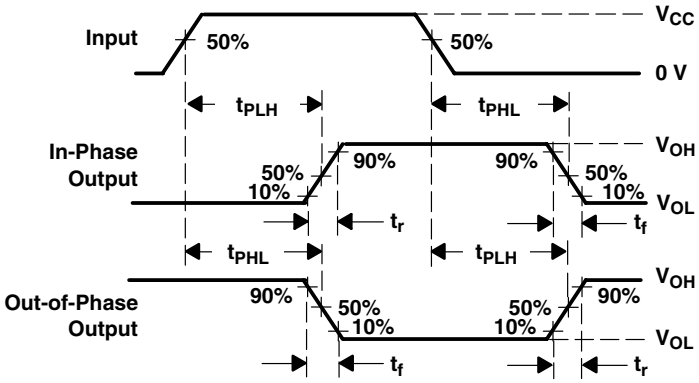
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

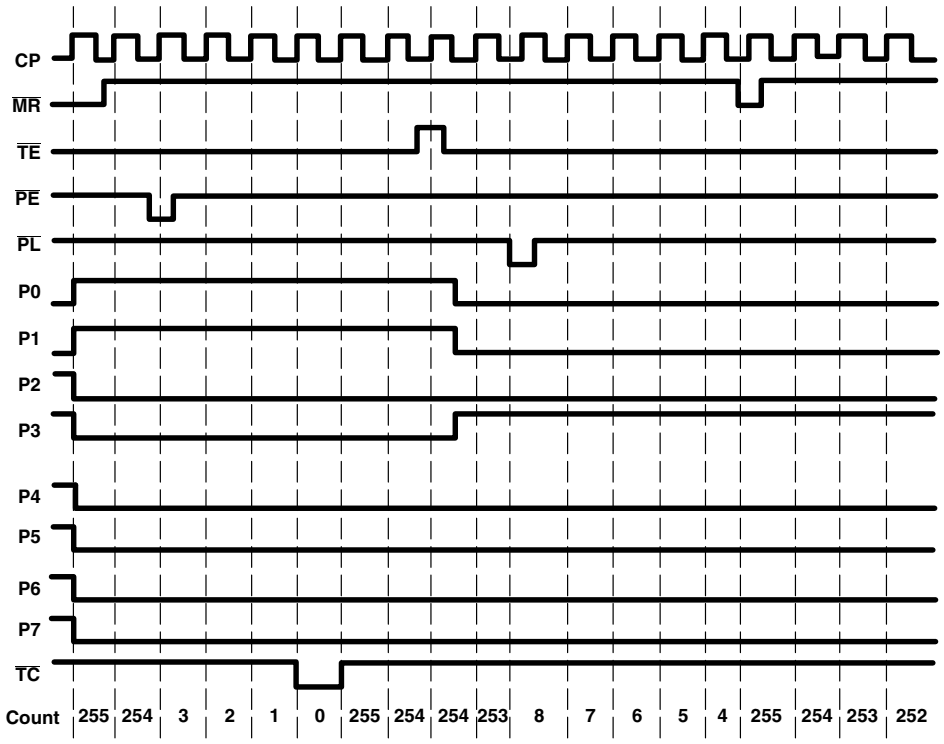


Figure 2. Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HC40103QM96Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
HC40103QM96G4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

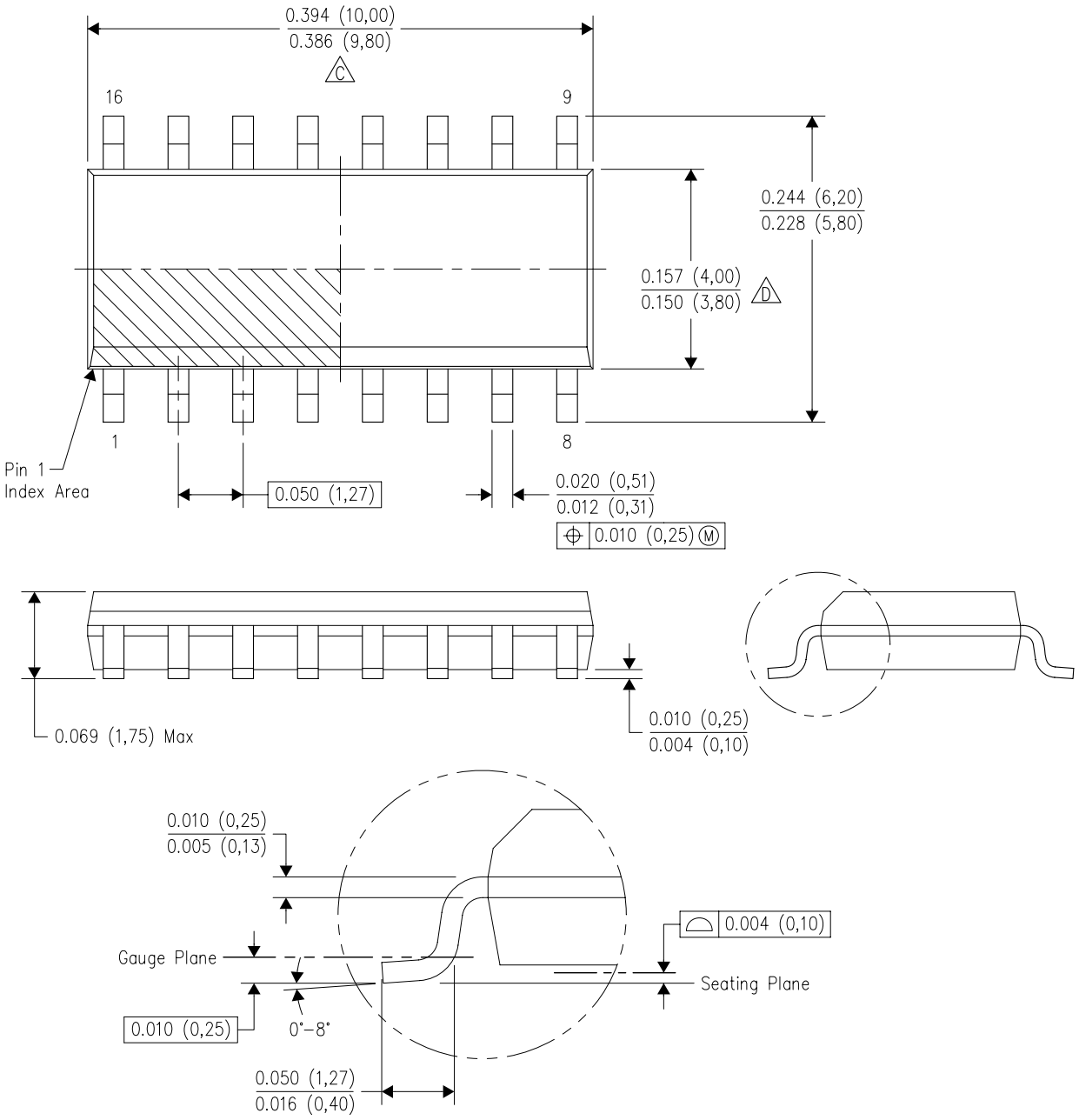
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF CD74HC40103-Q1 :
- Catalog: CD74HC40103
- Enhanced Product: CD74HC40103-EP
- Military: CD54HC40103

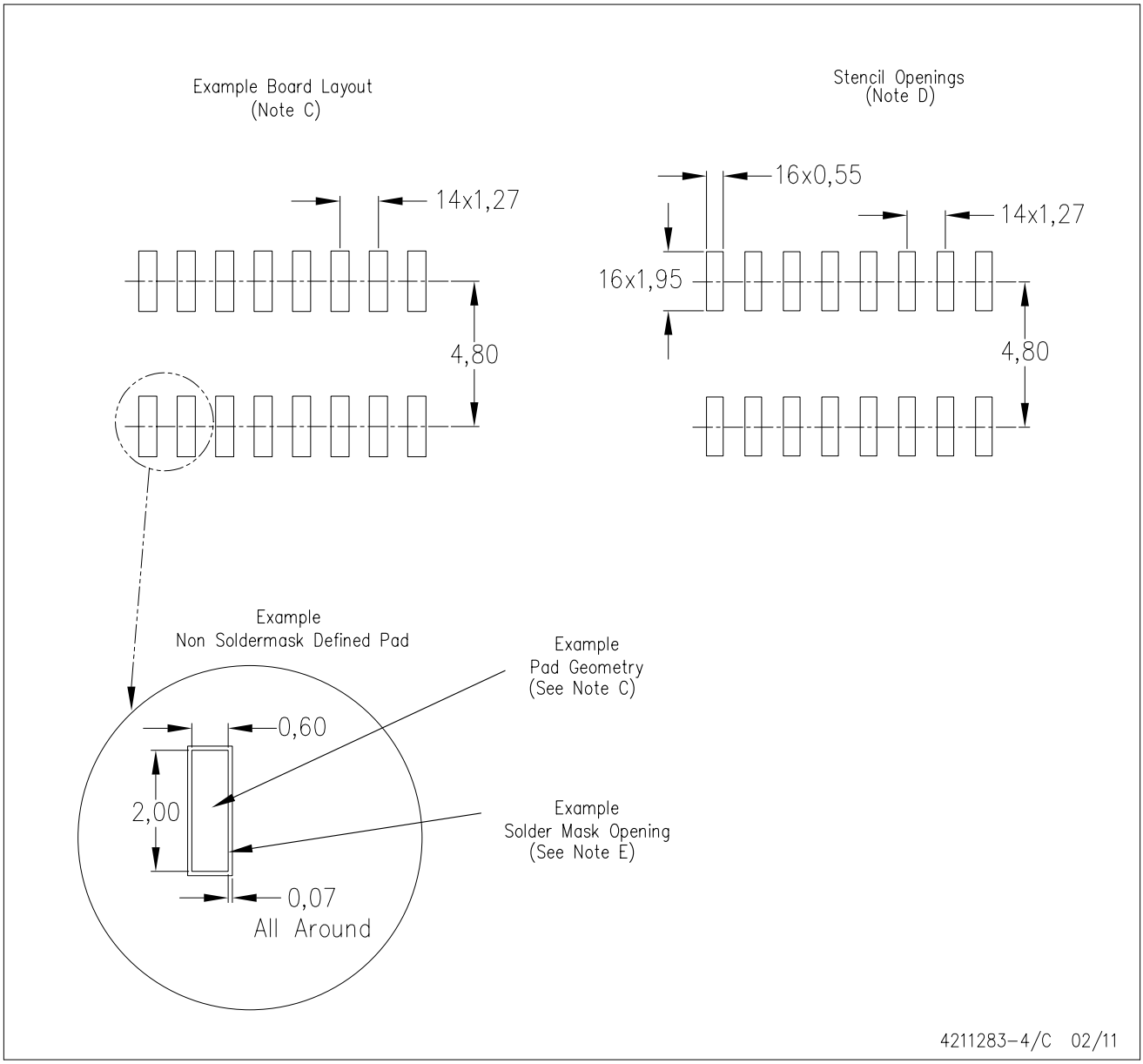
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265