Vertical clock driver for CCD imagers

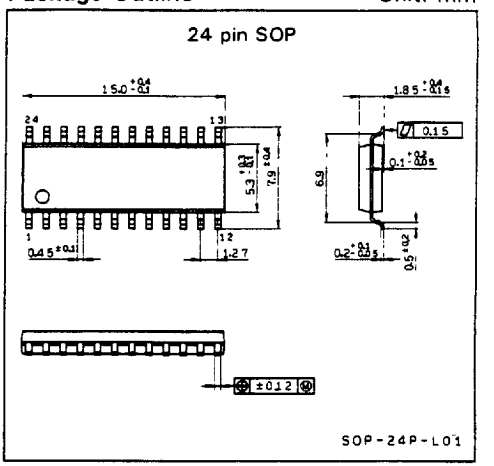
Description

The CXA1065M is a bipolar IC developed to drive the vertical shift register of CCD imagers (ICX022 etc.).

It is composed of seven drivers that can drive large capacitors with wide voltage amplitude. A suppressing function of coupling between phases reduces blooming and smear to make this IC ideal for vertical clock driving of CCD imaging devices.

Package Outline

Unit: mm



Features

- Almost all functions required for vertical clock driving of CCD imager are provided.
- Negative voltage source is not needed.
- Suppressing function of coupling between phases.
- Wide output amplitude — Output voltage amplitude is almost equal to supply voltage.
- Wide operating voltage range −5.5 to +25 V
- Low power consumption with the built-in power-saving circuit — 116 mW Typ. when the ICX022 equivalent circuit load is driven.

Structure

Silicon monolithic IC

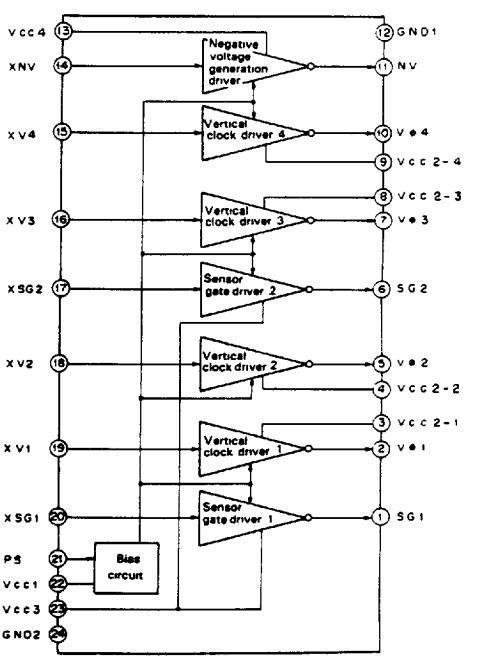
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{cc1}	6	V
	$V_{cc2\text{-}1}$	27	V
	$V_{cc2\text{-}2}$	27	V
	$V_{cc2\text{-}3}$	27	V
	$V_{cc2\text{-}4}$	27	V
	V_{cc3}	27	V
	V_{cc4}	27	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	560	mW

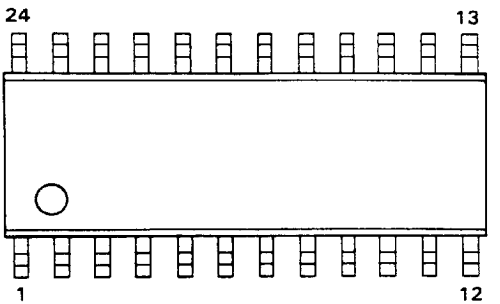
Recommended Operating Conditions

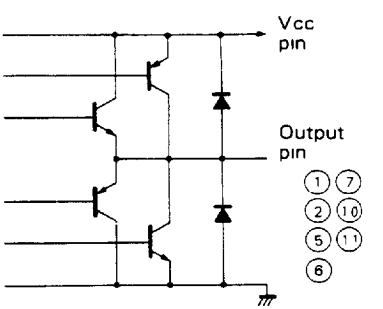
V_{cc1}	4.5 to 5.5	V
$V_{cc2\text{-}1}$	5.5 to 25	V
$V_{cc2\text{-}2}$	5.5 to 25	V
$V_{cc2\text{-}3}$	5.5 to 25	V
$V_{cc2\text{-}4}$	5.5 to 25	V
V_{cc3}	5.5 to 25	V
V_{cc4}	5.5 to 25	V

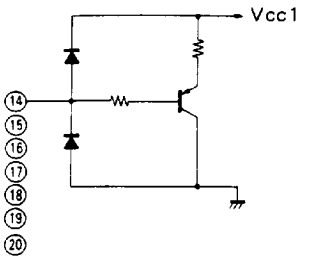
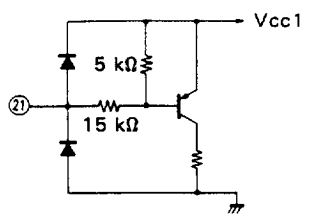
Block Diagram



Pin Configuration (Top View) and Description



No	Symbol	Description		Equivalent circuit
Function of each driver is inverter Truth table: Input L → Output H; Input H → Output L				
1	SG1	Sensor gate driver 1	Output pins	
2	Vφ1	Vertical clock driver 1		
5	Vφ2	Vertical clock drivr 2		
6	SG2	Sensor gate driver 2		
7	Vφ3	Vertical clock driver 3		
10	Vφ4	Vertical clock driver 4		
11	NV	Negative voltage generation driver		
3	Vcc2-1	Vertical clock driver 1	Vcc pins	
4	Vcc2-2	Vertical clock driver 2		
8	Vcc2-3	Vertical clock driver 3		
9	Vcc2-4	Vertical clock driver 4		
13	Vcc4	Negative voltage generation driver		
23	Vcc3	Sensor gate driver 1, 2		
12	GND1	GND		
24	GND2			

No.	Symbol	Description		Equivalent circuit
14	XNV	Negative voltage generation driver	Input pin	
15	XV4	Vertical clock driver 4		
16	XV3	Vertical clock driver 3		
17	XSG2	Sensor gate driver 2		
18	XV2	Vertical clock driver 2		
19	XV1	Vertical clock driver 1		
20	XSG1	Sensor gate driver 1		
21	PS	Input pin for the power-saving signal (For the power-saving function, refer to the Description of Functions.)		
22	Vcc1	Power supply of the bias circuit.		

Electrical Characteristics

DC characteristics

Ta = 25°C

V_{CC1} = 5V, $V_{CC2\text{-}1}$ = 12V, $V_{CC2\text{-}2}$ = 12V, $V_{CC2\text{-}3}$ = 12V, $V_{CC2\text{-}4}$ = 12V, V_{CC3} = 12V, V_{CC4} = 12V

With outputs open

Parameter			Symbol	Input condition (Blank 0V, H 5V)								Min	Typ	Max	Unit
				PS	XV1	XV2	XV3	XV4	XSG1	XSG2	XNV				
Input current into PS pin		Input current low level	I_{ILPS}									−500	−270		μA
		Input current high level	I_{IHPS}	H									0 03	15	μA
Input current into 7 drivers	Input current low level	XV1	I_{ILXV1}									−15	−2 5		μA
		XV2	I_{ILXV2}												
		XV3	I_{ILXV3}	H											
		XV4	I_{ILXV4}	H											
		XSG1	I_{ILXSG1}	H											
		XSG2	I_{ILXSG2}	H											
		XNV	I_{ILXNV}												
	Input current high level	XV1	I_{IHXV1}		H								0.03	15	μA
		XV2	I_{IHXV2}			H									
		XV3	I_{IHXV3}				H								
		XV4	I_{IHXV4}					H							
		XSG1	I_{IHXSG1}						H						
		XSG2	I_{IHXSG2}							H					
		XNV	I_{IHXNV}								H				
Input voltage	Low level		V_{IL}											0 05	V
	High level		V_{IH}									4 95			V

Parameter		Symbol	Input condition (Blank 0V, H 5V)								Min	Typ.	Max.	Unit
			PS	XV1	XV2	XV3	XV4	XSG1	XSG2	XNV				
DC supply cuttent of bias circuit at Vcc1	PS L All inputs. L	Icc1 LL									1.5	3 5	5 5	mA
	PS L All inputs H	Icc1 LH		H	H	H	H	H	H	H	0.5	1 7	3.0	mA
	PS H All inputs L	Icc1 HL	H								1 5	3 2	5.0	mA
	PS. H All inputs H	Icc1 HH	H	H	H	H	H	H	H	H	0 5	1 3	2.5	mA
DC supply current of vertical clock driver 1 at Vcc2-1	PS. L XV1. L	Icc2 1 LL									0.5	2.0	3 0	mA
	PS L XV1 H	Icc2 1 LH		H										
	PS H XV1 L	Icc2 1 HL	H								0.1	0.5	1.0	mA
	PS H XV1 H	Icc2 1 HH	H	H							1 5	3.2	5.0	mA
DC supply current of vertical clock driver 2 at Vcc2-2	PS L XV2: L	Icc2 2 LL									0.5	2.0	3.0	mA
	PS. L XV2: H	Icc2 2 LH			H									
	PS· H XV2: L	Icc2-2 HL	H								0.1	0.5	1.0	mA
	PS. H XV2· H	Icc2-2 HH	H		H						1 5	3.2	5.0	mA
DC supply current of vertical clock driver 3 at Vcc2 3	PS: L XV3: L	Icc2-3 LL									0.5	2.0	3.0	mA
	PS: L XV3: H	Icc2-3 LH				H								
	PS: H XV3: L	Icc2 3 HL	H								1.5	3.2	5.0	mA
	PS: H XV3: H	Icc2-3 HH	H			H					0.1	0.5	1 0	mA
DC supply current of vertical clock driver 4 at Vcc2 4	PS: L XV4: L	Icc2-4 LL									0.5	2.0	3.0	mA
	PS. L XV4· H	Icc2-4 LH					H							
	PS: H XV4· L	Icc2-4 HL	H								1.5	3.2	5.0	mA
	PS: H XV4: H	Icc2-4 HH	H				H				0.1	0.5	1.0	mA
DC supply current of sensor gate drivers 1, 2 at Vcc3	PS. L XSG1, 2: L	Icc3 LL									1.0	4.0	6.0	mA
	PS: L XSG1, 2: H	Icc3 LH						H	H					
	PS: H XSG1, 2: L	Icc3 HL	H								3.0	6.4	10.0	mA
	PS: H XSG1, 2: H	Icc3 HH	H					H	H		0.1	0.7	1.4	mA
DC supply current of negative voltage generation driver at Vcc4	XNV· L	Icc4 L									0.5	2.0	3.0	mA
	XNV· H	Icc4 H								H				

Characteristics when CXA1065M drives the equivalent circuit of CCD imager, ICX022

Supply current

Ta = 25°C, V_{CC1} = 5V, V_{CC2} = 10.6V, V_{CC3} = 13.4V, V_{CC4} = 10.6V
The CXD1035B (timing generator) is used as the input signal source

Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
Supply current at V_{CC1}	I_{CC1}		0.5	1.9	3.0	mA
Supply current at V_{CC2}	I_{CC2}		3.0	7.1	8.5	mA
Supply current at V_{CC3}	I_{CC3}		0.2	0.8	1.5	mA
Supply current at V_{CC4}	I_{CC4}		0.5	2.0	3.0	mA

Output waveform of each driver

Ta = 25°C, V_{CC1} = 5V, V_{CC2} = 10V, V_{CC3} = 13.4V, V_{CC4} = 10.6V
The CXD1035B (timing generator) is used as the input signal source.

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Output waveform of negative voltage generation driver	Falling edge voltage	V_{NVL}	Voltage at NV at 350ns after XNV rising edge	0.05	0.71	1.15	V
	Rising edge voltage	V_{NVH}	Voltage at NV at 350ns after XNV falling edge	9.45	10.13	10.55	V
	L level voltage	V_{NVLL}	Voltage at NV at 2100ns after rising edge of XNV	−0.08	−0.02	0.04	V
	H level voltage	V_{NVHH}	Voltage at NV at 2100ns after at XNV falling edge	10.52	10.58	10.64	V

Parameter			Symbol	Condition	Min	Typ	Max	Unit
Output waveforms of vertical clock drivers 1 2, 3 4	L level voltage	$V_{\phi 1}$	$V_{\phi 1L}$	Voltage at $V_{\phi 1}$ at 490ns after XV1 rising edge	0 06	0 32	0 80	V
		$V_{\phi 2}$	$V_{\phi 2L}$	Voltage at $V_{\phi 2}$ at 490ns after XV2 rising edge		0 35		
		$V_{\phi 3}$	$V_{\phi 3L}$	Voltage at $V_{\phi 3}$ at 490ns after XV3 rising edge		0 45		
		$V_{\phi 4}$	$V_{\phi 4L}$	Voltage at $V_{\phi 4}$ at 490ns after XV4 rising edge		0 47		
	H level voltage	$V_{\phi 1}$	$V_{\phi 1H}$	Voltage at $V_{\phi 1}$ at 1050ns after XV1 falling edge	9 91	9 98	10 06	V
		$V_{\phi 2}$	$V_{\phi 2H}$	Voltage at $V_{\phi 2}$ at 1050ns after XV2 falling edge				
		$V_{\phi 3}$	$V_{\phi 3H}$	Voltage at $V_{\phi 3}$ at 1050ns after XV3 falling edge				
		$V_{\phi 4}$	$V_{\phi 4H}$	Voltage at $V_{\phi 4}$ at 1050ns after XV4 falling edge				
	L coupling voltage	$V_{\phi 1}$	$V_{\phi 1LL}$	Voltage at $V_{\phi 1}$ at 280ns after XV2 rising edge	−0 58	−0 29	0 01	V
		$V_{\phi 2}$	$V_{\phi 2LL}$	Voltage at $V_{\phi 2}$ at 280ns after XV3 rising dege	−0 55	−0 34	−0 2	V
		$V_{\phi 3}$	$V_{\phi 3LL}$	Voltage at $V_{\phi 3}$ at 280ns after XV4 rising dege	−0.60	−0 37	−0 13	V
		$V_{\phi 4}$	$V_{\phi 4LL}$	Voltage at $V_{\phi 4}$ at 280ns after XV1 rising dege	−0.60	−0 42	−0 23	V
	H coupling voltage	$V_{\phi 1}$	$V_{\phi 1HH}$	Voltage at $V_{\phi 1}$ at 280ns after XV2 falling edge	10.16	10.46	10.62	V
		$V_{\phi 2}$	$V_{\phi 2HH}$	Voltage at $V_{\phi 2}$ at 280ns after XV3 falling edge		10.45		
		$V_{\phi 3}$	$V_{\phi 3HH}$	Voltage at $V_{\phi 3}$ at 280ns after XV4 falling edge		10 37		
		$V_{\phi 4}$	$V_{\phi 4HH}$	Voltage at $V_{\phi 4}$ at 280ns after XV1 falling edge		10.44		
	L coupling amplitude	$V_{\phi 1}$	$V_{\phi 1L\text{-}LL}$	$V_{\phi 1L} - V_{\phi 1LL}$	0.14	0.61	1.07	V
		$V_{\phi 2}$	$V_{\phi 2L\text{-}LL}$	$V_{\phi 2L} - V_{\phi 2LL}$	0.25	0.68	1.10	V
		$V_{\phi 3}$	$V_{\phi 3L\text{-}LL}$	$V_{\phi 3L} - V_{\phi 3LL}$	0.36	0.81	1.26	V
		$V_{\phi 4}$	$V_{\phi 4L\text{-}LL}$	$V_{\phi 4L} - V_{\phi 4LL}$	0.44	0.88	1.32	V
Output waveforms of sensor gate drivers 1 2	Falling edge voltage	SG1	V_{SG1L}	Voltage at SG1 at 350ns after XSG1 rising edge	0.14	0.84	1.46	V
		SG2	V_{SG2L}	Voltage at SG2 at 350ns after XSG2 rising edge		0.88		
	Rising edge voltage	SG1	V_{SG1H}	Voltage at SG1 at 350ns after XSG1 falling edge	11.94	12.74	13.26	V
		SG2	V_{SG2H}	Voltage at SG2 at 350ns after XSG2 falling edge		12.59		
	L level voltage	SG1	V_{SG1LL}	Voltage at SG1 at 1330ns after XSG1 rising edge	−0.11	0.00	0 11	V
		SG2	V_{SG2LL}	Voltage at SG2 at 1330ns after XSG2 rising edge				
	H level voltage	SG1	V_{SG1HH}	Voltage at SG1 at 1330ns after XSG1 falling edge	13.25	13 36	13.47	V
		SG2	V_{SG2HH}	Voltage at SG2 at 1130ns after XSG2 falling edge				

Electrical Characteristics Test Circuit 1

DC characteristics testing

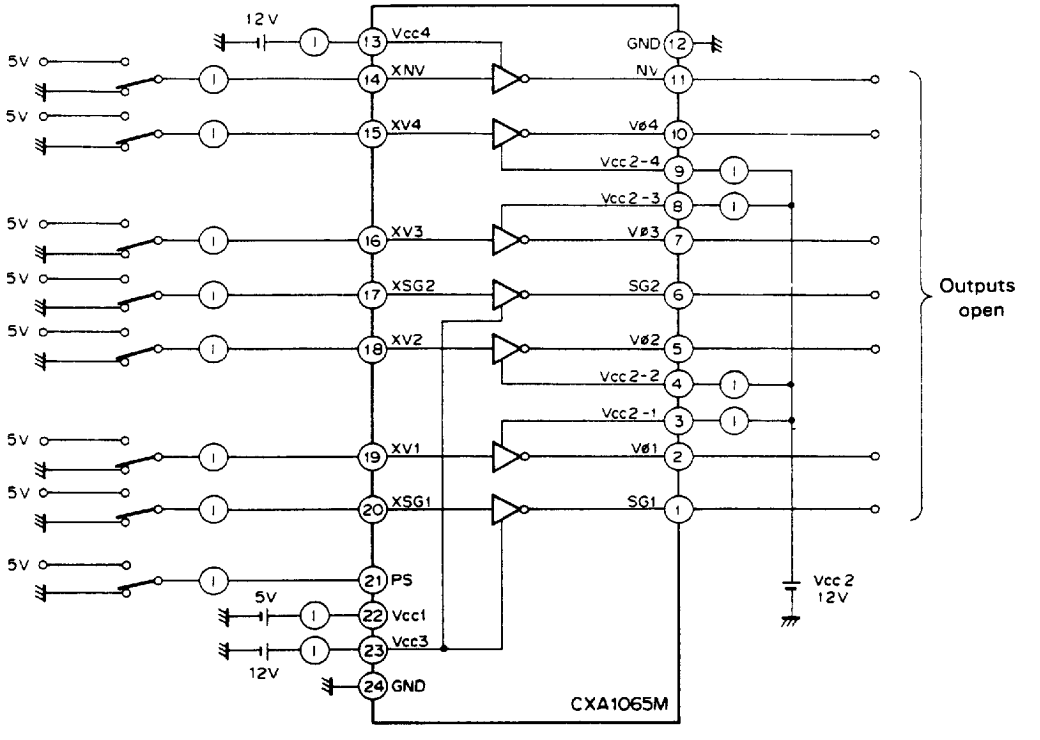
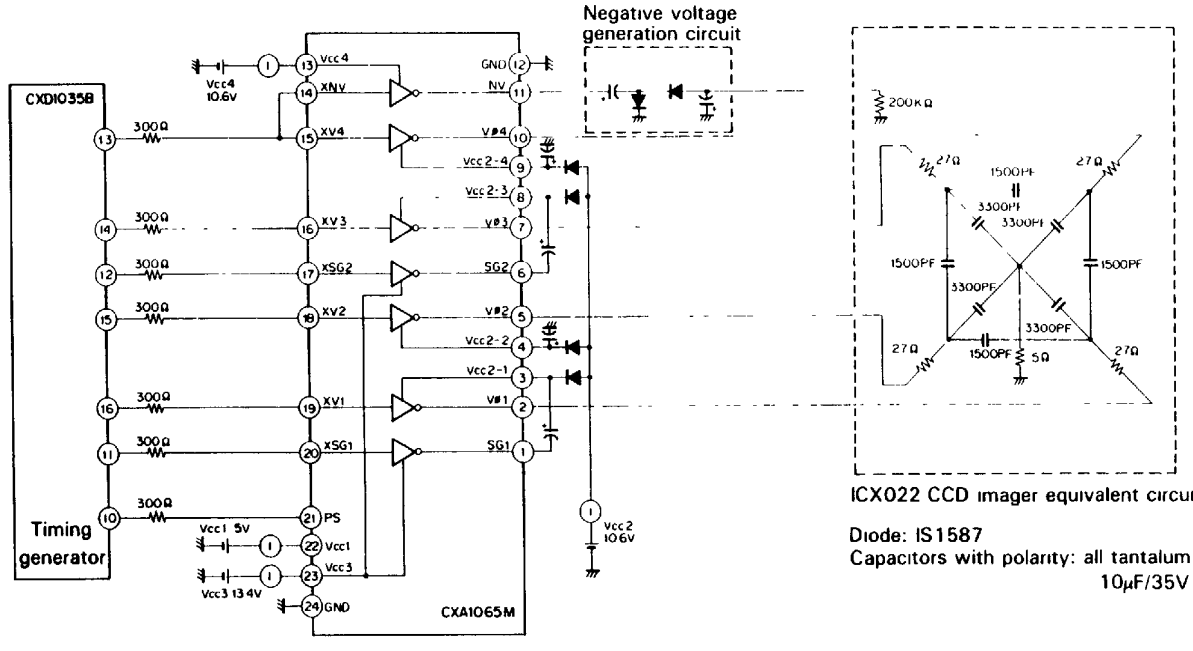


Fig. 1

Electrical Characteristics Test Circuit 2

Supply current testing when CXA1065M drives the equivalent circuit of CCD Imager, ICX022.



ICX022 CCD imager equivalent circuit

Diode: IS1587

Capacitors with polarity: all tantalum

10μF/35V

Fig. 2

SONY

Electrical Characteristics Test Circuit 3

Waveforms Testing

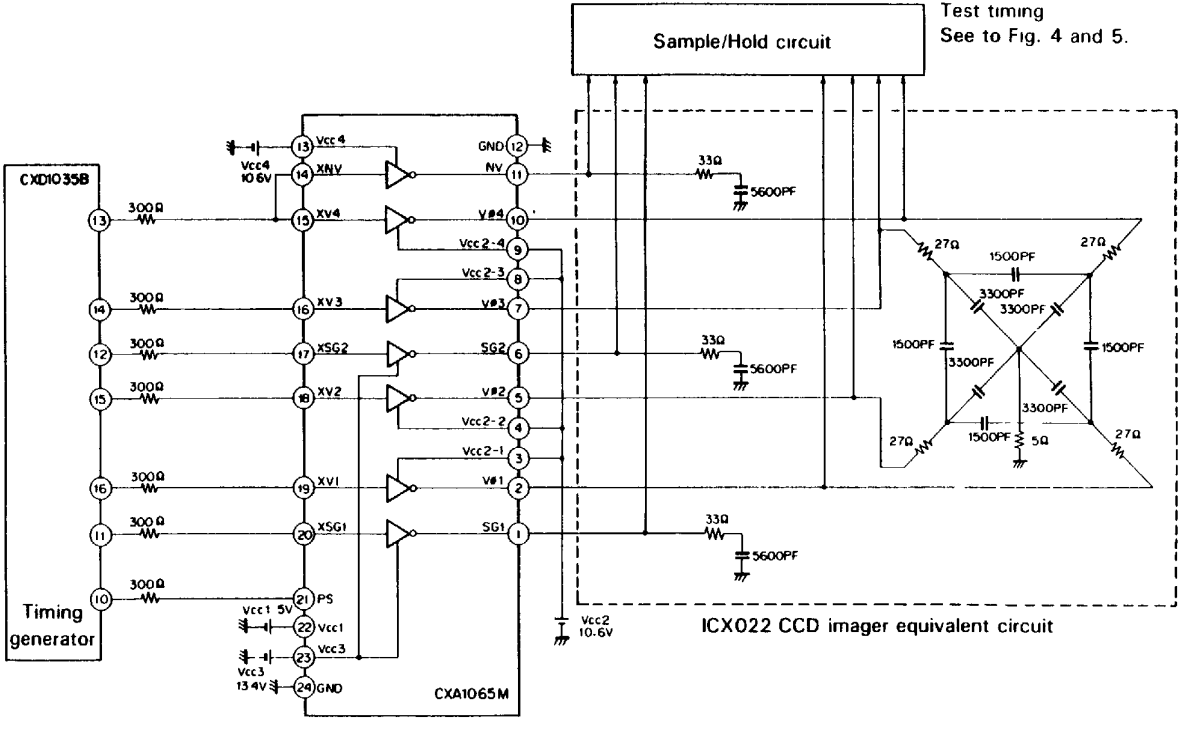


Fig. 3

Timing Chart

Waveform testing of 4-phase vertical clock drivers

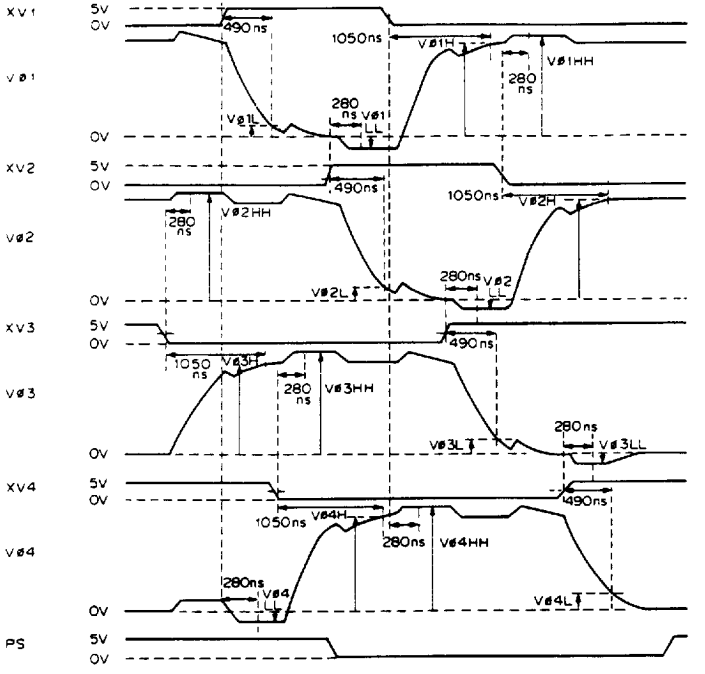


Fig. 4

Waveform testing of sensor gate drivers and negative voltage generation drivers

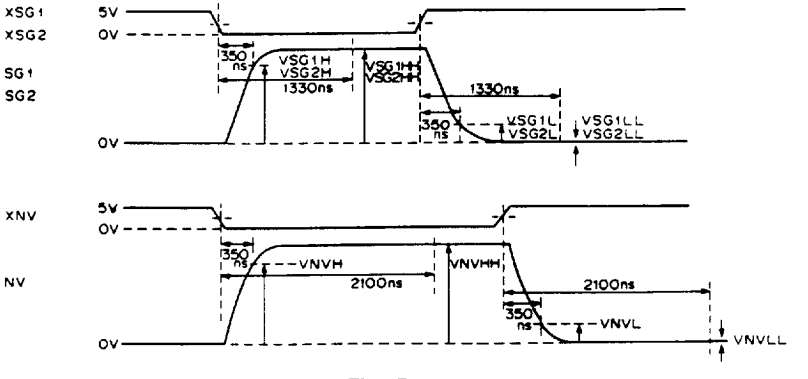


Fig. 5

Description of Operation

Description of functions and operation of the CXA1065M internal circuits

The CXA1065M is composed of a bias circuit and seven drivers.

Apply a voltage of 5 V to the Vcc1 terminal of the bias circuit. This circuit not only determines the DC bias for the seven drivers, but also has a power-saving function which reduces the power consumptions of four vertical clock drivers and two sensor gate drivers.

Directly connect the output of a CMOS IC to the input pins of the seven drivers. (Signal level, H: 5V, L: 0V) The output signal of each driver is inverted with low output impedance and wide amplitude. The output H level voltage of each driver is almost equal to the bias voltage of output stage and the L level output voltage is almost equal to the ground level. (See Fig. 6.)

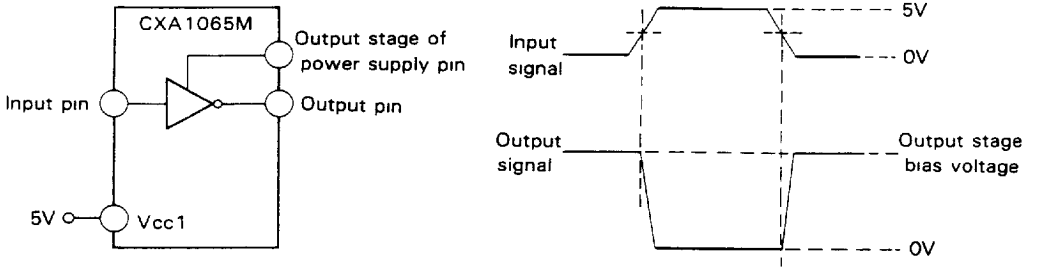


Fig. 6

The 4-phase clock drivers have a suppressing function of the coupling between phases when a CCD imager is driven. This function is suppress coupling voltage from other phases through the imager junction capacitances.

*Power-saving function

The CCD imaging device is equivalently, capacitive load.

Then a large driving ability is required only in the transient period of the output, and there is no need for such a large ability in other periods. The DC bias of the 4-phase clock drivers and 2 sensor gate drivers is changed by the input signal at the PS pin with appropriate timing, to reduce bias current when a large driving ability is not needed and achieve low power consumption.

Reference data: Typical values of supply current when the ICX022 equivalent circuit is driven (See Fig. 2)

	Using power-saving function	Not using power-saving function (PS pin fixed at 0V)
Supply current at Vcc1	1.9 mA	2.3 mA
Supply current at Vcc2	7.1 mA	12.7 mA
Supply current at Vcc3	0.8 mA	3.3 mA
Supply current at Vcc4	2.0 mA	2.0 mA

Description of Operation (CCD imager (ICX022) vertical clock driving system)

(For further information on the driving system of the CCD imager, refer to the specifications.)

Connect the output pin of the CXD1035B (CMOS IC) which is the CCD camera scanning timing generator, to the respective pins (Pin 14 through 21) of CXA1065M.

Clamp the output signal of the 4-phase vertical clock driver to the low level and input it to the vertical shift register transfer clock pin of the CCD imager.

Rectify the output signal of the negative voltage generation driver to obtain two reference voltage (negative voltages) for the low-level clamp. These two voltages are provided to compensate the clamping loss which may occur from the difference in duty between the 4-phase vertical clock drive signals. (When stable low-level clamp reference voltage supply is available with in the equipment, the rectifying circuit for the negative voltage is no more required.)

With the system shown in Fig. 8, the H level voltage of V clock level of the 4-phase vertical clock drive signals after the low-level clamp, is kept at 0 V even if Vcc4 is varied. This is because the circuit is designed to keep the low-level clamp reference voltage equal to the output voltage amplitude of the vertical clock drivers.

To obtain one of the readout clock pulse signals: The output signal of sensor gate driver 1 is used to modulate the output bias voltage of vertical clock driver 1.

To obtain the other signal: The output signal of sensor gate driver 2 used to modulate the output bias voltage of vertical clock driver 3.

If no source of high DC voltage is available in the equipment, the output signal for negative voltage generation driver can be utilized to generate the CCD imager substrate voltage. (See Fig. 7.)

Substrate voltage generation circuit

When maximum DC power supply in the equipment is +15V

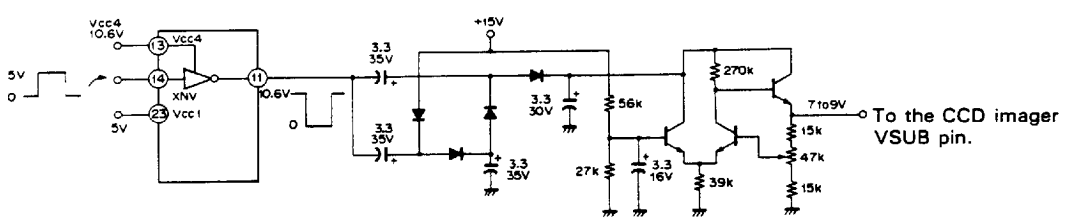
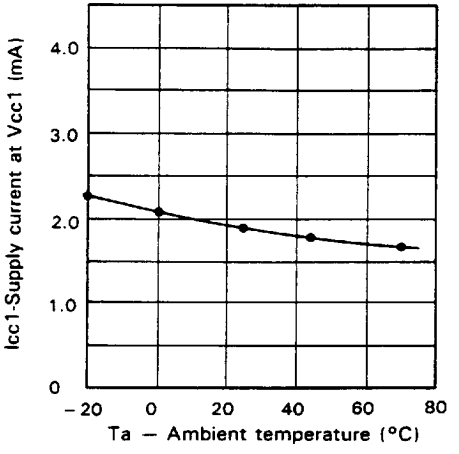


Fig. 7

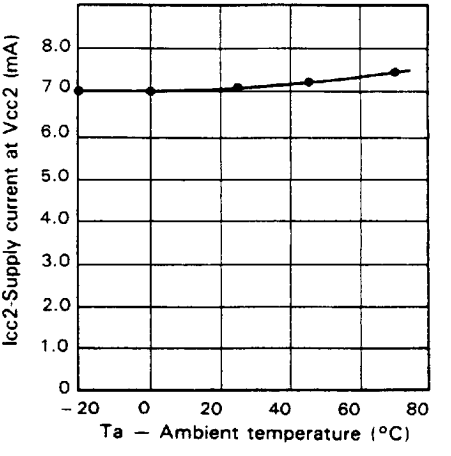
Performance Curves

Supply current when the ICX022 equivalent circuit is driven (Refer to the Test Circuit in Fig. 2).

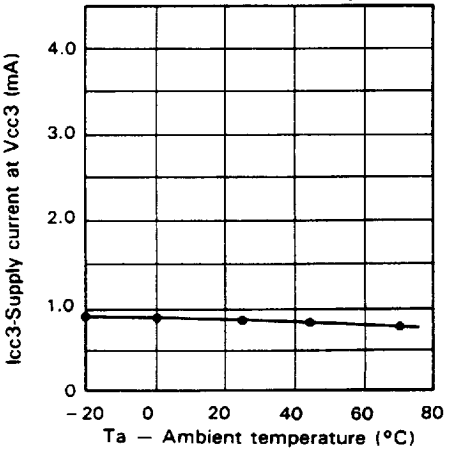
Supply current at Vcc1 vs. Ambient temperature



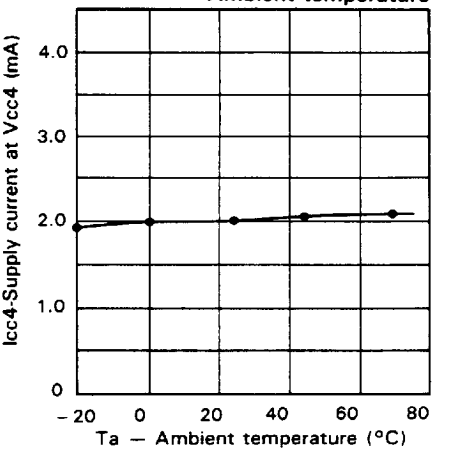
Supply current at Vcc2 vs. Ambient temperature



Supply current at Vcc3 vs. Ambient temperature



Supply current at Vcc4 vs. Ambient temperature



Notes on Application

- A large current flow through the power supply pin or the GND pin during the transient period of the output signal. Therefore, the GND pin must be grounded at a point within 1 cm from the pin. In addition, set the by-pass capacitor of the power supply pin within 1 cm from the pin.
- A conventional CMOS IC suffices as the input signal source of this IC (with an input current of Max. 500μA). To obtain the sharp CCD imager driving signal, minimize the length of the signal line.
- With an elongated signal line between the output pin of this IC and the input pin of the CCD imager, the inductance of the line may cause linking. To avoid this, shorten the line or insert a resistance in series to dump the linking.
- If the signal line between the output pin of this CMOS IC and input pin of this IC is too long, stray capacitance is large. In this case input signal of this IC is dull then sharp CCD imager driving signal is not obtained.