Programmable Delay Line/Duty Cycle Controller

Description

The CXB1119Q is an ultra high speed monolithic ECL Delay Line/Duty Cycle Controller IC.

Four binary inputs, S_0 to S_3, program the delay time from input D_{IN} to output Qd in 16 steps.

A pulse with plus (long) duty cycle is provided at output Qp, and a pulse with minus (short) duty cycle at output Qm. The duty cycle is also controlled by the input data.

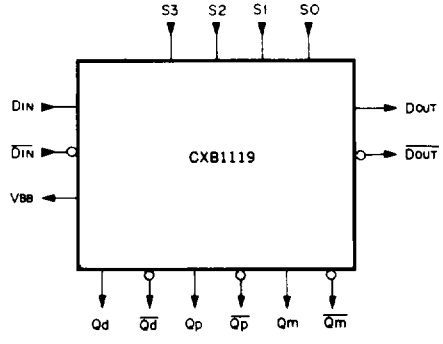
Features

- Programmable delay time: 870ps to 2240ps
- Programmable duty cycle
- Plus and minus duty cycle outputs
- Typical AC characteristics: T_{TLH}=185ps
  T_{THL}=175ps
- Differential data input and output
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

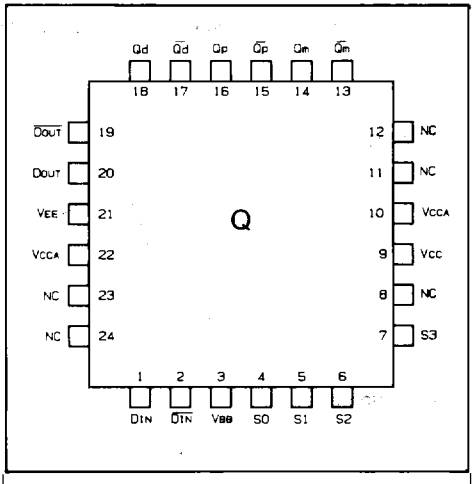
Pin Names

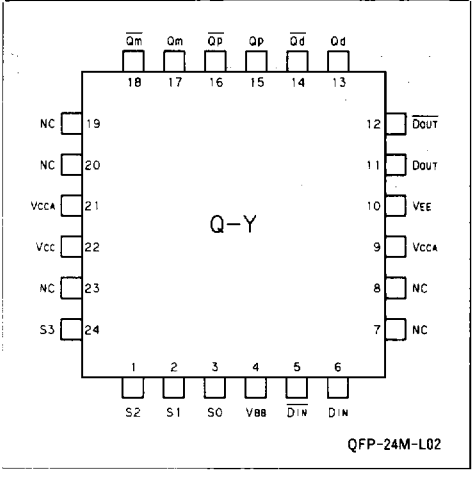
D_{IN}, $\overline{D_{IN}}$	Data inputs
S_n	Digital data input
D_{OUT}, $\overline{D_{OUT}}$	Buffered data outputs
Qd, $\overline{Qd}$	Delayed data outputs
Qp, $\overline{Qp}$	Plus duty cycle outputs
Qm, $\overline{Qm}$	Minus duty cycle outputs
V_{BB}	Reference voltage output
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment





QFP-24M-L02

DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−325	−239	−167	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

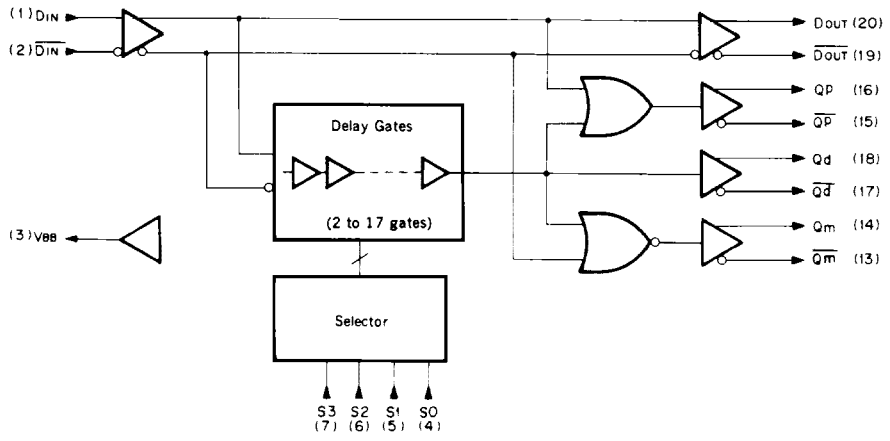
AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{dLH}	D_{IN}	Qd	S_0-S_3=LOW	700	870	1090	ps
	T_{dHL}				680	850	1065	
	T_{dLH}			S_0-S_3=HIGH	1570	2240	2800	
	T_{dHL}				1570	2240	2800	
	T_{OLH}		D_{OUT}		320	400	500	
	T_{OHL}				305	380	475	
	T_{pLH}		Qp	S_0-S_3=LOW	472	590	740	
	T_{mLH}		Qm	S_0-S_3=HIGH	444	555	695	
Rise time	T_{TLH}		Qd, D_{OUT} Qp, Qm	20% to 80%		185	230	
Fall time	T_{THL}					175	220	
Minimum pulse width	T_{pw}		Qm	S_0-S_3=LOW	285	305	330	
Jitter (σ)	T_{uc}		Qd	S_0-S_3=HIGH		5	12	

Note: AC test circuit; See page 4-3.

Block Diagram



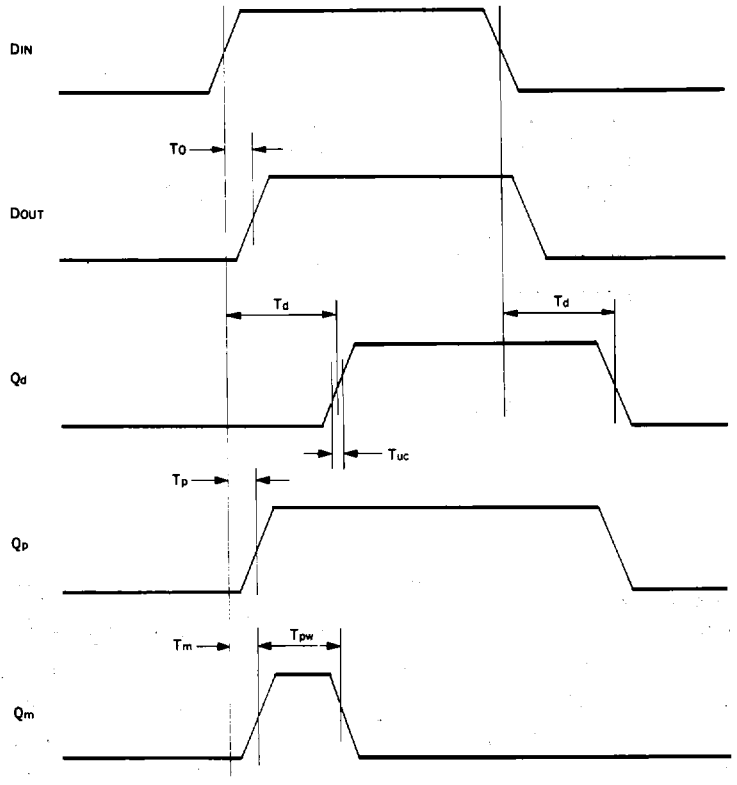
Truth Table

N	Input				Number of Gate	Output: Qd Typical Delay
	S_3	S_2	S_1	S_0		
0	L	L	L	L	1	870ps
1	L	L	L	H	2	945ps
2	L	L	H	L	3	1095ps
3	L	L	H	H	4	1155ps
4	L	H	L	L	5	1255ps
5	L	H	L	H	6	1305ps
6	L	H	H	L	7	1460ps
7	L	H	H	H	8	1520ps

N	Input				Number of Gate	Output: Qd Typical Delay
	S_3	S_2	S_1	S_0		
8	H	L	L	L	9	1645ps
9	H	L	L	H	10	1690ps
10	H	L	H	L	11	1805ps
11	H	L	H	H	12	1855ps
12	H	H	L	L	13	1990ps
13	H	H	L	H	14	2045ps
14	H	H	H	L	15	2210ps
15	H	H	H	H	16	2240ps

Typical delay time is calculated approximately by formula;
Td=(880+92N ps±70ps) ±25%

Timing Diagram



$Td \fallingdotseq (880 + 92N\ ps \pm 70ps) \pm 25\%$

$D_{OUT}(T) = D_{IN}(T - To)$
$Qd(T) = D_{IN}(T - Td)$
$Qp(T) = D_{OUT}(T) + \overline{Qd(T)}$
$Qm(T) = D_{OUT}(T) \cdot \overline{Qd(T)}$

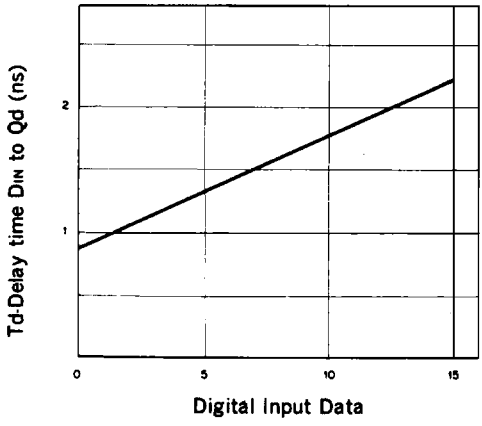


Figure1. Input Data vs Delay Time

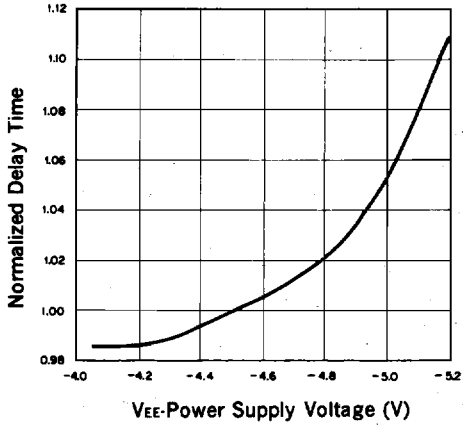


Figure2. Change in Delay Time vs. Change in Supply Voltage

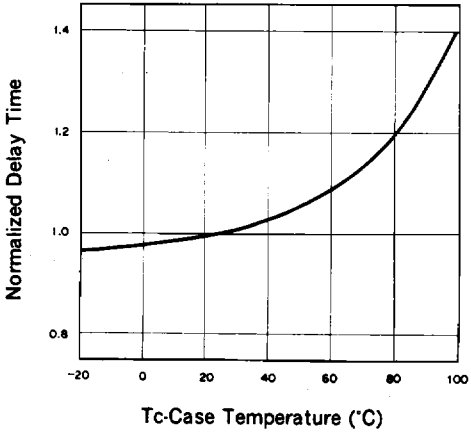


Figure3. Change in Delay Time vs. Change in Case Temperature

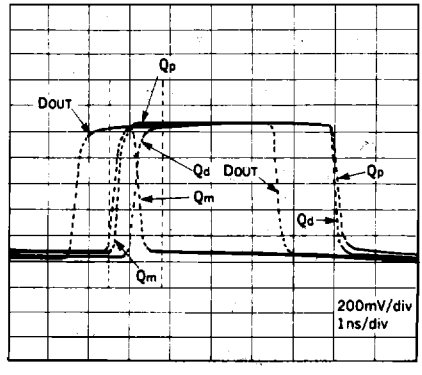


Figure4. Output Waveforms (N=0)