SONY CXD8068G

Preliminary

4:2:2 D1 Video Encoder

Outline

The CXD8068G is an encoder of 4:2:2 digital video parallel interface which is standardized by SMPTE and EBU. The chip is applicable to 10 bits as well as 8 bits.

Structure

- Bi-CMOS Gate Array

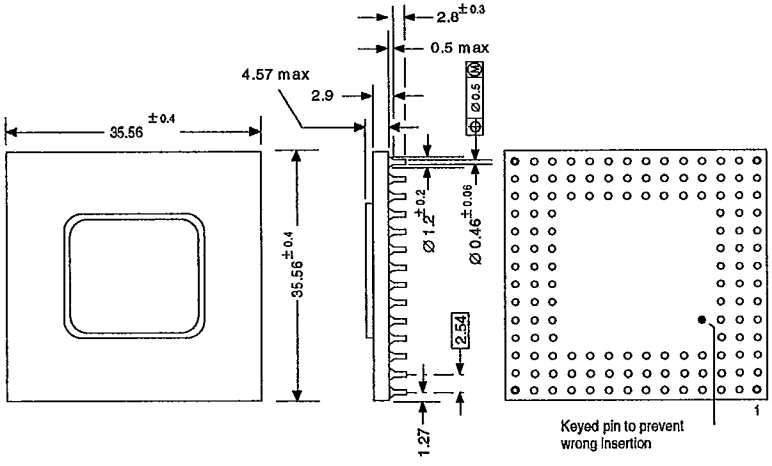
Functions

- 4:2:2 Video Parallel Digital Interface Encoder

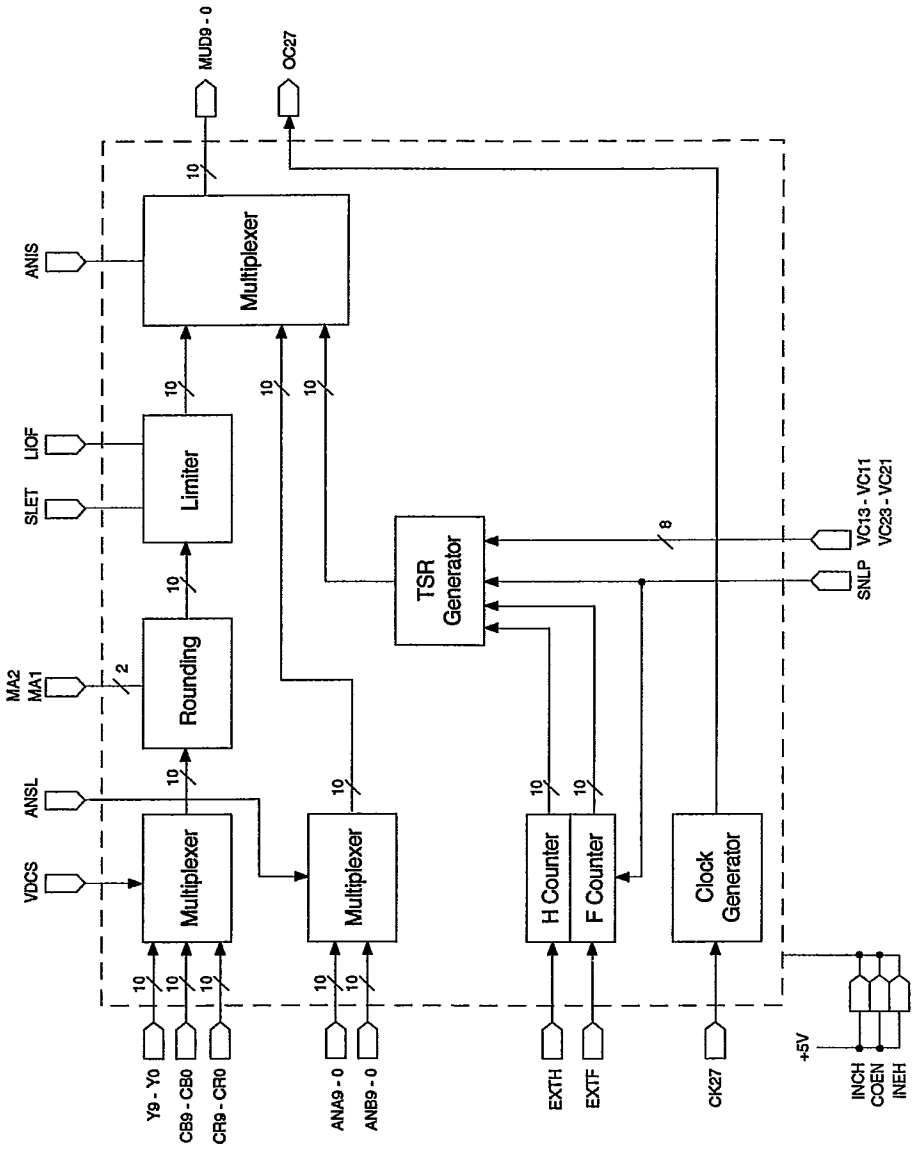
External Form

- 132pin PGA

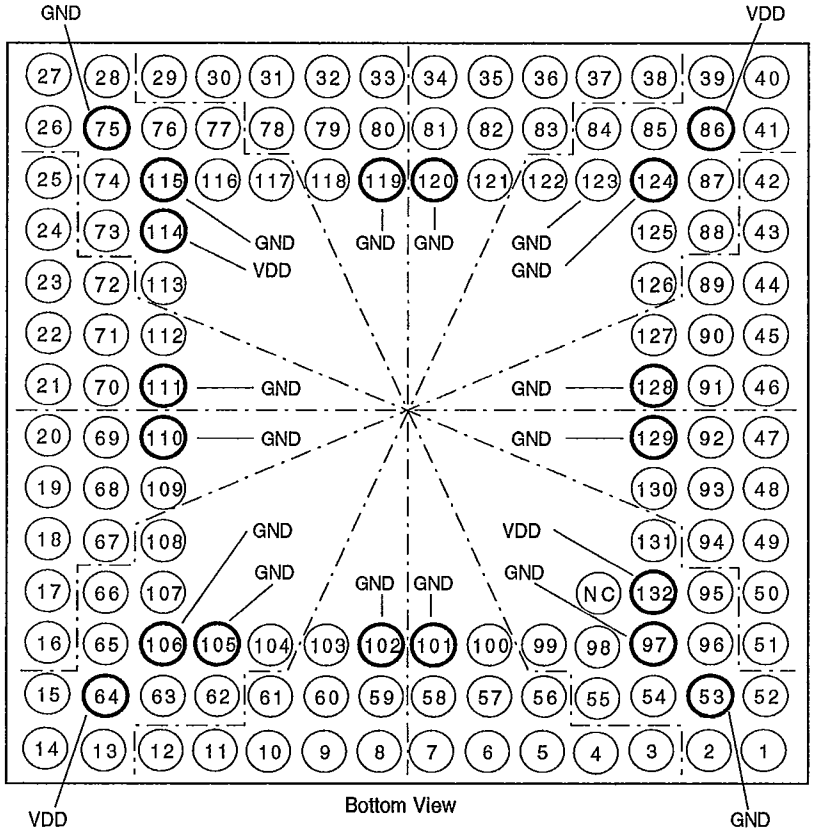
Package Outline



Block Diagram



Pin Configuration (Bottom View)



Pin Description

Pin Description	Pin No.	I/O	
Y9	87	I	(MSB)
Y8	42	I	
Y7	88	I	
Y6	43	I	Video Y Data
Y5	89	I	10bits: Y9~Y0
Y4	44	I	8bits: Y9~Y2
Y3	90	I	
Y2	45	I	
Y1	91	I	
Y0	46	I	(LSB)
CB9	92	I	(MSB)
CB8	47	I	
CB7	93	I	
CB6	48	I	Video CB Data (6.75MHz)
CB5	94	I	or CBCR multiplex Data (13.5MHz)
CB4	49	I	10bits: CB9~CB0
CB3	95	I	8bits: CB9~CB2
CB2	50	I	
CB1	96	I	
CB0	51	I	(LSB)
CR9	54	I	(MSB)
CR8	3	I	
CR7	55	I	
CR6	4	I	Video CR data (6.75MHz)
CR5	56	I	10bits: CR9~CR0
CR4	5	I	8bits: CR9~CR2
CR3	57	I	
CR2	6	I	
CR1	58	I	
CR0	7	I	(LSB)

Pin Description

Pin Description	Pin No.	I/O	
CK27	85	I	27MHz Clock
EXTH	79	I	Ref. H
EXTF	80	I	Ref. F
SLNP	37	I	525/625 switch
SLET	38	I	8bits/10bits switch
VDCS	39	I	Inut Video Croma Data Selection of multiplex and separate
LIOF	41	I	on/off of limiter
MA2	52	I	Rounding of the lower 2 bits when inputting with
MA1	2	I	10 bits and outputting with 8 bits.
VC13	26	I	
VC12	25	I	525/60 V-Blanking Control Field 1
VC11	24	I	
VC10	23	I	
VC23	22	I	
VC22	71	I	525/60 V-Blanking Control Field 2
VC21	21	I	
VC20	70	I	
TUB1	31	I	
TUB2	32	I	
TUS	33	I	Set to "Low" when using IC
TUC1	34	I	
TUC2	35	I	
ANA9	59	I	(MSB)
ANA8	8	I	
ANA7	60	I	Ancillary Data Input (13.5M 20 bits)
ANA6	9	I	or (27M 10bits) Input
ANA5	61	I	
ANA4	10	I	
ANA3	62	I	
ANA2	11	I	

Pin Description

Pin Description	Pin No.	I/O	
ANA1	63	I	
ANA0	12	I	(LSB)
ANB9	16	I	(MSB)
ANB8	65	I	
ANB7	17	I	
ANB6	66	I	Ancillary Data (13.5M 20bits) Input
ANB5	18	I	
ANB4	67	I	
ANB3	19	I	
ANB2	68	I	
ANB1	20	I	
ANB0	69	I	(LSB)
ANIS	15	I	Signal for the interval to input ANC data
ANSL	13	I	ANC Data Input 27M 10bits/13.5M 20bits switch
INCH	36	I	
COEN	40	I	
INEH	81	I	Set to "high" when using IC
LDAT	28	I	
TSCK	29	I	Test Pin
TSLD	30	I	Set to "high" (with pull up resistance)
TSLF	76	I	
TSST	77	I	
TSRT	78	I	

Pin Description

Pin Description	Pin No.	I/O	
CM9	117	O	(MSB)
CM8	118	O	
CM7	82	O	
CM6	121	O	
CM5	83	O	H. F. Counter Output
CM4	122	O	
CM3	84	O	
CM2	125	O	
CM1	126	O	
CM0	127	O	(LSB)
MUD9	74	O	(MSB)
MUD8	73	O	
MUD7	72	O	
MUD6	113	O	
MUD5	112	O	Multiplexer Data Output
MUD4	109	O	
MUD3	108	O	
MUD2	107	O	
MUD1	104	O	
MUD0	103	O	(LSB)
OC27	116	O	27MHz clock
OC13	131	O	13.5MHZ clock
OC6	98	O	6.7MHz clock
MFP	130	O	Position of Multiplexed F counter value
ANEH	100	O	"High" in between EAV and SAV.
ANEV	99	O	"High" in the digital active line of V-Blanking.

Electrical Characteristics

(Absolute Maximum Rating) (Ta=25°C)

Item	Symbol	Maximum Rating	Unit
Power voltage	V_{DD}	-0.5 ~ +7.0	V
Input voltage	V_S	-0.5 ~ +7.0	V
Output voltage	V_O	-0.5 ~ +5.5	V
Storage temperature	T_{st9}	-65 ~ +150	°C

(Recommended Operation Rating)

Item	Symbol	Min.	Max.	Unit
Power voltage	V_{DD}	4.5	5.5	V
High level input voltage	V_{IM}	2.0	V_{DD}	V
Low level input voltage	V_{IL}	0	0.8	V
High level output current	I_{OM}	-1	--	mA
Low level output current	I_{OL}	--	12	mA
Temperature	T_a	0	85	°C

(DC Characteristic Specification (Standard))

Item	Symbol	Condition	Min.	Typ.	Max	Unit
Input clamp voltage	V_{IC}	V_{DD}=4.5V, I_{IL}=-18mA	-1.5	-0.8	--	V
High level output voltage	V_{OH}	V_{DD}=4.5V, I_{OH}=-1mA	2.5	3.4	--	V
Low level output voltage	V_{OL}	V_{DD}=4.5V, I_{OL}=24mA	--	0.3	0.5	V
High level input current	I_{IH}	V_{DD}=5.5V, V_I=2.7V (Note)	--	--	+20	mA
Low level input current	I_{IL}	V_{DD}=5.5V, V_I=0.4V (Note)	-200	--	+20	mA
Output short current	I_{OS}	V_{DD}=5.5V, V_O=0V	-100	-40	-25	MA
High impedance output leak	I_{OZ}	V_{DD}=5.5V, V_{OH}=2.7V, V_{OL}=0.4V	-20	--	20	A
Input Thrcsh hold voltage	V_{TH}		--	1.5	--	V
Power current	I_{DD}			100	140	mA

Note: Exclude the input with pull up.

(In/output capacity characteristics)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input terminal	C_{IN}	V_{DD} = V_I = 0V			10	PF
Output terminal	C_{OUT}	f = 1MH			15	PF
In/output terminal	$C_{I/O}$				20	PF

Setting of Encoder

Pin Description		High	Low
SLNP	525/625 Switch	525/60	625/50
SLET	8 bits/10 bits (out put) Switch	10 bits	8 bits
VDCS	Input Croma Data Multiplex/Separate	Multiplex CB, CR (13.5MHz)	Separate CB, CR (6.75MHz)
LIOF	Limiter on/off	on	off
ANSL	ANC Data Input 27M 10 bits/13.5M 20 bits	13.5M 20 bits	27M 10 bits
ANIS	Input Video Data/ANC Data	Ancillary Data Output	Input Video Data Output

Rounding method of the lower 2bits.

When inputting with 10bits and outputting with 8bits.

Pin Description		Rounding method
MA 2	MA 1	
0	0	Round of the closest
0	1	Round up
1	0	Truncate
1	1	Through

V blanking falling line in 525/60 (refer to fig.6)

First Field

Pin Name				Line No.
VC13	VC12	VC11	VC10	
0	0	0	0	10
0	0	0	1	11
		}		}
1	0	0	1	19
1	0	1	0	20

Second Field

Pin Name				Line No.
VC23	VC22	VC21	VC20	
0	0	0	0	272
0	0	0	1	273
		}		}
1	0	0	1	281
1	0	1	0	282

Operation Procedure

1. Relation between input signal Y, CB, CR and EXTH

Input signals are Y signal sampled with 13.5MHz and CB, CR signal sampled with 6.75MHz or Multiplexed signal of CB, CR.

As for the timing relation between input signal Y, CB, CR and ext. H, please refer to the fig.1. (H counter inside IC is initialized by the falling edge of exth.)

2. Timing of EXTF Input (refer to Fig. 6)

EXTF falls at the line 4 in 525/60 and at the line 1 in 625/50. (F counter inside IC is initialized by the falling edge of EXTF).

3. Rounding and limitier

1) Rounding

It is needed to round the lower 2 bits of the input signal when being input with 10 bits and output with 8 bits since this IC is applicable to 10 bits in/outputs as well as 8 bits. There are 4 kinds of rounding methods, which are round to the closest, round up, truncate and through for 10 bits output. (Select with MA2, MA1).

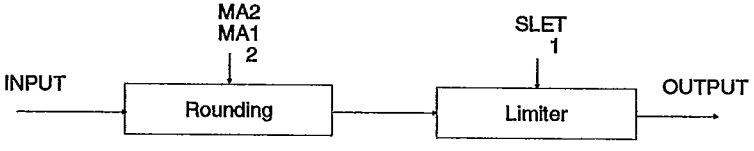
2) Limiter

Input signal is converted with limiter as follows. 8 bits and 10 bits can be selected with "SLET".

8 bit output)	Input	Output
	FF	FE
	00	01

10 bit output)	Input	Output
	3FF, 3FE, 3FD, DFC	3FB
	000, 001, 002, 003	004

As in/outputs through this IC, the following four patterns are possible.



8 bits (INPUT) 8 bits (OUTPUT)	TRUNCATE	8 bits
8 bits (INPUT) 10 bits (OUTOUT)	TRUNCATE	10 bits
10 bits (INPUT) 8 bits (OUTPUT)	*round to the closest * round up * truncate	8 bits
10 bits (INPUT) 10 bits (OUTPUT)	THROUGH	10 bits

4. Relation between ancillary data and the signal for input interval (ANIS)

It is possible to select (ANSL) 13.5MHz 20 bits (ANA9~0, ANB9~0) and 27M 10 bits (ANA9~0) inputs as ancillary data. ANC data can be input to any points if ANIS is high in the interval to input data.

1) 13.5M 20 bits input

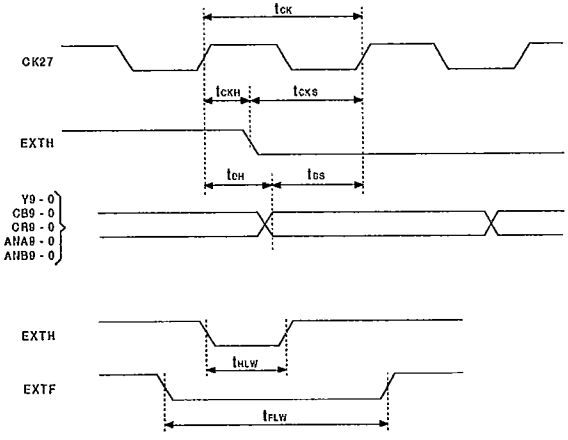
There are four cases according to the 13.5MHz clock output from IC, the signal for the interval to input ANC data (ANIS) and byte number of input data. (Refer to Fig. 2)

2) 27M 10 bits Input

Relation between the input data and the signal for the interval to input ANC data is shown as fig.3.

5. Output of Counter Value (CM9~CM0) (Fig. 4)

There is an H counter and F counter inside the IC. The H counter counts from 0 up to 857 in 525/60 and from 0 up to 863 in 625/50. F counter counts from 0 up to 524 in 525/60 and from 0 up to 624 in 625/50. This IC outputs multiplexed value of H counter and F counter. As mentioned in the above, H counter counts from 0 up to 857 (525/60) and form 0 to 863 (625/50), and then value which H counter counts is output with 10 bits and when that output value is 720, value of F counter is output (CM9 CM0) and the position pulse, which outputs value of F counter, is also output at the same time (MFP).



AC Characteristic

Item	Symbol	Min.	Typ.	Unit
CK27 cycle time	t_{CK}	30	37	ns
EXTH hold time	t_{CKH}	2		ns
EXTH setup time	t_{CKS}	5		ns
Input data hold time	t_{DN}	2		ns
Input data setup time	t_{DS}	5		ns
EXTH low level width	t_{HLW}	40		ns
EXTF low level width	t_{FLW}	70		µs

Pin Name

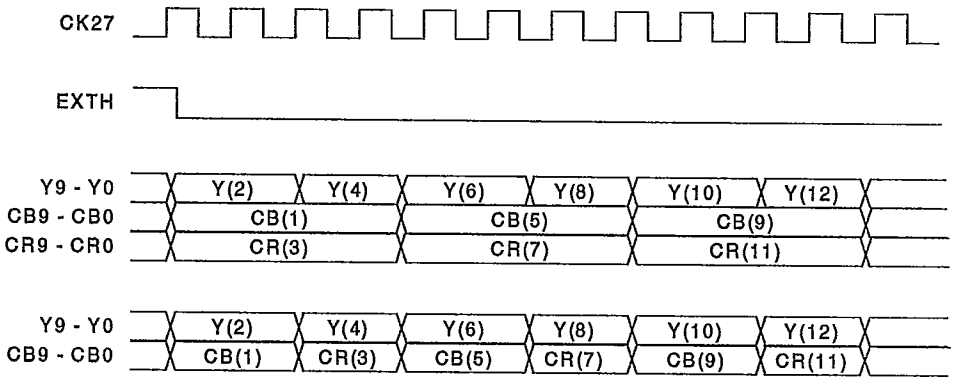


FIGURE 1

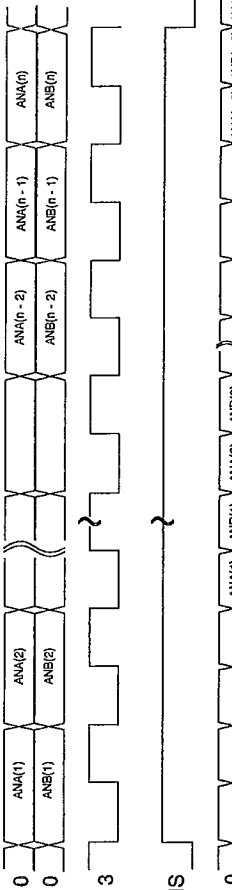


FIGURE 2

FIGURE 3

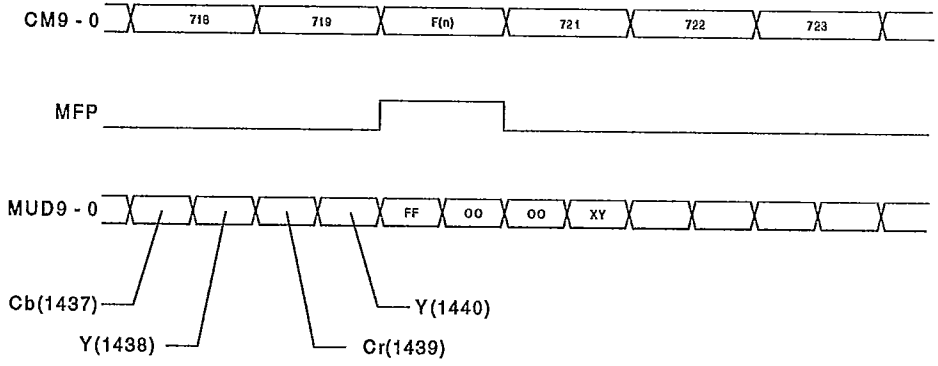
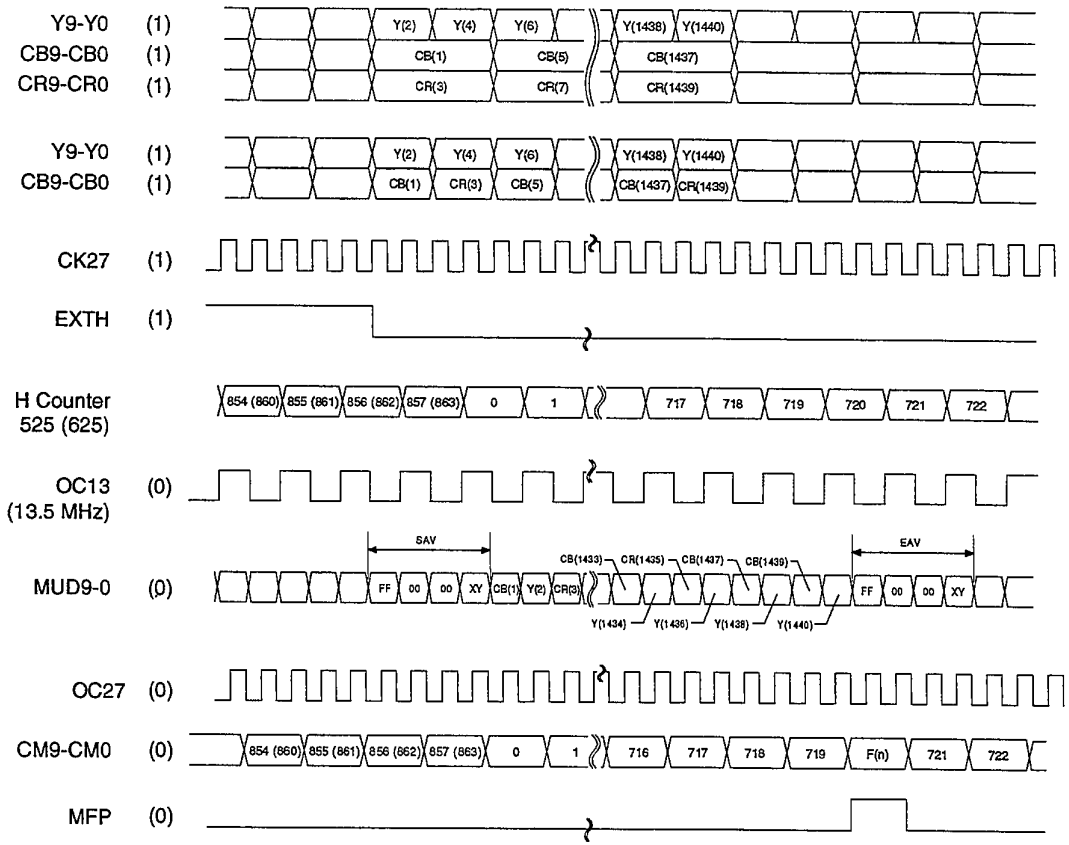

CM9 - 0
718
719
F(n)
721
722
723
MFP
MUD9 - 0
FF
00
00
XY
Cb(1437)
Y(1438)
Cr(1439)
Y(1440)

FIGURE 4



(1) = Input pin
(0) = Output pin

FIGURE 5

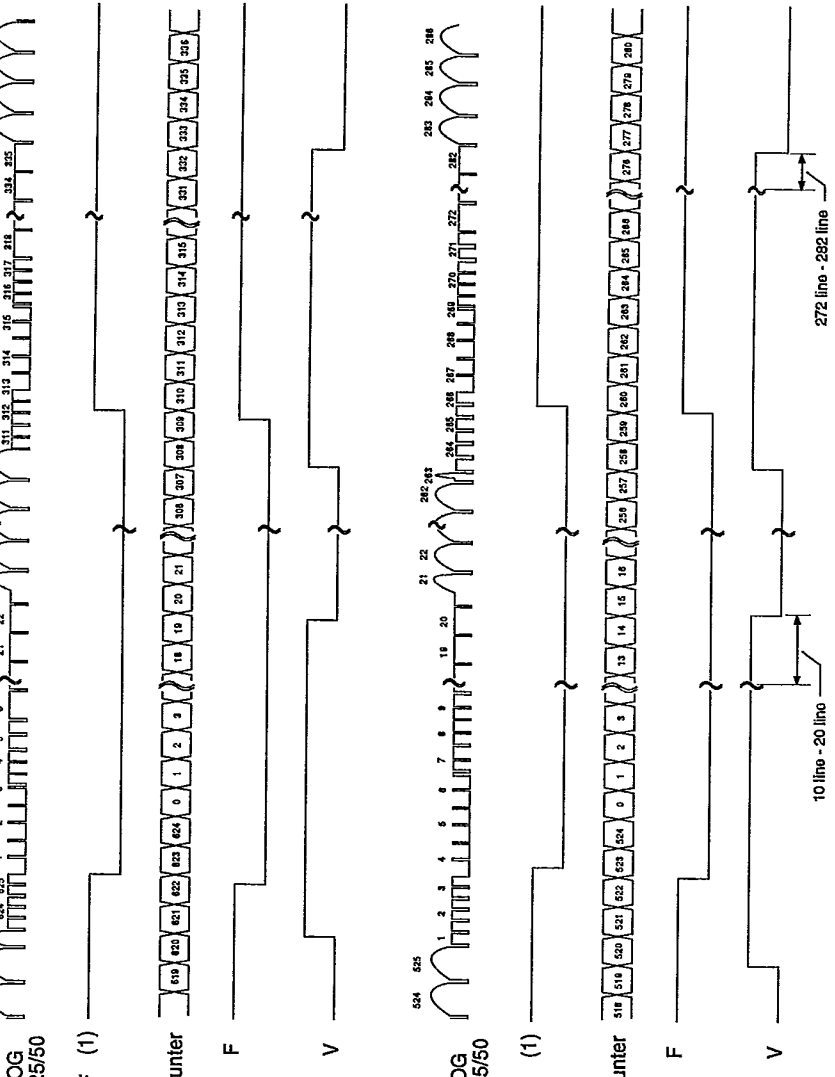

ANALOG 625/50
EXTF (1)
F Counter
F
V
10 line - 20 line
272 line - 282 line

FIGURE 6