SONY

CXK48324Q/R

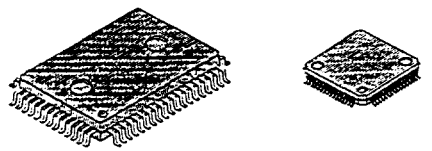
2.4-Mbit 3-port Video Signal Field Memory

Description

The CXK48324Q/R is a 3-port field memory compatible with both NTSC and PAL standard video signals and is capable of storing one 8-bit field picture with a single chip. The CXK48324Q/R is suitable as a memory for improving the picture quality, such as NR+TBC, and NR+double speed, etc. The functions are compatible with CXK1206M (1.2-Mbit field memory)

CXK48324Q
64 pin QFP (Plastic)

CXK48324R
80 pin VQFP (Plastic)



Features

- Three asynchronous ports: one Write port and two Read ports.
- The most suited structure for video signal processing of 960 columns 306 rows 8 bits
- Both NTSC and PAL are compatible with 4 fsc. (Only NTSC is 8 fs-compatible for Read.)
- Both recursive mode/non-recursive mode are provided, enabling a variety of applications.
- Random access: column → by block unit (Write only)
  row → by line unit
- Transfer between I/O ports and the internal memories is automatically controlled internally.
- Power supply: +5V±10%.
- I/O level: TTL-compatible, low input capacitance.
- 293,760-bit refresh cycle/21ms.

Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	Vcc	−1.0 to +7.0	V
• Operating temperature	Topr	0 to +70	°C
• Storage temperature	Tstg	−55 to +125	°C
• Allowable power dissipation	PD	1.0	W (CXK48324Q)
		0.7	W (CXK48324R)

Recommended Operating Conditions (Ta=0 to +70°C, Vss=0V)

• Supply voltage	Vcc	4.5 to 5.5	V
• Supply voltage	Vss	0	V
• Input voltage "High" level	VIH	2.4 to Vcc+1	V
• Input voltage "Low" level	VVL	−0.5* to +0.8	V

* Minimum undershoot: −2.0V (20ns and below)

DC Characteristics

Power consumption during operation 150mW (typ.) (approximately 1.5 times that of CXK1206M)

AC Characteristics

Minimum clock cycle	Write clock (CKW) 50ns
	Read clock (CKR) 30ns
Maximum access time (from CKR)	25ns

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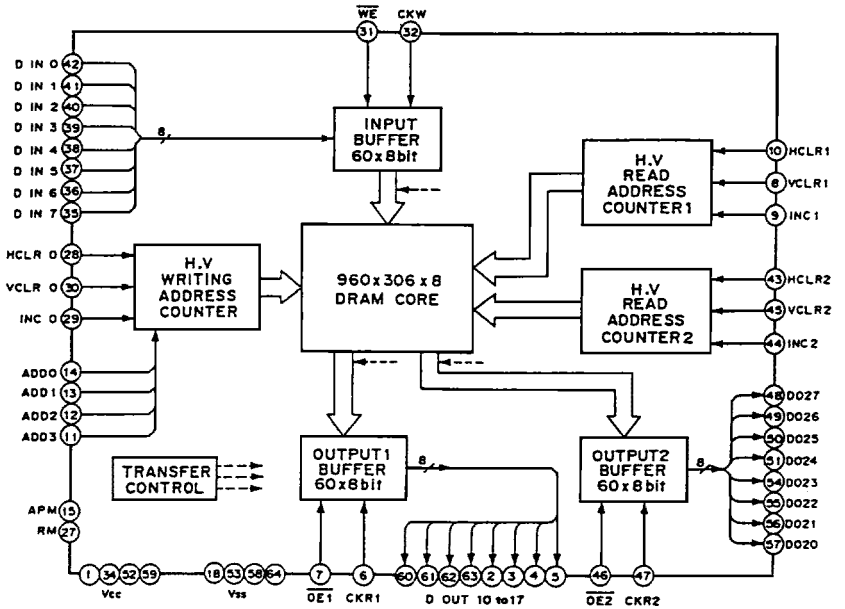
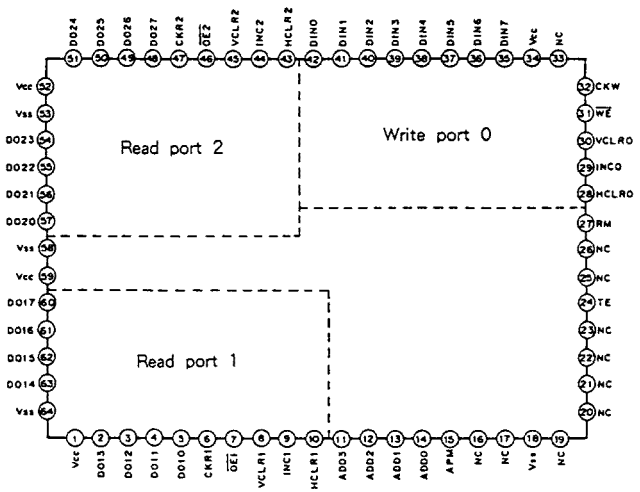
Block Diagram (QFP)

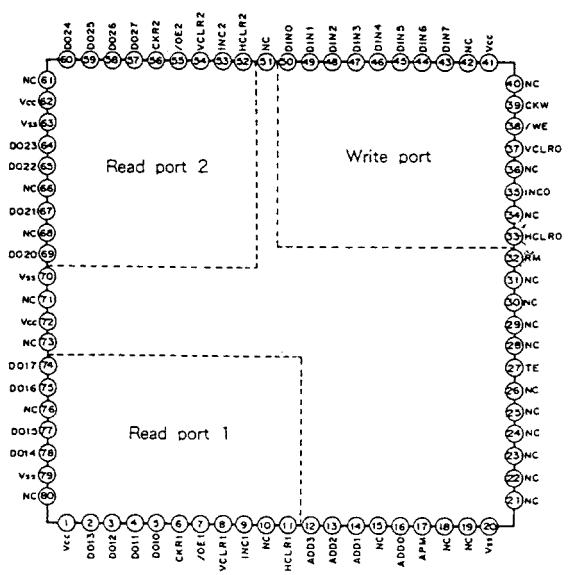


Pin Configuration (Top View)

(QFP)



(VQFP)



Pin Description

Pin No.		Symbol	I/O	Description
QFP	VQFP			
1	1	Vcc	——	Power supply (+5V)
2	2	DO13	O	Port 1 data output
3	3	DO12	O	Port 1 data output
4	4	DO11	O	Port 1 data output
5	5	DO10	O	Port 1 data output
6	6	CKR1	I	Port 1 shift signal
7	7	/OE1	I	Port 1 output enable
8	8	VCLR1	I	Port 1 vertical clear
9	9	INC1	I	Port 1 line increment
10	11	HCLR1	I	Port 1 horizontal clear
11	12	ADD3	I	Address 3 input
12	13	ADD2	I	Address 2 input
13	14	ADD1	I	Address 1 input
14	16	ADD0	I	Address 0 input
15	17	APM	I	Address preset mode enable
18	20	Vss	——	GND
24	27	TE	——	Test mode enable (normally fixed to Vss)
27	32	RM	I	Recursive mode enable
28	33	HCLR0	I	Port 0 horizontal clear
29	35	INC0	I	Port 0 line increment
30	37	VCLR0	I	Port 0 vertical clear
31	38	/WE	I	Port 0 Write enable
32	39	CKW	I	Port 0 shift signal
34	41	Vcc	——	Power supply (+5V)
35	43	DIN7	I	Port 0 data input
36	44	DIN6	I	Port 0 data input
37	45	DIN5	I	Port 0 data input
38	46	DIN4	I	Port 0 data input
39	47	DIN3	I	Port 0 data input
40	48	DIN2	I	Port 0 data input
41	49	DIN1	I	Port 0 data input
42	50	DIN0	I	Port 0 data input
43	52	HCLR2	I	Port 2 horizontal clear
44	53	INC2	I	Port 2 line increment
45	54	VCLR2	I	Port 2 vertical clear
46	55	/OE2	I	Port 2 output enable

Pin No.		Symbol	I/O	Description
QFP	VQFP			
47	56	CKR2	I	Port 2 shift signal
48	57	DO27	O	Port 2 data output
49	58	DO26	O	Port 2 data output
50	59	DO25	O	Port 2 data output
51	60	DO24	O	Port 2 data output
52	62	Vcc	—	Power supply (+5V)
53	63	Vss	—	GND
54	64	DO23	O	Port 2 data output
55	65	DO22	O	Port 2 data output
56	67	DO21	O	Port 2 data output
57	69	DO20	O	Port 2 data output
58	70	Vss	—	GND
59	72	Vcc	—	Power supply (+5V)
60	74	DO17	O	Port 1 data output
61	75	DO16	O	Port 1 data output
62	77	DO15	O	Port 1 data output
63	78	DO14	O	Port 1 data output
64	79	Vss	—	GND
—	—	NC	—	No Connection

RM

Depending on the status of this pin, the CXK48324Q/R operates in either of the two modes: the recursive mode during "High"-level setting, and the non-recursive mode during "Low"-level setting.

- Recursive mode: This mode permits sequential access to 960×306 memory cells from 0 to 293,759. Initialization is conducted by inputting to Pins VCLR0, VCLR1, and VCLR2. For Write, when "High"-level VCLR0 is latched by CKW, the serial data input is treated as the data input to Line 0/Block 0. For Read, 64 clocks after CKR1 and CKR2 latch on to "High"-level VCLR1 and VCLR2 respectively, the serial data output is output as Line 0/Block 0 data.
- Non-recursive mode: This mode treats 960×306 memory cells as a unit of 1 line/16 blocks (60 bits per block). It controls lines with VCLR0/VCLR1/VCLR2 and INC0/INC1/INC2, while controlling blocks with HCLR0/HCLR1/HCLR2. The difference from the recursive mode is that for Write, the serial data input at the moment when HCLR0 is latched by CKW is handled as the input data to Line 0/Block 0; while for Read, the serial data is output as Line 0/Block 0 output data from Read ports 1 and 2, 64 clocks after CKR1/CKR2 latches on to HCLR1/HCLR2.

APM

This pin is necessary for the address preset mode which presets the block address within one line of the Write port. The address preset mode is valid only when RM is set to "Low" level (non-recursive mode). If this pin is set at "High" level when HCLR0 is latched by CKW, one of 16 blocks will be selected by four bits, ADD0 to ADD3.

ADD0, ADD1, ADD2, and ADD3

In the non-recursive, address preset mode these pins select the horizontal block address.

- The four address lines select one of the 16 line blocks when activated by the APM pin.
- The address input during APM mode is effective during the period which $\overline{WE}$ is "High". $\overline{WE}$ must be "High" at the time HCLR0 is input and when $\overline{WE}$ returns "Low" CKW latches the signal.

CKW

The rising edge of this pin generates a signal which latches input data at Pins DIN0 to DIN7, to be sent to the shift register, and also a signal which latches the input at internal address pointer control pins (VCLR0, HCLR0, INC0). Because this signal is used as the basic signal for start control of the internal clock synchronizing logical circuit and the dynamic RAM, clock operation is necessary irrespective of whether Write operation is active or not.

VCLR0

This pin has different roles depending on whether Pin RM is at "High" level (recursive mode) or "Low" level (non-recursive mode).

The number of counts for VCLR0 is counted only when the state latched at every CKW is at "High" level following the recognition of a "Low" level. Continuation of "High" level is counted as "one".

This operation is valid if $\overline{WE}$ is High when VCLR0 is input until the point at which $\overline{WE}$ becomes "Low" and is latched by CKW.

In recursive mode: When CKW latches VCLR0 at "High" level, the serial write data input at that moment is taken in as * (0, 0) data. Among the data entered so far, data of less than one block unit (60 bits) are rejected.

* (0, 0) indicates Line 0/Block 0; thus, the number of lines and blocks upon control signal input will be hereafter represented by "v" and "h" respectively in (v, h).

- In non-recursive mode: When CKW latches VCLR0 at "High" level, the shift register advances until the current serial Write block (60 bits) is filled up, and the line is cleared. In short, when VCLR0 is input during serial Write, it is transferred to the (v, h) memory cell after the input completion of 60 bits. Then, the data to be serially written are transferred to the (0, h+1) memory cell.

HCLR0

When CKW latches HCLR0 at "High" level, the input data at this time is taken in as data for (v, 0). From input data already entered, those not sufficient to fill up a block (60 bits) are rejected. When Pin RM is at "High" level (recursive mode), a signal to this pin will hold no meaning.

The number of counts for HCLR0 is counted only when the state latched at every CKW is at "High" level following the recognition of a "Low" level. Continuation of "High" level is counted as "one".

This operation is valid if $\overline{WE}$ is "High" when HCLR0 is input until the point at which $\overline{WE}$ becomes "Low" and is latched by CKW.

INC0

When CKW latches INC0 at "High" level, the lines are incremented by the number of times the pin was latched. The incremented lines become valid in the following two ways: when "High"-level HCLR0 is latched, and when the shift register advances to the end of the block after "High"-level VCLR0 is latched. When Pin RM is at "High" level (recursive mode), signals to this pin will hold no meaning.

The number of counts for INC0 is counted only when the state latched at every CKW is at "High" level following the recognition of a "Low" level. Continuation of "High" level is counted as "one".

This operation is valid if $\overline{WE}$ is "High" when INC0 is input until the point at which $\overline{WE}$ becomes "Low" and is latched by CKW.

- When combined with VCLR0, the number of counts "n" for INC0, from the time CKW latched on to VCLR0 until the shift register is filled to 60 bits, causes the next 60-bit data input to be written into the (n, h+1) memory cell. Note that INC0 is invalid when used simultaneously with VCLR0.
- When combined with HCLR0, the number of counts "n" for INC0, from the time CKW last latched on to HCLR0 up to the present latch, causes the following 60-bit data input to be written into the (v+n, 0) memory cell. Note that INC0 is valid when used simultaneously with HCLR0.

CKR1, CKR2

The rising edge of these pins activates the shift register of the Read port and issues signals for data output from output pins, DO10 to DO17, DO20 to DO27, and also signals which latch each internal address pointer control input (VCLR1/VCLR2, HCLR1/HCLR2, INC1/INC2).

VCLR1, VCLR2

The role of these pins depends on whether if the state of Pin RM is "High" level (recursive mode) or "Low" level (non-recursive mode).

The number of counts for VCLR1/VCLR2 is counted only when the state latched at every CKR1/CKR2 is at "High" level following recognition of a "Low" level. Continuation of "High" level is counted as "one".

- In recursive mode: When CKR1/CKR2 latch VCLR1/VCLR2 at "High" level, (0, 0) data is output 64 clocks later. Until this time, the current shift register data (60 bits) will be completed, and the shift register will retain the last output data.
- In non-recursive mode: When CKR1/CKR2 latch VCLR1/VCLR2 at "High" level, first, the block of the current serial Read and the following 60-bit block is output; and next, the serial block output with lines cleared is started. In short, when VCLR1/VCLR2 are latched, the lines of the internal address counter is cleared; but at this time, the next serial output data (v, h+1) has been sent from the memory cell to the data register. While (v, h+1) is output, (0, h+2) is transferred and then output.

HCLR1, HCLR2

When CKR1/CKR2 latch HCLR1/HCLR2 at "High" level, (v, 0) data is output 64 clocks later. In the meantime, the current shift register data output will be completed, and the shift register will retain the final output data. When Pin RM is at "High" level (recursive mode), any signal sent to these pins will hold no meaning.

The number of counts for HCLR1/HCLR2 is counted only when the state latched at every CKR1/CKR2 is latched at "High" level following the recognition of a "Low" level. Continuation of "High" level is counted as "one".

TE

This pin is used for testing. Fixed to Vss.

INC1, INC2

When CKR1/CKR2 latch INC1/INC2 at "High" level, lines are incremented by the number of times the pins are latched. The incremented lines become valid in the following two ways: when "High"-level HCLR1/HCLR2 is latched, and when after "High"-level VCLR1/VCLR2 are latched, the line address is latched at the 57th clock of the same block. When Pin RM is at "High" level (recursive mode), any signal to these pins will hold no meaning.

The number of counts "n" for INC1/INC2 is counted only when the state latched at every CKR1/CKR2 is at "High" level following the recognition of a "Low" level. Continuation of "High" level is counted as "one".

- When combined with VCLR1/VCLR2, count number "n" of INC1/INC2 enables the one after the next output data to become (n, h+2) memory cell data. Count number "n" of INC1/INC2 indicates count number for INC1/INC2 prior to the 57th block in which CKR1/CKR2 latched VCLR1/VCLR2.
  Note that INC1/INC2 are invalid when used simultaneously with VCLR1/VCLR2.
- When combined with HCLR1/HCLR2, count number "n" of INC1/INC2 enables the shift register to be output 64 clocks after HCLR1/HCLR2. Count number "n" of INC1/INC2 indicates count number from the time CKE1/CKR2 previously latched HCLR1/HCLR2 up to the point immediately before the present latch.
  Note that INC1/INC2 are valid when used simultaneously with HCLR1/HCLR2.

Data Input (DIN0 to DIN7)

Information to the data inputs is accepted and sent to the shift register at the rising edge of CKW when $\overline{WE}$ is at "Low" level. When $\overline{WE}$ is at "High" level, input data will not be accepted, and the Write shift register (gate function of Write clock) does not function.

Input to shift register is accepted immediately. However, after one block (60 bits) data input to the memory cell is completed, the input data is loaded to the data register, and data transfer from data register to memory cell is continued until the shift register is filled with new data. Thus, for serial Write data input in the serial Write mode, data is transferred to the memory cell with one block delay.

Input control ($\overline{WE}$)

Input control for DIN0 to DIN7 is conducted by $\overline{WE}$. When $\overline{WE}$ is at "Low" level, input enable is established in synchronization with CKW. But, when $\overline{WE}$ is at "High" level, input is not accepted and the Write shift register stops its shift operation. This function is used for such purposes as in thinning out input data, etc. (gate function of Write-circuit input clock (CKW) by $\overline{WE}$).

This operation is valid if $\overline{WE}$ is "High" when VCLR0, INC0, HCLR0, preset address (the case of input simultaneously with HCLR0 at APM mode) are input until the point at which $\overline{WE}$ becomes "Low" and is latched by CKW.

Data output (DO10 to DO17, DO20 to DO27)

The output buffer provides three-state TTL levels. When $\overline{OE1}$/$\overline{OE2}$ are at "Low" level, output is immediately enabled to output data synchronous with CKR1/CKR2. When $\overline{OE1}$/$\overline{OE2}$ are at "High" level, although the output goes to high impedance state, the shift register will run in synchronization with CKR1/CKR2, so that data transfer from the memory cell to the data registered, and also data loading from the data register to the the shift register are enabled.

Shift register data is output whenever necessary. This output data is data that had been transferred to the shift register from the memory cell one block before the present output block.

Output control ($\overline{OE1}$/$\overline{OE2}$)

$\overline{OE1}$ exclusively controls output pins, DO10 to DO17, while $\overline{OE2}$ exclusively controls output pins, DO20 to DO27. Both controls do not stop shift operation of the Read port shift register. When $\overline{OE1}$/$\overline{OE2}$ are at "Low," the output control for DO10 to DO17 and DO20 to DO27 is output enabled without synchronizing with CKR1/CKR2. When $\overline{OE1}$/$\overline{OE2}$ are at "High," output will be in high impedance state without synchronizing with CKR1/CKR2.

Electrical Characteristics

DC Characteristics

(Vcc=5V ± 10%, Vss=0V, Ta=0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current *1	I_{CC1}	tscw0=70ns tscr1, 2=70ns	—	—	45	mA
(Normal operation)	I_{CC2}	tscw0=70ns tscr1, 2=35ns	—	—	60	mA
(Normal operation)	I_{CC3}	tscw0=50ns tscr1, 2=50ns	—	—	60	mA
(Normal operation)	I_{CC4}	tscw0=50ns tscr1, 2=30ns	—	—	75	mA
Power supply current (when refreshing) *1, 2	I_{CC5}	tscw0=420ns tscr=70ns	—	—	20	mA

Item	Symbol	Min.	Max.	Unit
Input leakage current (for all inputs) (0V ≦ Vin ≦ 5.5V; 0V, Vcc=5.5V)	I_I (L)	–10	10	µA
Output leakage current (output in high impedance state; 0V ≦ Vout ≦ 5.5V)	Io (L)	–10	10	µA
Output voltage "High" level (I_{OH}=–1mA)	V_{OH}	2.4	—	V
Output voltage "Low" level (I_{OL}=2.1mA)	V_{OL}	—	0.6	V

Note) *1. Outputs are open.
Power supply current depends upon cycle time and output load.
*2. WE="High", only one Read port in operation.

AC Characteristics

(Vcc=5V ± 10%, Vss=0V, Ta=0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Refresh interval	t_{REF}		—	—	21	ms
CKR cycle time	t_{SCR}		30	—	70	ns
CKR pulse width	t_{CKR}		8	—	—	ns
CKR precharge time	t_{SPR}		8	—	—	ns
CKW pulse width	t_{CKW}		8	—	—	ns
CKW precharge time	t_{SPW}		15	—	—	ns
Access time from CKR	t_{SAC}		—	—	25	ns
Data output hold time from CKR	t_{SOH}		5	—	—	ns
Access time from $\overline{OE}$	t_{OEA}		—	—	20	ns
Data output hold time from $\overline{OE}$	t_{OEH}		5	—	—	ns

Note) After power ON, wait more than 200 µs (pause period) before inserting the dummy cycle. With the dummy cycle, insert VCLR (when in recursive more) or VCLR and HCLR (when in non-recursive mode) more than once and CKR and CKW insert more than 60th clock. Insert the dummy cycle to each port.

Item	Symbol	Min.	Typ.	Max.	Unit
Data output turn-off delay time from $\overline{OE}$	t_{OEZ}	—	—	20	ns
VCLR HCLR–CKR active set-up time INC CKW	t_{CKS}	5	—	—	ns
VCLR HCLR–CKR active hold time INC CKW	t_{CKH}	7	—	—	ns
VCLR HCLR–CKR inactive set-up time INC CKW	t_{CK1}	5	—	—	ns
VCLR HCLR–CKR inactive hold time INC	t_{CK2}	7	—	—	ns
CKW cycle time	t_{SCW}	50	—	2tscr	ns
DIN, CKW set-up time	t_{DS}	5	—	—	ns
DIN, CKW hold time	t_{DH}	7	—	—	ns
$\overline{WE}$, CKW active set-up time	t_{WES}	5	—	—	ns
$\overline{WE}$, CKW active hold time	t_{WEH}	7	—	—	ns
$\overline{WE}$, CKW inactive set-up time	t_{WE1}	5	—	—	ns
$\overline{WE}$, CKW inactive hold time	t_{WE2}	7	—	—	ns
ADD, CKW set-up time	t_{AS}	10	—	—	ns
ADD, CKW hold time	t_{AH}	8	—	—	ns
Input pulse rise time, fall time	t_T	3	—	40	ns

Clock Correlation

The CXK48324Q/R employs DRAM in the memory block. Thus, in order to maintain data, one of the clock relations listed below must be satisfied. Further, for NRM (non-recursive mode), use either HCLR or INC for access to all necessary memory areas within 21ms.

T_{SCW}	T_{SCR1}	T_{SCR2}	
50 to 2×T_{SCR1}	30 to T_{MAX}	T_{SCR1} to stop	ns
50 to 2×T_{SCR2}	T_{SCR2} to stop	30 to T_{MAX}	ns

For access to one entire picture (960dots×306lines) within 21ms, the maximum cycle time T_{MAX} for continuous CKR1 (or CKR2), is shown below.

$$T_{MAX}=\frac{21ms}{960dots\times306lines}\fallingdotseq 70ns$$

Stand-by mode with image data save function

To reduce power consumption while saving image data, fix WE at "High" and use only one Read port. In this mode, writing is not possible. Clock correlation will be of the following listed below. Further, for NRM (non-recursive mode), use either HCLR or INC for access to all necessary memory areas within 21ms.

T_{SCW}	T_{SCR1}	T_{SCR2}	
50 to 6×T_{SCR1}	30 to T_{MAX}	T_{SCR1} to Stop	ns
50 to 6×T_{SCR2}	T_{SCR2} to Stop	30 to T_{MAX}	ns

For access to one entire picture (960dots ×306lines) within 21ms, the maximum cycle time T_{MAX} for continuous CKR1 (or CKR2) is shown below.

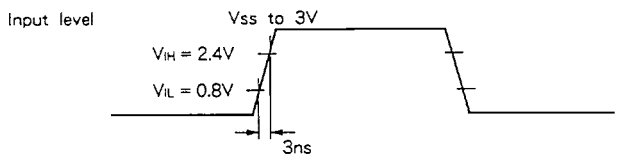
$$T_{MAX}=\frac{21ms}{960dots\times306lines}\fallingdotseq 70ns$$

Input/Output Capacitance (This parameter is sampled value, not 100% tested.)

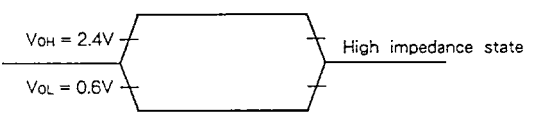
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input	C_{IN}	Ta=0°C to +70°C	—	—	7	pF
Data output capacitance (DO10 to DO27)	C_D	Vcc=+5V±10%	—	—	7	pF
Input capacitance (ADD0 to ADD3)	C_T		—	—	10	pF

AC Characteristics Test Conditions

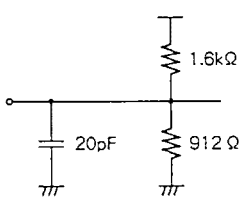
1) Input



2) Output

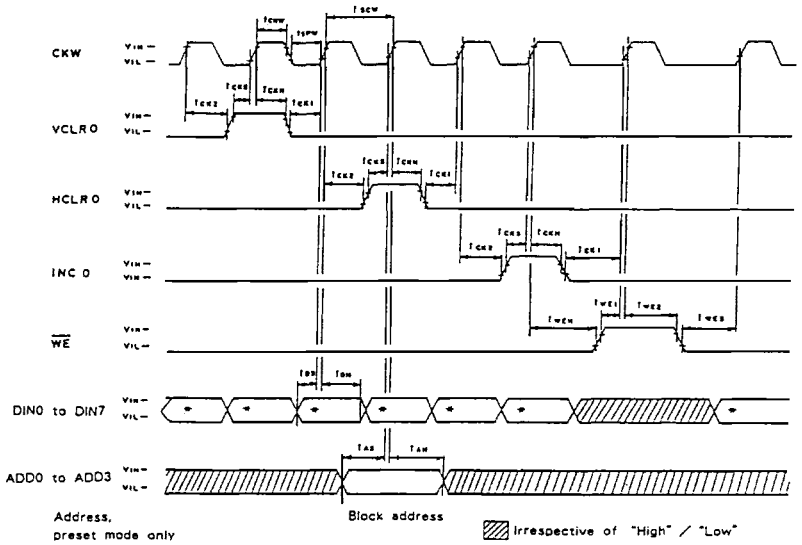


3) Data output load
DO10 to DO17, DO20 to DO27



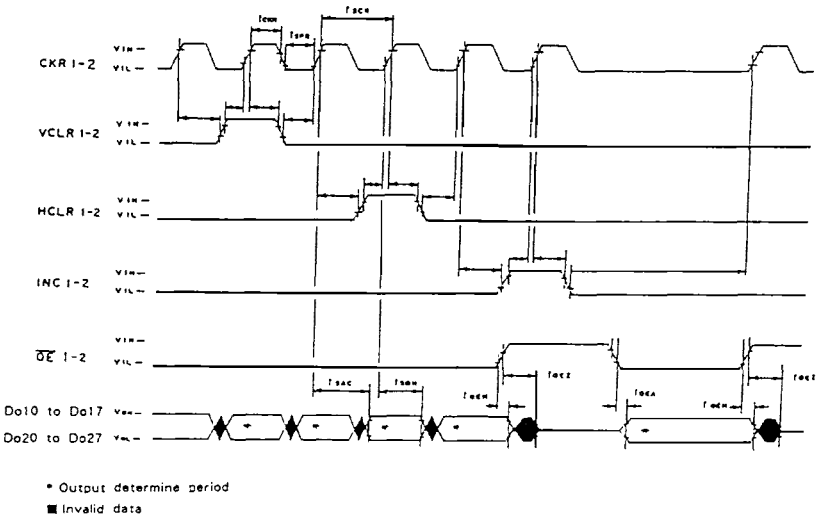
Timing Diagram

Write port



* Irrespective of "High"/"Low" levels, depending upon the control method of the input determine period, VCLR0, etc.

Read port



Description of Functions

The CXK48324Q/R has the following three operation modes. As to the details of timing, etc., refer to relevant section.

1. **Recursive mode**
   This mode handles the memory as a simple digital delay line. Control is enabled by VCLR0/VCLR1/VCLR2, $\overline{WE}$, $\overline{OE1}$, and $\overline{OE2}$.
2. **Non-recursive mode**
   This mode controls the memory in block/line units. Control is enabled by VCLR0/VCLR1/VCLR2, INC0/INC1/INC2, HCLR0/HCLR1/HCLR2, $\overline{WE}$, $\overline{OE1}$, and $\overline{OE2}$.
3. **Non-recursive mode, address preset mode**
   These modes control the memory in block/line units, and provide free address setting in block units when writing into the memory. Control is enabled by VCLR0/VCLR1/VCLR2, INC0/INC1/INC2, HCLR0/HCLR1/HCLR2, $\overline{WE}$, $\overline{OE1}$, $\overline{OE2}$, ADD0/ADD1/ADD2/ADD3.

Function Tables

Function table – 1 <Operation mode table>

Operation mode	Control input		Address input
	RM	APM	ADD0 to ADD3
Recursive mode	High	Low	——
Non-recursive mode	Low	Low	——
Non-recursive mode, address preset mode	Low	High	Input determination

——: No pin name for this mode.

Correspondence table for address/block division

Block No.	ADD3	ADD2	ADD1	ADD0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Note) The block number increases according to the writing/reading sequence within the line.

Function table – 2 <Write>

Mode		Operation cycle	RM	VR0	HR0	IC0	APM	A0 to A3	Internal address pointer
Recursive mode	1	Initial cycle	High	High	—	—	Low	—	(v, h) clears to (0, 0).
	2	Normal cycle		Low	—	—	Low	—	Circulates from 0 to 293,759.
Non-recursive mode	1	Initial cycle	Low	High ①	High ①	Low	Low	—	(v, h) clears to (0, 0).
	2	Normal cycle		Low	Low	Low	Low	—	(v, h) advances to the end of Line v.
	3	First block cycle		Low	High	Low	Low	—	h of (v, h) is cleared to (v, 0).
	4	Line address cycle		Low	High	nHigh ②	Low	—	v is advanced by "n," and h is cleared, changing (v, h) to (v+n, 0).
	5	VCLR0 special cycle No. 1		High	Low	Low	Low	—	(v, h) advances to the end of Block h, and v is cleared to (0, h+1).
	5	VCLR0 special cycle No. 2		High	Low	nHigh ③	Low	—	(v, h) advances to the end of Block h, and v is set to (n, h+1).
	5	VCLR0 special cycle No. 3		High ④	High ④	nHigh ④	Low	—	v is set, and h is cleared, changing from (v, h) to (n, 0).

VR : VCLR0
HR0 : HCLR0
IC0 : INC0
A0 to A3 : ADD0 to ADD3
(v, h), v : Number of lines for the Write port during control signal input
h : Number of the blocks for the Write port during control signal input
High : Latched by CKW at "High" level
nHigh : Latched by CKW at "High" level "n" number of times

Note)
- The structure of this device is 306 lines, 16 blocks, and 60 bits.
- For functions of write, address, counter, and reset; input of at least one VCLR0 for the recursive mode, or at least one input of VCLR0 and HCLR0 for the non-recursive mode is necessary.
- Input for Pins RM and APM must be set to either "Low" or "High" in terms of DC.

Note ① It is necessary to either simultaneously input VCLR0 and HCLR0, or to input HCLR0 before the first clock of the block following the block containing VCLR0.

Note ② nHigh: Number of times INC0 was in "High" state before HCLR0 → HCLR0.

Note ③ nHigh: Number of times INC0 was in "High" state before the first clock of the block following VCLR0 → Block h.

Note ④ It is necessary to input INC0 and HCLR0 before the first clock of the block following the block containing VCLR0.

Function table – 3 <Write>

Mode		Operation cycle	RM	VR0	HR0	IC0	APM	A0 to A3	Internal address pointer
Non-recursive address preset mode	1	Initial cycle	Low	High ①	High ①	Low	High ⑤	Input determination	v is cleared and h is set, changing from (v, h) to (0, ADD).
	2	Normal cycle		Low	Low	Low	High ⑤	—	(v, h) advances to the end of Line v.
	3	Address preset cycle		Low	High	Low	High ⑤	Input determination	h of (v, h) is set to (v, ADD).
	4	Line address, block address preset cycle		Low	High	nHigh ②	High ⑤	Input determination	v is advanced by "n," and h is set, changing (v, h) to (v+n, ADD).
	5	VCLR0 special cycle No. 1		High	Low	Low	High ⑤	—	(v, h) advances to the end of Block h, and v is cleared, changing to (0, h+1).
	5	VCLR0 special cycle No. 2		High	Low	nHigh ③	High ⑤	—	(v, h) advances to the end of Block h, and v is set, changing to (n, h+1).
	5	VCLR0 special cycle No. 3		High ④	High ④	nHigh ④	High ⑤	Input determination	(v, h) is set to (n, ADD).

VR0 : VCLR0
HR0 : HCLR0
IC0 : INC0
A0 to A3 : ADD0 to ADD3
(v, h), v : Number of lines for the Write port during control signal input
h : Number of the blocks for the Write port during control signal input
High : Latched by CKW at "High" level
nHigh : Latched by CKW at "High" level "n" number of times

Note)
- The structure of this device is 306 lines, 16 blocks, and 60 bits.
- For functions of write, address, counter, and reset; input of at least one VCLR0 for the recursive mode, or at least one input of VCLR0 and HCLR0 for the non-re cursive mode is necessary.
- Input for Pins RM and APM must be set to either "Low" or "High" in terms of DC.

Note① It is necessary to either simultaneously input VCLR0 and HCLR0, or to input HCLR0 before the first clock of the block following the block containing VCLR0.

Note② nHigh: Number of times INC0 was in "High" state before HCLR0 HCLR0.

Note③ nHigh: Number of times INC0 was in "High" state before the first clock of the block following VCLR0 → Block h.

Note④ It is necessary to input INC0 and HCLR0 before the first clock of the block following the block containing VCLR0.

Note⑤ In the function table for the address preset mode, the block address is latched at the same "High"-level HCLR0 which was latched by CKW.

Function table – 4 <Read 1>

Mode		Operation cycle	RM	VR1	HR1	IC1	Internal address pointer
Recursive mode	1	Initial cycle	High	High	—	—	(v, h) advances to the end of Block h, goes to (0, 0) with a 64-clock delay from VCLR1.
	2	Normal cycle		Low	—	—	Circulates from 0 to 293,759.
Non-recursive mode	1	Initial cycle	Low	High ①	High ①	Low	(v, h) advances to the end of Block h, and cleared to (0, 0) after a 64-clock delay from HCLR1.
	2	Normal cycle		Low	Low	Low	(v, h) advances to the end of Line v.
	3	First block cycle		Low	High	Low	(v, h) advances to the end of Block h, goes to (v, 0) after a 64-clock delay from HCLR1.
	4	Line address cycle		Low	High	nHigh ②	(v, h) advances to the end of Block h, goes to (v+n, 0) after a 64-clock delay from HCLR1.
	5	VCLR1 special cycle No. 1		High	Low	Low	(v, h) advances to the end of Blocks h and h+1, and v is cleared to (0, h+2).
	5	VCLR1 special cycle No. 2		High	Low	nHigh ③	(v, h) advances to the end of Blocks h and h+1, and v is set to (n, h+2).
	5	VCLR1 special cycle No. 3		High ④	High ④	nHigh ④	(v, h) advances to the end of Block h; v is set and h is cleared after a 64-clock delay from HCLR1.

VR1 : VCLR1
HR1 : HCLR1
IC1 : INC1
(v, h), v : Number of lines for the Read port during control signal input
h : Number of the blocks for the Read port during control signal input
High : Latched by CKR1 at "High" level
nHigh : Latched by CKR1 at "High" level "n" number of times

Note)
- The structure of this device is 306 lines, 16 blocks, and 60 bits.
- Address preset is not possible during Read, regardless of APM pin control.
- For functions of Read, address, counter, and reset; input of at least one VCLR1 for the recursive mode, or at least one input of VCLR1 and HCLR1 for the non-recursive mode is necessary.
- Input for Pins RM and APM should be set to either "Low" or "High" in terms of DC.

Note ① It is necessary to either simultaneously input VCLR1 and HCLR1, or to input HCLR1 before the 55th clock of the block that contains VCLR1. Inputting VCLR1 prior to the 64-clock delay from HCLR1 is prohibited.

Note ② nHigh: Number of times INC1 was in "High" state before HCLR1 HCLR1.

Note ③ nHigh: Number of times INC1 was in "High" state before VCLR1 55th clock of Block h.

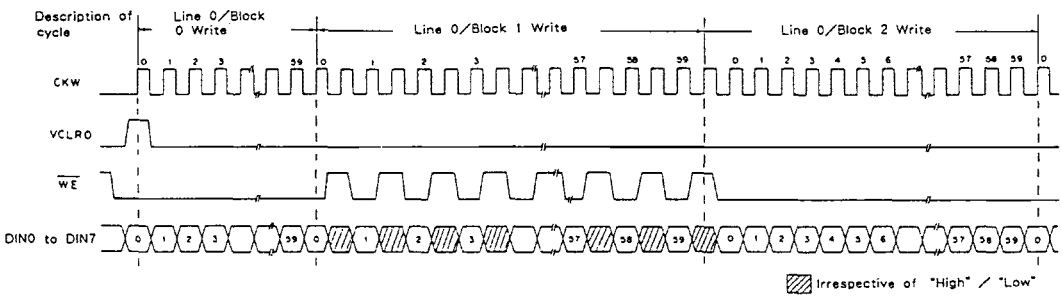
Note ④ It is necessary to enter INC1 and HCLR1 before the 55th clock of the block containing VCLR1.

Function table–5 <Read 2>

For VCLR2, HCLR2 and INC2, function table is the same as Function table – 4.

Recursive mode – Write

1. Initial cycle 2. Normal cycle

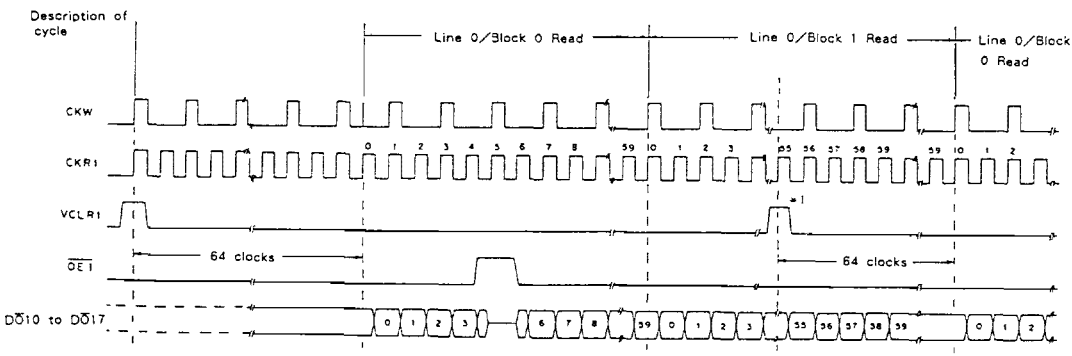


Note) • After Write is finished up to Line 0/Block 15, the next 60 bits are automatically written to Block 0 of the next line.

• After Write is finished up to Line 305/Block 15, the next 60 bits are automatically written as Line 0/Block 0.

Recursive mode – Read

1. Initial cycle 2. Normal cycle



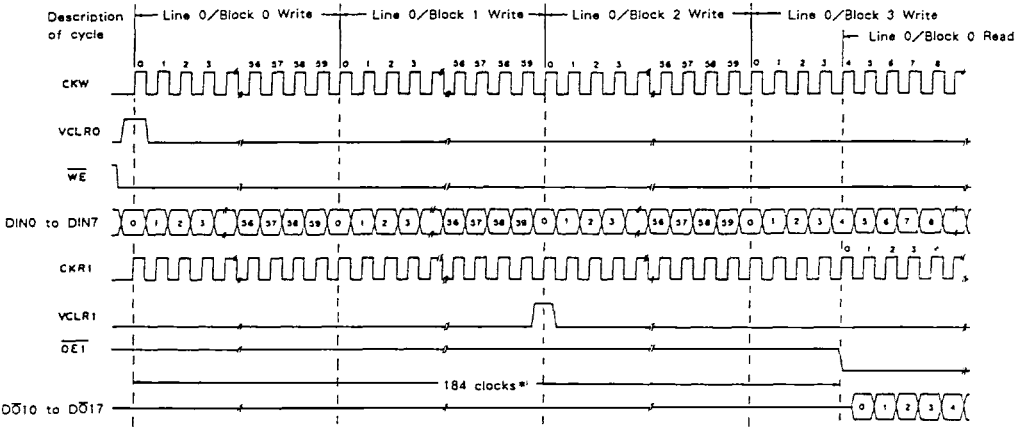
Note) • After Read is finished up to Line 0/Block 15, the next 60 bits are automatically read from block 0 of the next line.

• After Read is finished up to Line 305/Block 15, the next 60 bits are automatically read from Line 0/Block 0.

*1 If VCLR is input within 55 clocks of the present data being read, the last data of the block will be maintained on hold. If VCLR is input after the 55th clock, the block following the present will also be read, and Block 0 data is output with a 64-clock delay.

Recursive mode (For non-recursive mode, VCLR in the figure is equivalent to HCLR.)

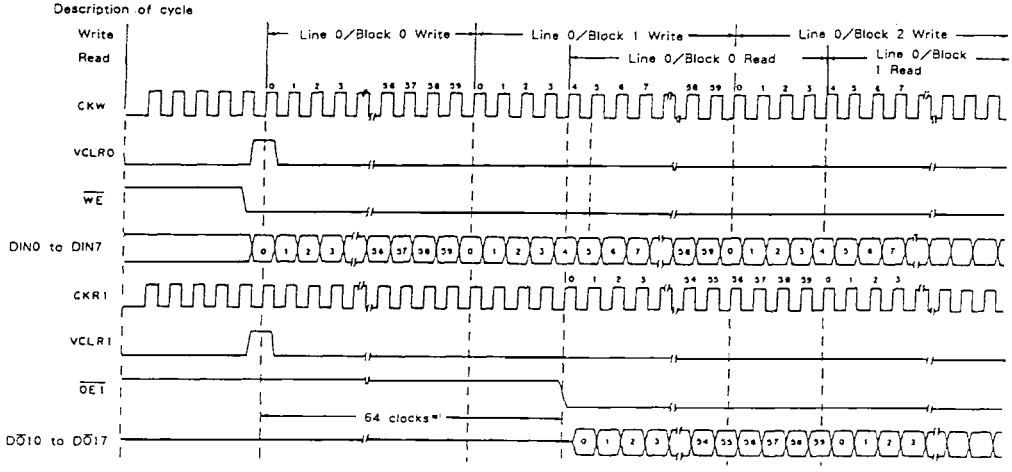
New data access mode



Note) *1 For access to new data, the block Write is transferred after the 60-bit Write, followed by the Read transfer of the same block before the read-out. Thus, the Read clock delay from the Write clock is at least 184 clocks.

Recursive mode (For non-recursive mode, VCLR in the figure is equivalent to HCLR.)

Old data access mode

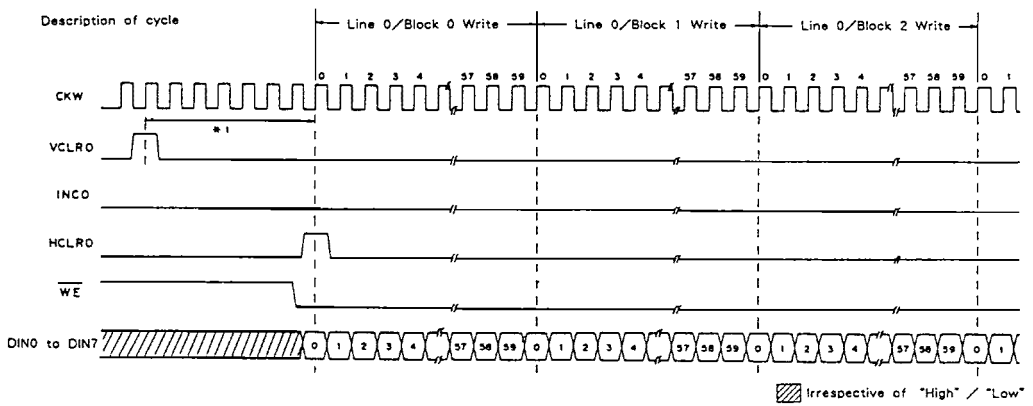


Note) • When the Read clock delay is 65 to 183 clocks from the Write clock, although it is undeterminable whether if the data access is new or old, the Write of the new data is guaranteed.

*1 For access to old data, because the Read transfer must come before the Write transfer of the new data, the Read clock delay must be within 64 clocks from the Write clock.

Non-recursive mode – Write

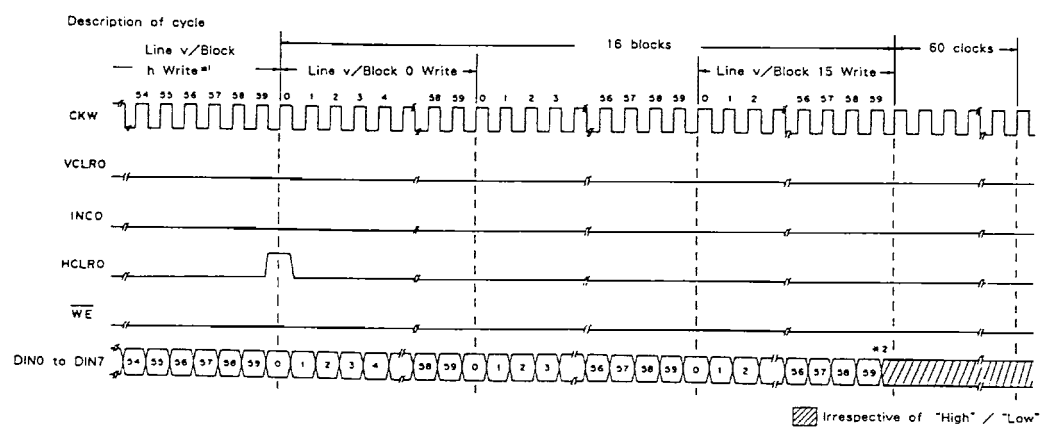
1. Initial cycle (Writes data from Line 0/Block 0.) 2. Normal cycle



Note) *1 For the initial cycle, it is necessary to simultaneously input VCLR0 and HCLR0, or input HCLR0 before the first clock of the block following the block containing VCLR0.

Non-recursive mode – Write

3. First block cycle (Writes data from the beginning of a block.)

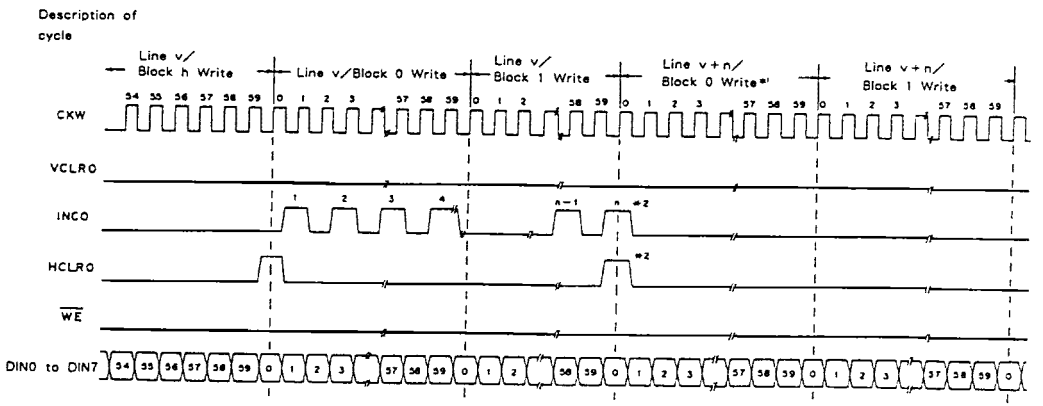


Note) *1 After the Write of one block (60 bits) is completed, it is transferred by Write transfer during the next block.

*2 For non-recursive mode, after Writing is completed up to the final block of a line, no further writing is possible. Also, Write transfer of the final block is accomplished 60 clocks after the final block Write is completed.

Non-recursive mode – Write

4. Line address cycle (Address control in the direction of lines.)

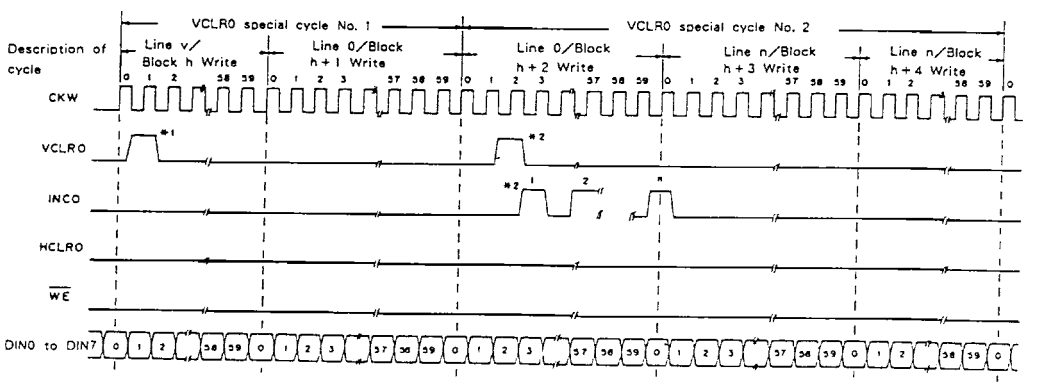


Note) *1 "n" indicates the number of INC0 inputs.

*2 The present HCLR0 latches from the previous HCLR0 to the INC0 which was input simultaneously with the present HCLR0. Line address recursively circulates from the present address depending upon the number of INC0 inputs.

Non-recursive mode – Write

5. VCLR0 special cycle No. 1 and 2

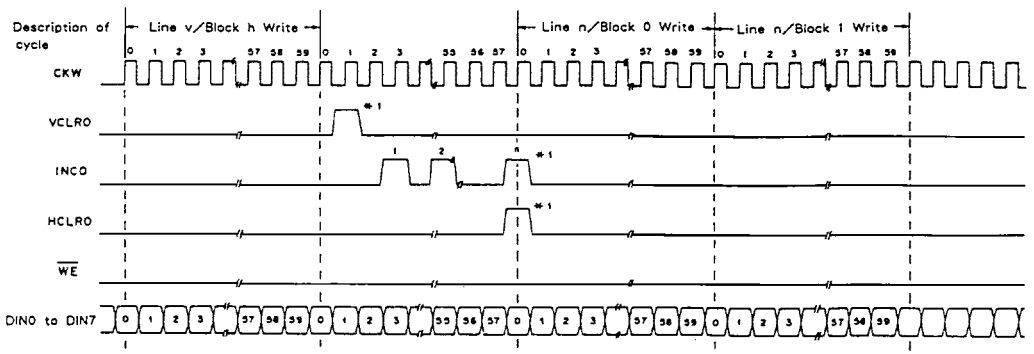


Note) *1 VCLR0 input at the 1st clock of Block h or after, resets the line address and is latched at the end of the block.

*2 When VCLR0 is input at the 1st clock of Block h or after, followed by INC0 input, the line address is reset and incremented by the number of INC0 inputs to Block 1. The line address is latched at the beginning of the next block.
When VCLR0 and INC0 are input simultaneously, only the address is valid.

Non-recursive mode – Write

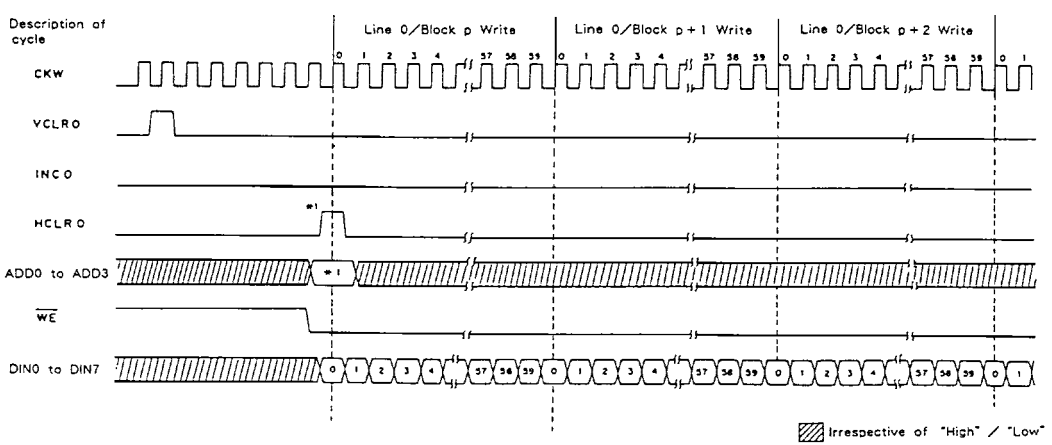
6. VCLR0 special cycle No. 3



Note) *1 When VCLR0 is input at the 1st clock of Block h or after, INC0 is input "n" times and followed by HCLR0, the line address is reset and incremented by the number of INC0 inputs. Line address is latched while block address is reset by HCLR0.

Non-recursive address preset mode – Write

1. Initial cycle 2. Normal cycle



Note) *1 The block address is latched by HCLR0 in the address preset mode.

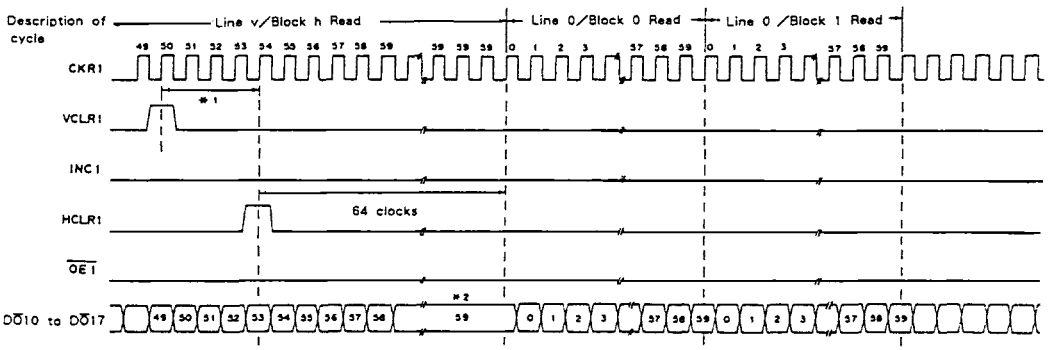
Non-recursive address preset mode – Write

3. Address preset cycle
4. Line address, block address, preset cycle
5. VCLR0 special cycle No. 1, 2, and 3

Above three cycles are different from the non-recursive mode only in the point that the block address is latched by HCLR0. Therefore, refer to the section on non-recursive mode for details.

Non-recursive mode – Read

1. Initial cycle (Reads data from Line 0/Block 0) 2. Normal cycle

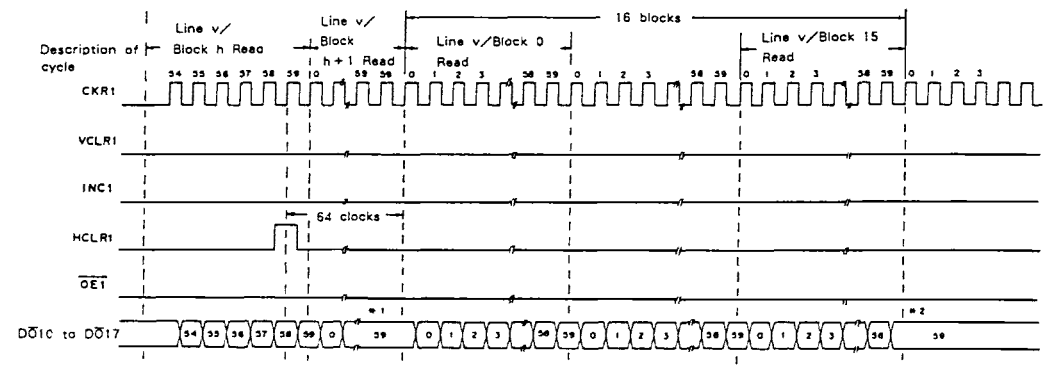


Note) *1 If VCLR1 and HCLR1 are input simultaneously, or HCLR1 is input within the 55th clock of the block containing VCLR1, Line 0/Block 0 data is output with a 64-clock delay from HCLR1.

*2 If HCLR is input within the 55th clock of the present block being read, the last data of the block is maintained on hold. If HCLR is input after the 55th clock, the block following the present will also be read, and Block 0 data is output with a 64-clock delay.

Non-recursive mode, Read

3. First block cycle

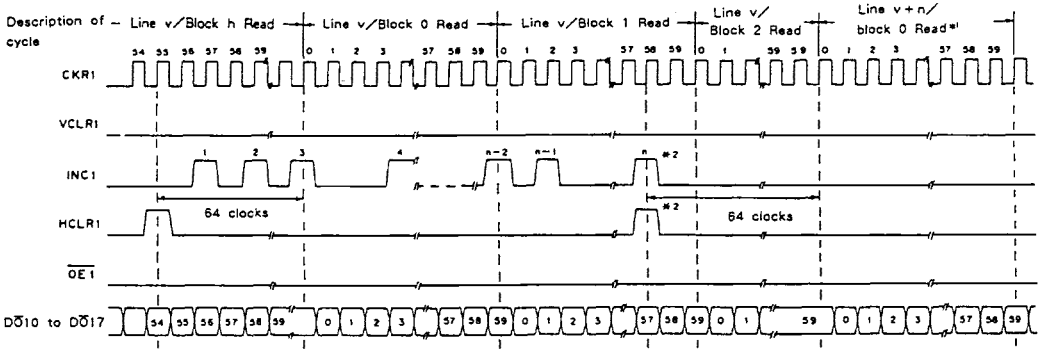


Note) *1 If HCLR is input within the 55th of the present block being read, the last data of the block is maintained on hold. If HCLR is input after the 55th clock, the block following the present will also be read, and Block 0 data is output with a 64-clock delay.

*2 For the non-recursive mode, after reading is completed to the last block of the line, the last data output is maintained on hold.

Non-recursive mode – Read

4. Line address cycle

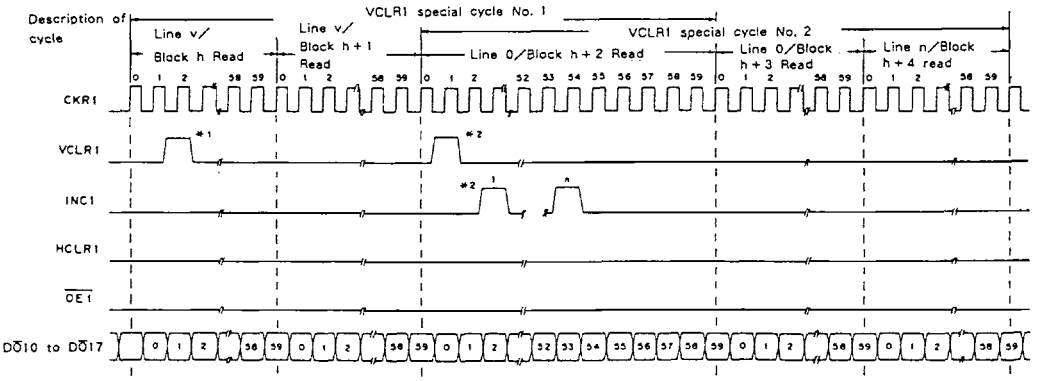


Note) *1 "n" indicates the number of INC1 inputs.

*2 The present HCLR1 latches from the clock after the previous HCLR1 to the INC1 which was input simultaneously with the present HCLR1. The line address recursively circulates from the present address depending upon the number of INC1 inputs.

Non-recursive mode – Read

5. VCLR1 special cycle No. 1 and 2

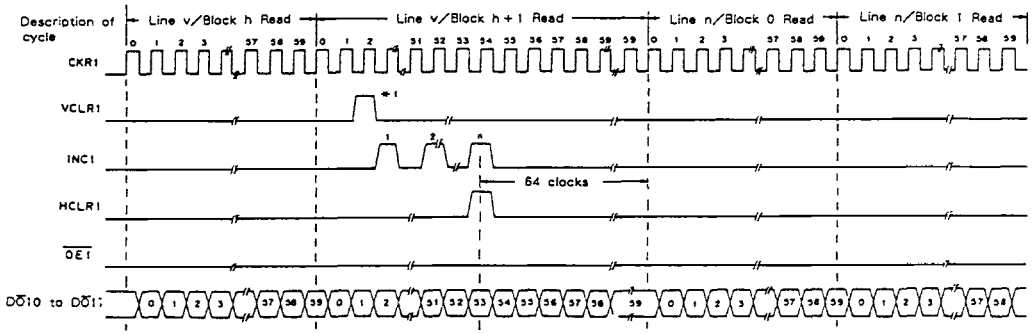


Note) *1 VCLR1 input within the 56th clock of a block reading, resets the line address and is latched at the 57th clock. Read transfer of Line 0/Block h+2 is carried out in the following block.

*2 When VCLR1 is input within the 56th clock during the reading of a block and then followed by INC1 input, the line address is reset and incremented by the number of INC1 inputs within the 56th clock when the block was read. The line address is latched at the 57th clock. When VCLR1 and INC1 are input simultaneously, the address reset is valid.

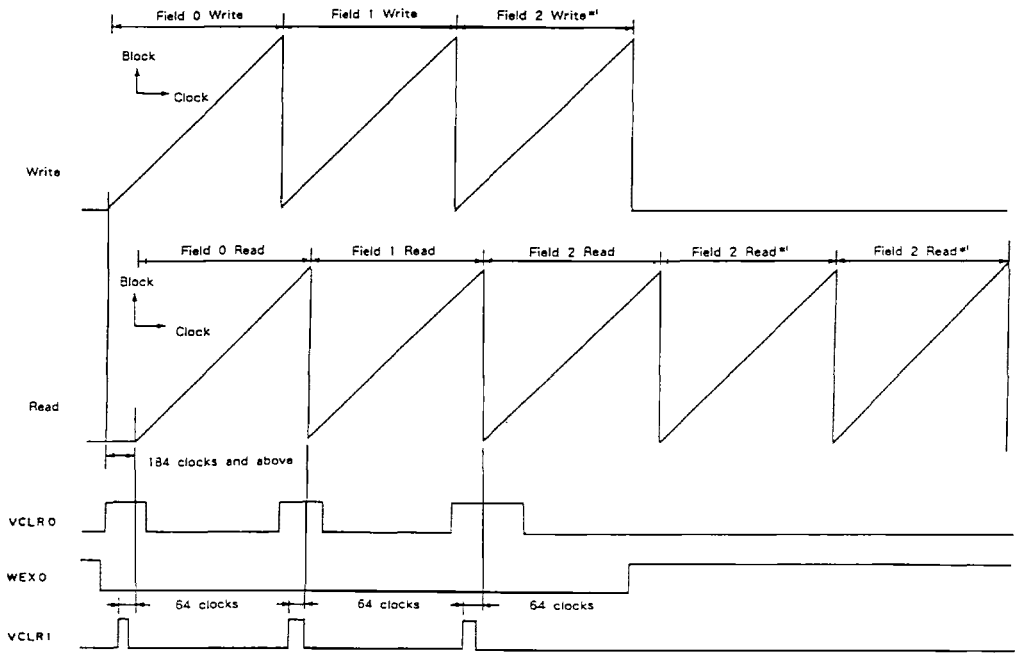
Non-recursive mode – Read

6. VCLR1 special cycle No. 3



Note) *1 When VCLR1 is input to a block, followed by inputs of INC1 "n" times and HCLR1 before the 56th clock, the line address is reset and incremented by the number of INC1 inputs. The line address is latched and the block address is reset in the next clock.

Application Example 1. For delay line, field memory in recursive mode

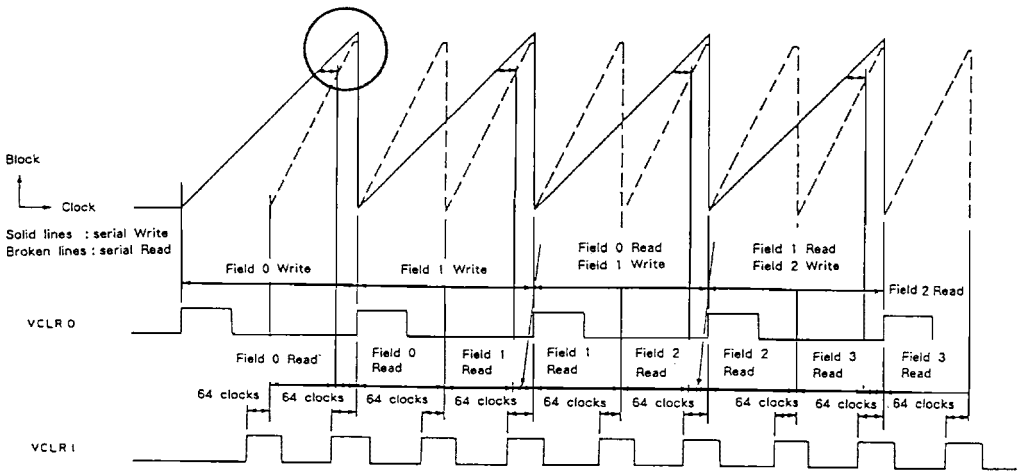


Continuous inputs of CKW0 and CKR1, $\overline{OET}$ = "Low"

Note)
- If the cycle times of CKW and CKR1 are equal, this example is also possible when asynchronous.
- If the cycle times differ between CKW and CKR1, there is a possibility of Read overtaking Write. Refer to Application Example 2.
- In non-recursive mode, it is necessary to advance lines one at a time with combinations of INC and HCLR inputs.

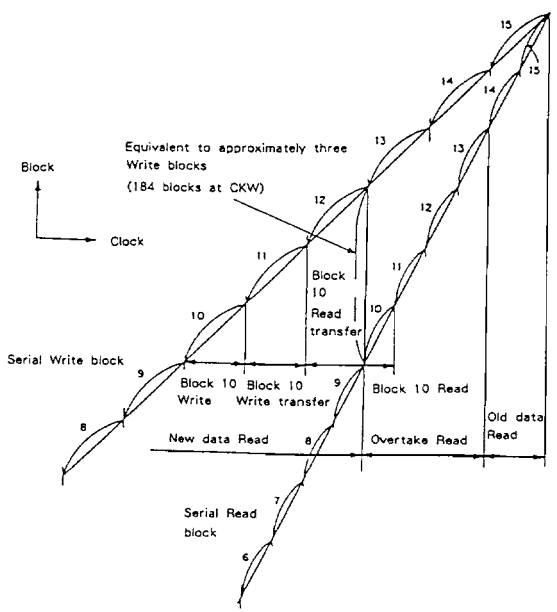
*1 When using 306 lines, 16 blocks, and 60 bits, continuous Read is possible by inputting CKR1 and CKW without VCLR1.

Application Example 2. Double-speed conversion in recursive mode



Continuous inputs of CKW0 and CKR1, $\overline{WE}$ = "Low," $\overline{OET}$ = "Low"

Description of circled area



- Overtake Read
  For double-speed conversion, in order to read the written block data, the phase delay of Read from Write must be equivalent to three Write blocks (184 clocks at CKW).

Application Example 3. Writing 1/2 compressed data in memory for non-recursive mode and address preset mode.

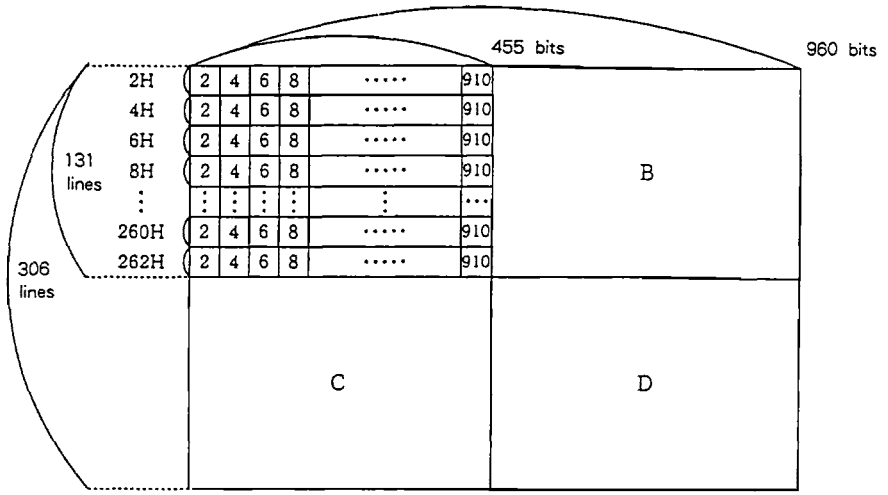
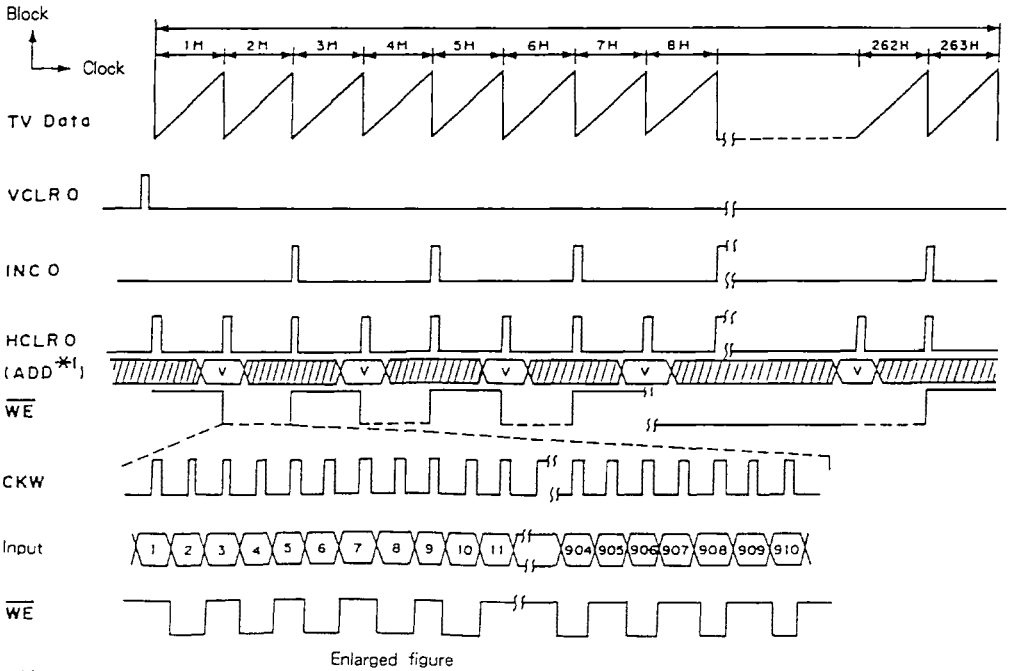


Fig. Inside of the memory

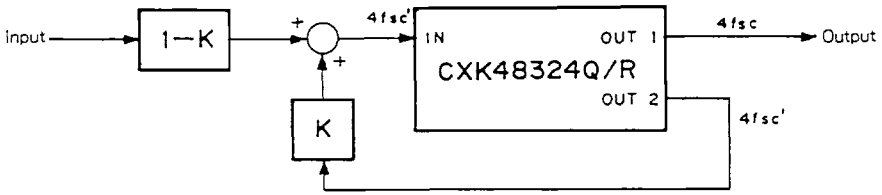


V : Valid address
▨ Irrespective of "High" / "Low"

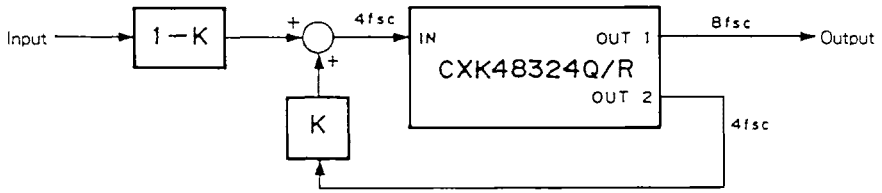
Note) *1 Use of the address preset mode enables writing to areas of B, C, and D. Writing to area C is also enabled by operating INC0 in non-recursive mode.

3-port Field Memory Application Example

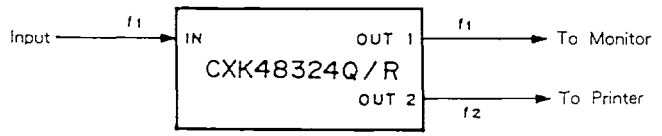
1. NR+TBC



2. NR+double scan



3. Monitor and Printer Concurrent Drive

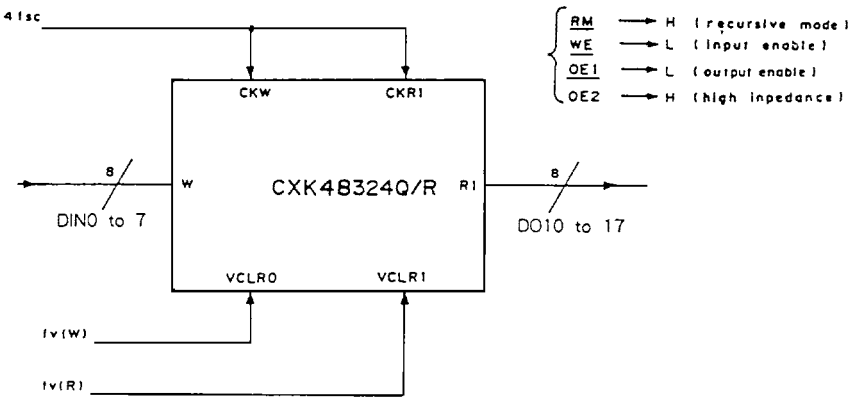


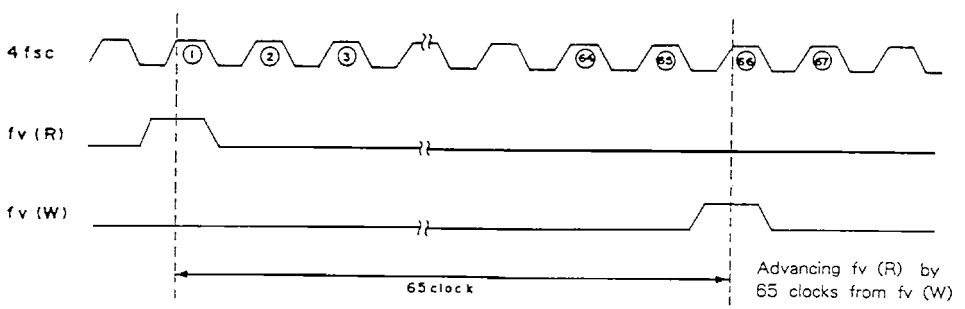
Application Circuit (1)

Using recursive mode: The following diagram shows a circuit with:

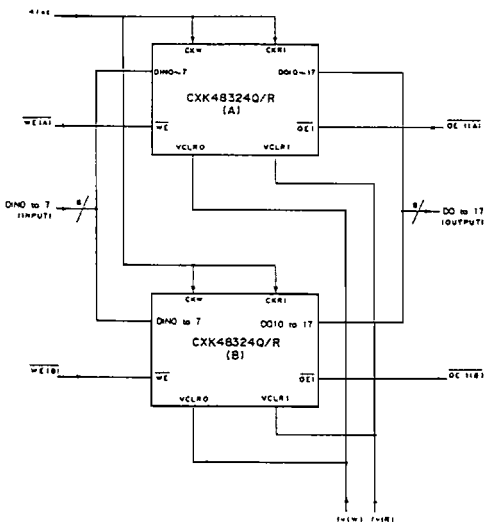
1) 1 field delay
2) 1 frame delay

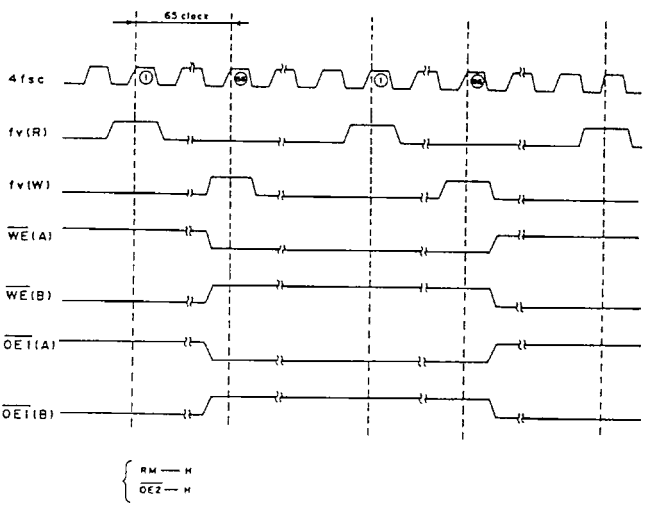
(1) 1 field delay:





Application Circuit (2) 1 frame delay

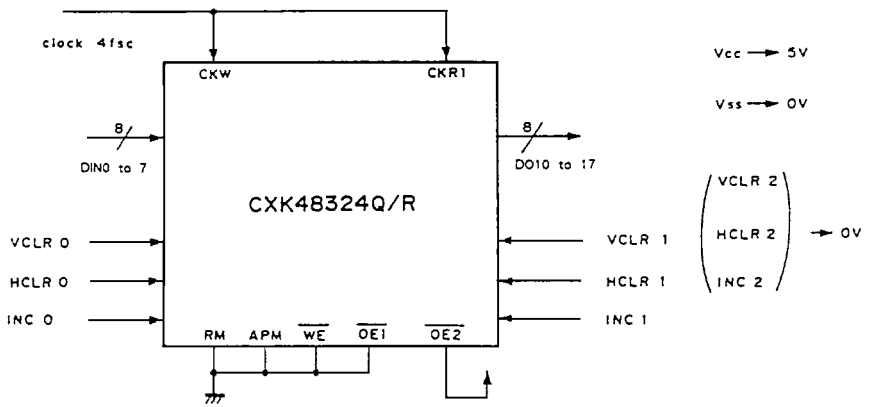


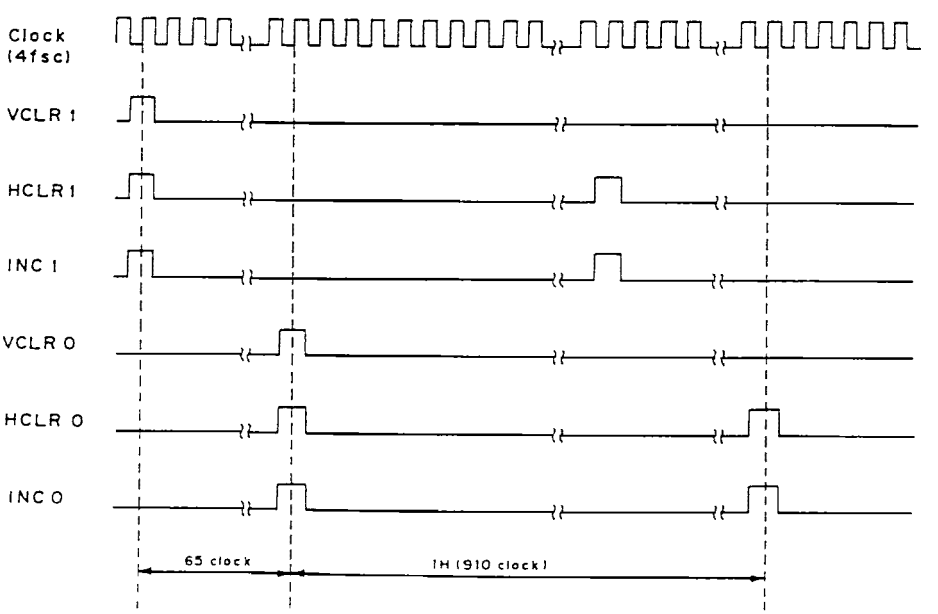


Note)
1. Do not turn off CKW for transfer control between DRAM and I/O port.
2. Do not turn off CKR1 for refreshing.
3. Switchover A chip and B chip with $\overline{WE}$ and $\overline{OE1}$.

Application Circuit (3)

The following is a circuit achieving "1 field delay" using non-recursive mode.

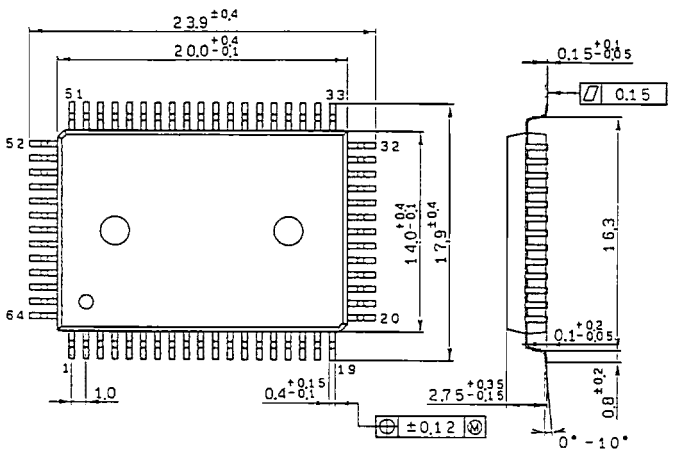




Package Outline Unit : mm

CXK48324Q

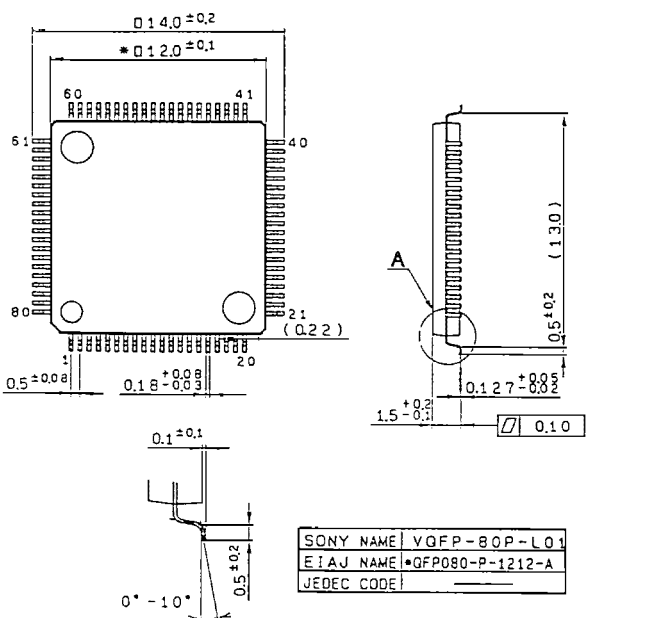
64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	•QFP064-P-1420-A
JEDEC CODE	——

CXK48324R

80pin VQFP (Plastic) 0.5g



SONY NAME	VQFP-80P-L01
EIAJ NAME	•QFP080-P-1212-A
JEDEC CODE	——

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.