PRELIMINARY

CY7C1041AV33/ GVT73256A16

256K x 16 Static RAM

Features

- **Fast access times: 10, 12 ns**
- **Fast $\overline{OE}$ access times: 5, 6, and 7 ns**
- **Single +3.3V ±0.3V power supply**
- **Fully static—no clock or timing strobes necessary**
- **All inputs and outputs are TTL-compatible**
- **Three state outputs**
- **Center power and ground pins for greater noise immunity**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options**
- **Automatic $\overline{CE}$ power-down**
- **High-performance, low power consumption, CMOS double-poly, double-metal process**
- **Packaged in 44-pin, 400-mil SOJ and 44-pin, 400-mil TSOP**

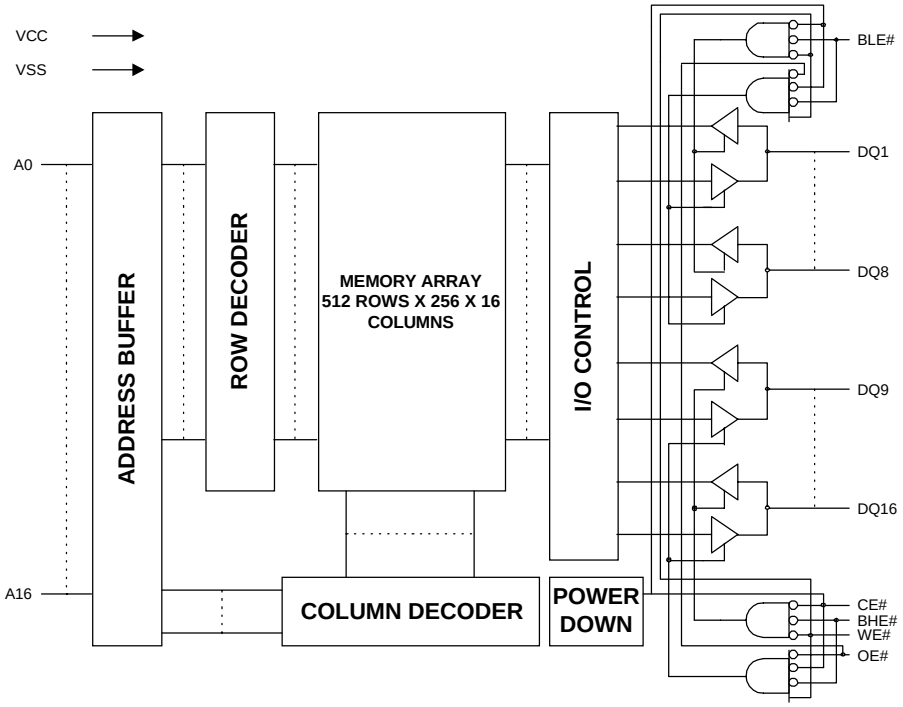
Functional Description

The CY7C1049AV33\GVT73512A8 is organized as a 262,144 x 16 SRAM using a four-transistor memory cell with a high-performance, silicon gate, low-power CMOS process. Cypress SRAMs are fabricated using double-layer polysilicon, double-layer metal technology.

This device offers center power and ground pins for improved performance and noise immunity. Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers Chip Enable ($\overline{CE}$), separate Byte Enable controls ($\overline{BLE}$ and BHE) and Output Enable ($\overline{OE}$) with this organization.

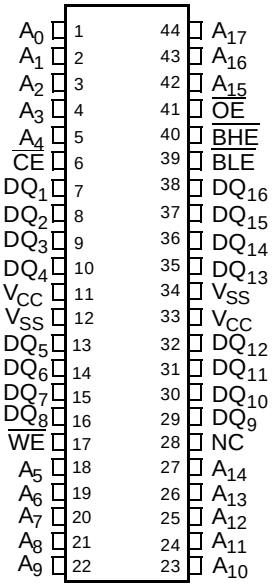
The device offers a low-power standby mode when chip is not selected. This allows system designers to meet low standby power requirements.

Functional Block Diagram



Pin Configuration

SOJ/TSOP II
Top View



Selection Guide

			CY7C1049AV33-10/ GVT73512A8-10	CY7C1049AV33-12/ GVT73512A8-12
Maximum Access Time (ns)			10	12
Maximum Operating Current (mA)			240	210
Maximum CMOS Standby Current (mA)	Com'l/Ind'l		10	10
	Com'l	L	3.0	3.0

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$	$\overline{BHE}$	DQ_1–D_8	DQ_9–D_{16}	POWER
Low Byte Read (DQ_1–DQ_8)	L	H	L	L	H	Q	High-Z	Active
High Byte Read (DQ_9–DQ_{16})	L	H	L	H	L	High-Z	Q	Active
Word Read (DQ_1–DQ_{16})	L	H	L	L	L	Q	Q	Active
Low Byte Write (DQ_1–DQ_8)	L	L	X	L	H	D	High-Z	Active
High Byte Write (DQ_9–DQ_{16})	L	L	X	H	L	High-Z	D	Active
Word Write (DQ_1–DQ_{16})	L	L	X	L	L	D	D	Active
Output Disable	L	X	X	H	H	High-Z	High-Z	Active
	L	H	H	X	X	High-Z	High-Z	Active
Standby	H	X	X	X	X	High-Z	High-Z	Standby

Pin Descriptions

SOJ & TSOP Pin Numbers	Pin Name	Type	Description
1, 2, 3, 4, 5, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 42, 43, 44	A_0–A_{17}	Input	Addresses Inputs: These inputs determine which cell is addressed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is LOW, the chip is selected. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enable: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, the data is written to or read from the lower byte (DQ_1–DQ_8). When $\overline{BHE}$ is LOW, the data is written to or read from the higher byte (DQ_9–DQ_{16}).
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ_1–DQ_{16}	Input/ Output	SRAM Data I/O: Data inputs and data outputs. Lower byte is DQ_1–DQ_8 and upper byte is DQ_9–DQ_{16}.
11, 33	V_{CC}	Supply	Power Supply: 3.3V ±0.3V%.
12, 34	V_{SS}	Supply	Ground.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic).....–55°C to +125°

Junction Temperature .....+125°

Power Dissipation 1.0W

Short Circuit Output Current ..... 50 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

Note:
1. T_A is the “Instant On” case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Conditions	Min.	Max.	Unit
V_{IH}	Input High (Logic 1) Voltage[2, 3]		2.2	V_{CC}+0.5	V
V_{II}	Input Low (Logic 0) Voltage[2, 3]		–0.5	0.8	V
IL_I	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	–5	5	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–5	5	µA
V_{OH}	Output High Voltage[2]	I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OL} = 8.0 mA		0.4	V
V_{CC}	Supply Voltage[2]		3.0	3.6	V

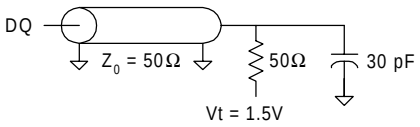
Parameter	Description	Conditions	Power	Typ.	-10	-12	Unit
I_{CC}	Power Supply Current: Operating[4, 5]	Device selected; $\overline{CE} \le V_{IL}$; V_{CC} = Max.; $f = f_{MAX}$; outputs open	std.	90	240	210	mA
			low		240	210	
I_{SB1}	TTL Standby[5]	$\overline{CE} \ge V_{IH}$; V_{CC} = Max.; $f = f_{MAX}$	std.	25	70	60	mA
			low		70	60	
I_{SB2}	CMOS Standby[5]	$\overline{CE1} \ge V_{CC} - 0.2$; V_{CC} = Max.; all other inputs $\le V_{SS} + 0.2$ or $\ge V_{CC} - 0.2$; all inputs static; f = 0	std.	0.1	10	10	mA
			low		3.0	3.0	

Capacitance[6]

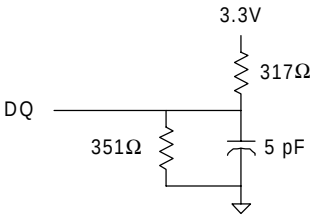
Parameter	Description	Test Conditions	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
$C_{I/O}$	Input/Output Capacitance (DQ)		8	pF

Note:
2. All voltages referenced to V_{SS} (GND).
3. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{RC}/2$.
   Undershoot: $V_{IL} \le -2.0V$ for $t \le t_{RC}/2$
4. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
5. Typical values are measured at 3.3V, 25°C, and 20 ns cycle time.
6. This parameter is sampled.

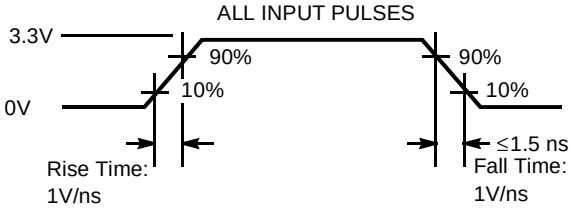
AC Test Loads and Waveforms



(a)



(b)



Switching Characteristics[5] Over the Operating Range

Parameter	Description	7C1041AV33-10/ GVT73256A16-10		7C1041AV33-12/ GVT73256A16-12		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	READ Cycle Time	10		12		ns
t_{AA}	Address Access Time		10		102	ns
t_{ACE}	Chip Enable Access Time		10		12	ns
t_{OH}	Output Hold from Address Change	3		3		ns
t_{LZCE}	Chip Enable to Output in Low-Z[6, 7]	3		3		ns
t_{HZCE}	Chip Disable to Output in High-Z[6, 7, 8]		5		6	ns
t_{AOE}	Output Enable Access Time		5		6	ns
t_{LZOE}	Output Enable to Output in Low-Z	0		0		ns
t_{HZOE}	Output Enable to Output in High-Z[6, 8]		5		6	ns
t_{ABE}	Byte Enable Access Time		5		6	ns
t_{LZBE}	Byte Enable to Output in Low-Z[6, 7]	0		0		ns
t_{HZBE}	Byte Disable to Output in High-Z[6, 7, 8]		5		6	ns
t_{PU}	Chip Enable to Power-up Time[6]	0		0		ns
t_{PD}	Chip Disable to Power-down Time[6]		10		12	ns
WRITE CYCLE						
t_{WC}	WRITE Cycle Time	10		12		ns
t_{CW}	Chip Enable to End of Write	8		8		ns
t_{AW}	Address Valid to End of Write, with $\overline{OE}$ HIGH	8		8		ns
t_{AS}	Address Set-up Time	0		0		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{WP2}	WRITE Pulse Width	10		10		ns
t_{WP1}	WRITE Pulse Width, with $\overline{OE}$ HIGH	8		8		ns
t_{DS}	Data Set-up Time	5		6		ns
t_{DH}	Data Hold Time	0		0		ns
t_{LZWE}	Write Disable to Output in Low-Z[6, 7]	3		4		ns
t_{HZWE}	Write Enable to Output in High-Z[6, 7, 8]		5		6	ns
t_{BW}	Byte Enable to End of Write	8		8		ns

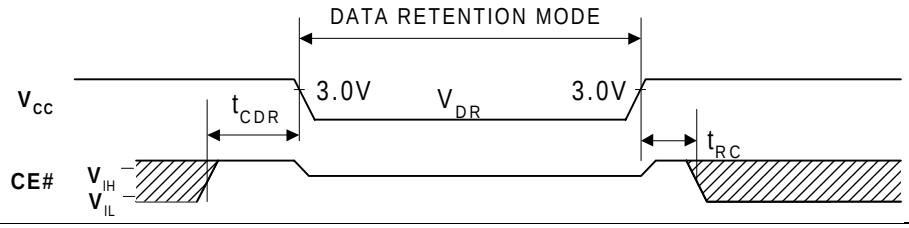
Data Retention Characteristics Over the Operating Range (For L version only)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}[9]	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$; all other inputs $\leq V_{SS} + 0.2$ or $\geq V_{CC} - 0.2$; all inputs static; f = 0	$V_{CC} = 2V$		0.2	1.6	mA
			$V_{CC} = 3V$		0.3	2.4	mA
t_{CDR}[6]	Chip Deselect to Data Retention Time			0			ns
t_R[6, 10]	Operation Recovery Time			t_{RC}			ns

Notes:

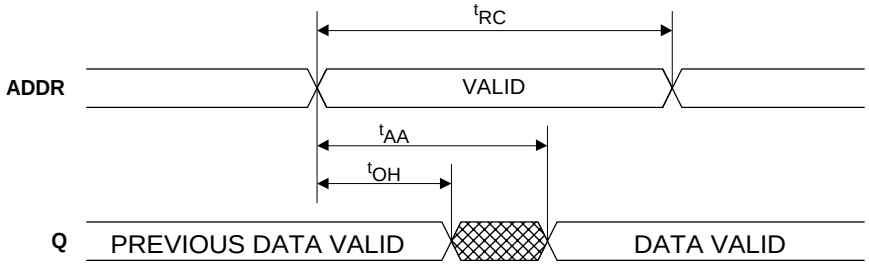
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
8. Output loading is specified with C_L=5 pF as in AC Test Loads. Transition is measured ±500mV from steady state voltage.
9. Capacitance derating applies to capacitance different from the load capacitance shown in AC Test Loads.
10. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform

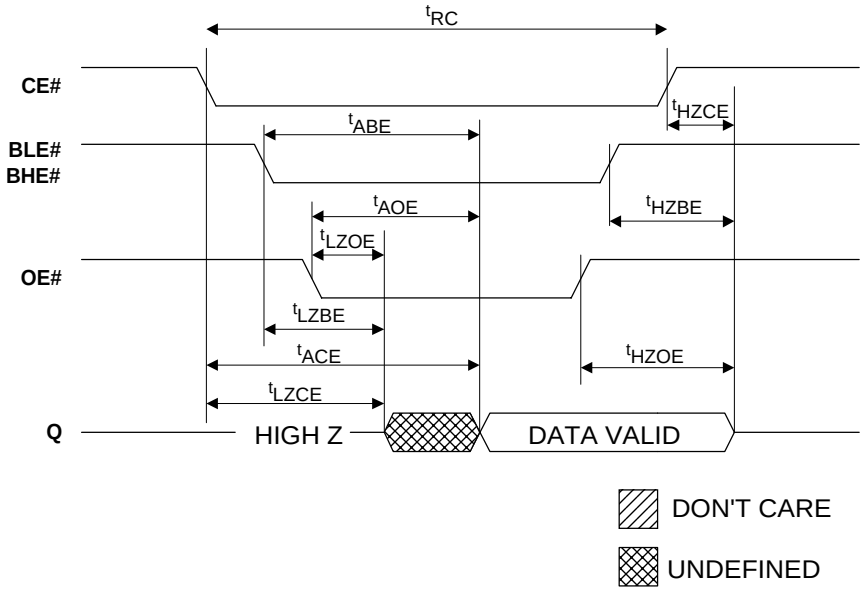


Switching Waveforms

Read Cycle No. 1[11, 12]



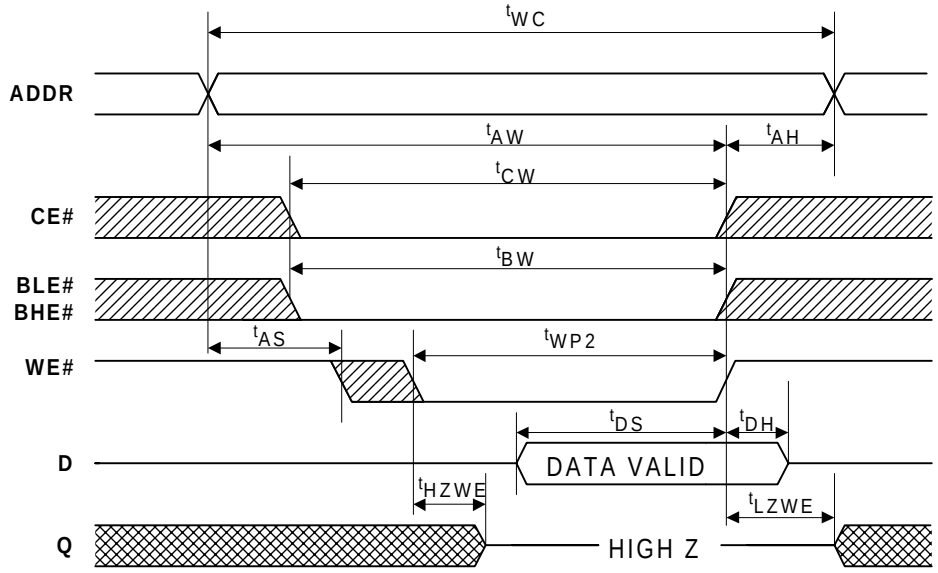
Read Cycle No. 2[7, 11, 13, 14]



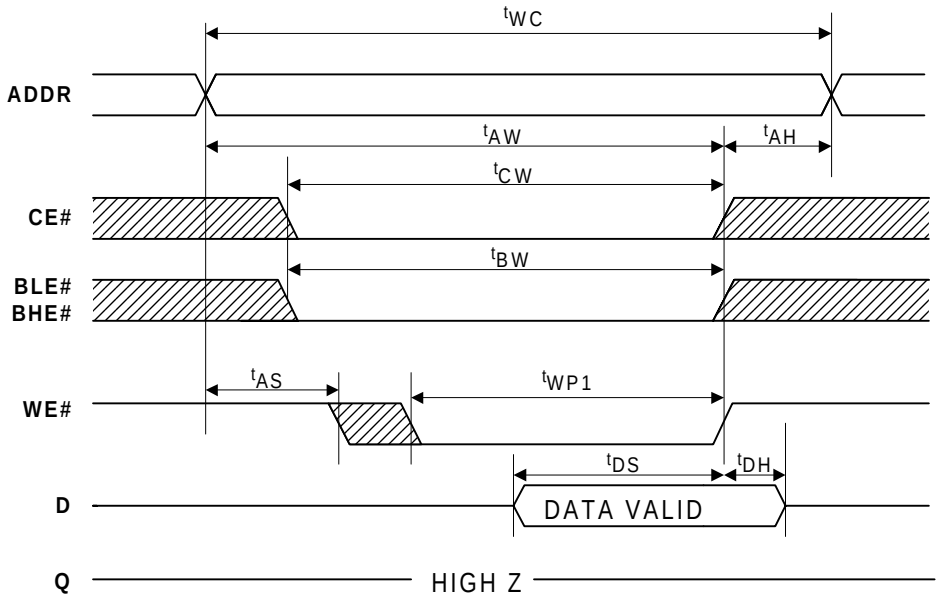
Notes:
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected. Chip Enable and Output Enables are held in their active state.
13. Address valid prior to or coincident with latest occurring chip enable.
14. Chip Enable and Write Enable can initiate and terminate a write cycle.

Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled with OE Active LOW)[9, 7, 14]

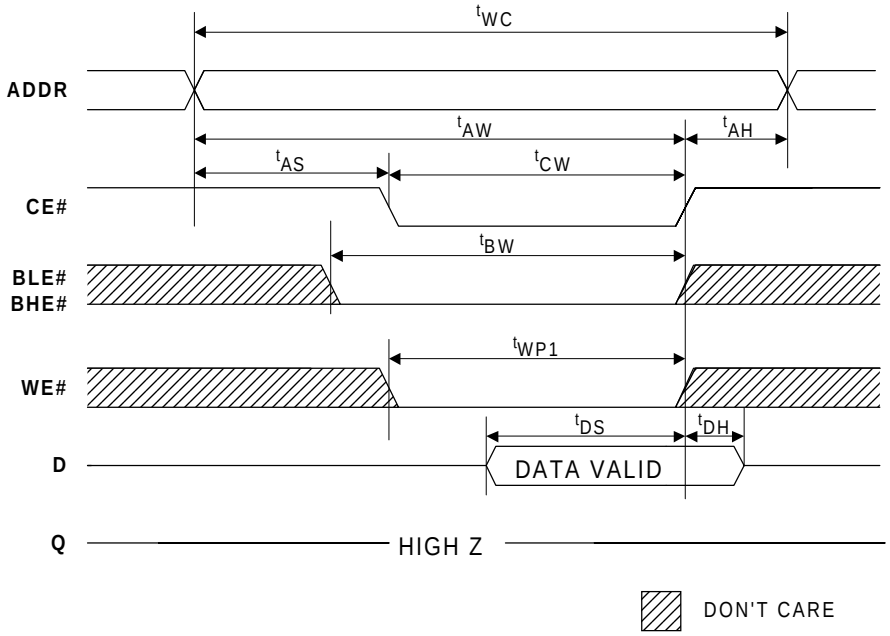


Write Cycle No. 2 (WE Controlled with OE Inactive HIGH)[9, 14]

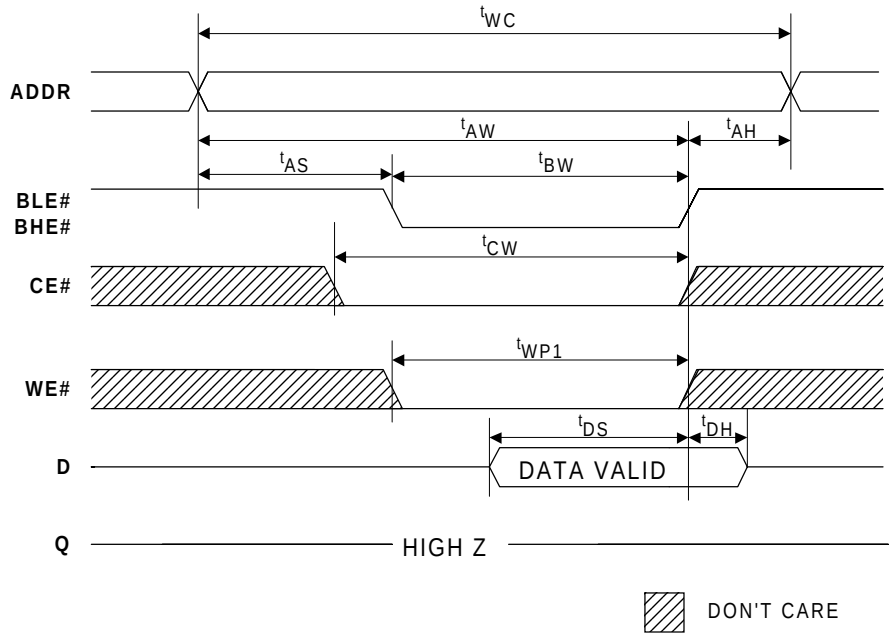


Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{CE}$ Controlled)[9, 14]



Write Cycle No. 4 (Byte Enable Controlled)[9, 14]



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1041AV33-10VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	GVT73256A16J-10C			
	CY7C1041AV33-10ZC	Z44	44-Pin TSOP II	
	GVT73256A16TS-10C			
	CY7C1041AV33L-10VC	V36	36-Lead (400-Mil) Molded SOJ	
	GVT73256A16J-10LC			
	CY7C1041AV33L-10ZC	Z44	44-Pin TSOP II	
	GVT73256A16TS-10LC			
12	CY7C1041AV33-12VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	GVT73256A16J-12C			
	CY7C1041AV33-12ZC	Z44	44-Pin TSOP II	
	GVT73256A16TS-12C			
	CY7C1041AV33L-12VC	V36	36-Lead (400-Mil) Molded SOJ	
	GVT73256A16J-12LC			
	CY7C1041AV33L-12ZC	Z44	44-Pin TSOP II	
	GVT73256A16TS-12LC			

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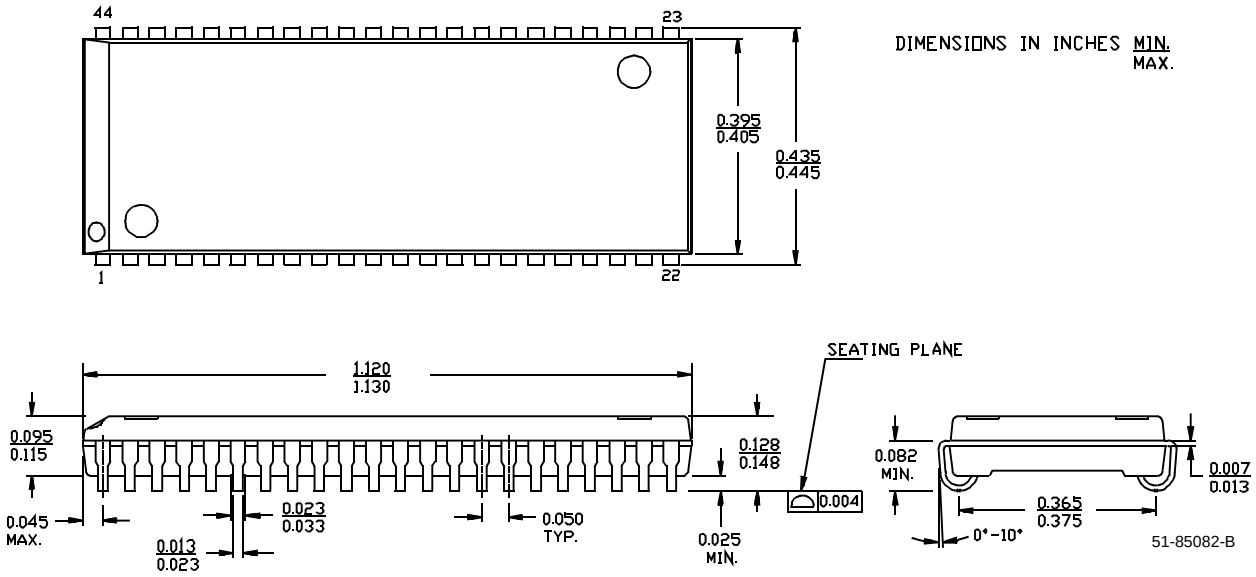
Package Diagrams

44-Lead (400-Mil) Molded SOJ V34



Package Diagrams (continued)

44-Pin TSOP II Z44