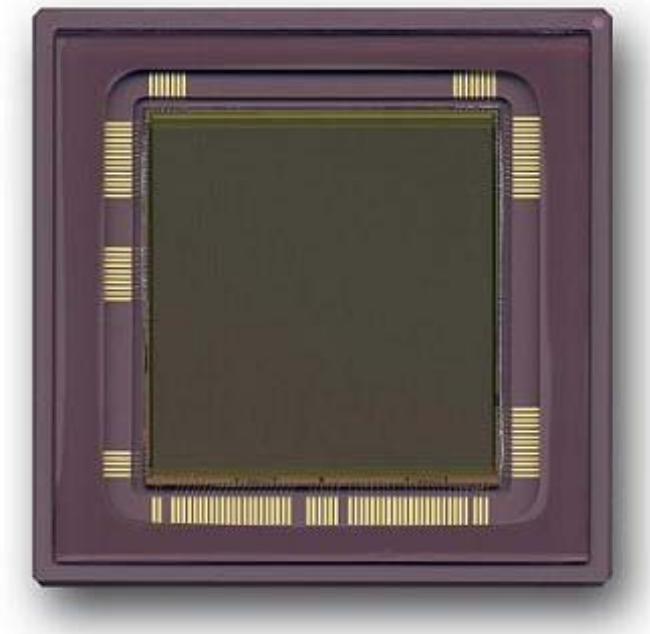
LUPA-4000

4M Pixel CMOS Image Sensor



Preamble

Overview

This document describes the interfacing and the driving of the LUPA-4000 image sensor. This 4 mega-pixel CMOS active pixel sensor features synchronous shutter and a maximal frame-rate of 15 fps in full resolution. The readout speed can be boosted by means of sub sampling and windowed Region Of Interest (ROI) readout. High dynamic range scenes can be captured using the double and multiple slope functionality.

The sensor can be used with one or two outputs. Two on chip 10-bit ADC's can be used to convert the analog data to a 10-bit digital word stream. The sensor uses a 3-wire Serial-Parallel (SPI) interface. It is housed in a 127-pin ceramic PGA package.

This data sheet allows the user to develop a camera-system based on the described timing and interfacing.

Main features

The main features of the image sensor are identified as:

- 2048 x 2048 active pixels (4M pixel resolution)
- 12 μm^2 square pixels (based on the high-fill factor active pixel sensor technology of FillFactory (US patent No. 6,225,670 and others))
- Peak QE x FF of 37.50%
- Optical format: 24,6 mm x 24,6 mm
- Pixel rate of 66 MHz using a 33 MHz system clock
- Optical dynamic range: 66 dB (2000:1) in single slope operation and up to 90 dB in multiple slope operation
- 2 On-chip 10 bit, 33 MSamples/s ADC
- Full snapshot shutter
- Random programmable windowing and sub-sampling modes
- 127-pin PGA package
- Binning (Voltage averaging in X-direction)
- Programmable read out direction (X and Y)

Part Number and ordering information

Name	Package	Mono-chrome/color
CYIL1SM4000AA-GDC	127 pin ceramic PGA	Monochrome

The LUPA-4000 is also available in color or monochrome without the cover glass. Please contact Cypress for more information.

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Specifications

General specifications

Table 1. General specifications

Parameter	Specification	Remarks
Pixel architecture	6T-pixel	Based on the high fill-factor active pixel sensor technology of FillFactory
Pixel size	12 µm x 12 µm	The resolution and pixel size results in a 24,6 mm x 24,6 mm optical active area.
Resolution	2048 x 2048	
Pixel rate	66 MHz	Using a 33 MHz system clock and 1 or 2 parallel outputs.
Shutter type	Pipelined snapshot shutter	Full snapshot shutter (integration during read out is possible).
Full frame rate	15 frames/second	Frame rate increase possible with ROI read out and/or sub sampling.

Electro-optical specifications

Overview

Table 2. Electro-optical specifications

Parameter	Specification	Remarks
FPN	<1.25% RMS	of max. output swing
PRNU	<2.5% RMS	at 25% and 75% (% of the signal)
Conversion gain	13.5 uV/electron	@ output (measured).
Output signal amplitude	1V	Converted by 2 on-chip 10-bit ADC's in 2x10 parallel digital outputs. Or to be used with external ADC's
Saturation charge	80.000 e-	
Sensitivity	2090 V.m2/W.s	Average white light.
	11.61 V/lux.s	Visible band only (180 lx = 1 W/m2).
Peak QE * FF Peak SR * FF	37.5% 0.19 A/W	Average QE*FF = 35%. Average SR*FF = 0.15 A/W. See spectral response curve.
Dark current (@ 21 °C)	<140 mV/s or 10000 e-/s	
Noise electrons	< 40 e-	
S/N ratio	2000:1	66 dB.
Spectral sensitivity range	400 - 1000 nm	
Parasitic sensitivity	< 1/5000	I.e. sensitivity of the storage node during read out (after integration).
MTF	64%	
Power dissipation	<200 mWatt	Typical (without ADC's).

Spectral response curve

Figure 1. Spectral response curve

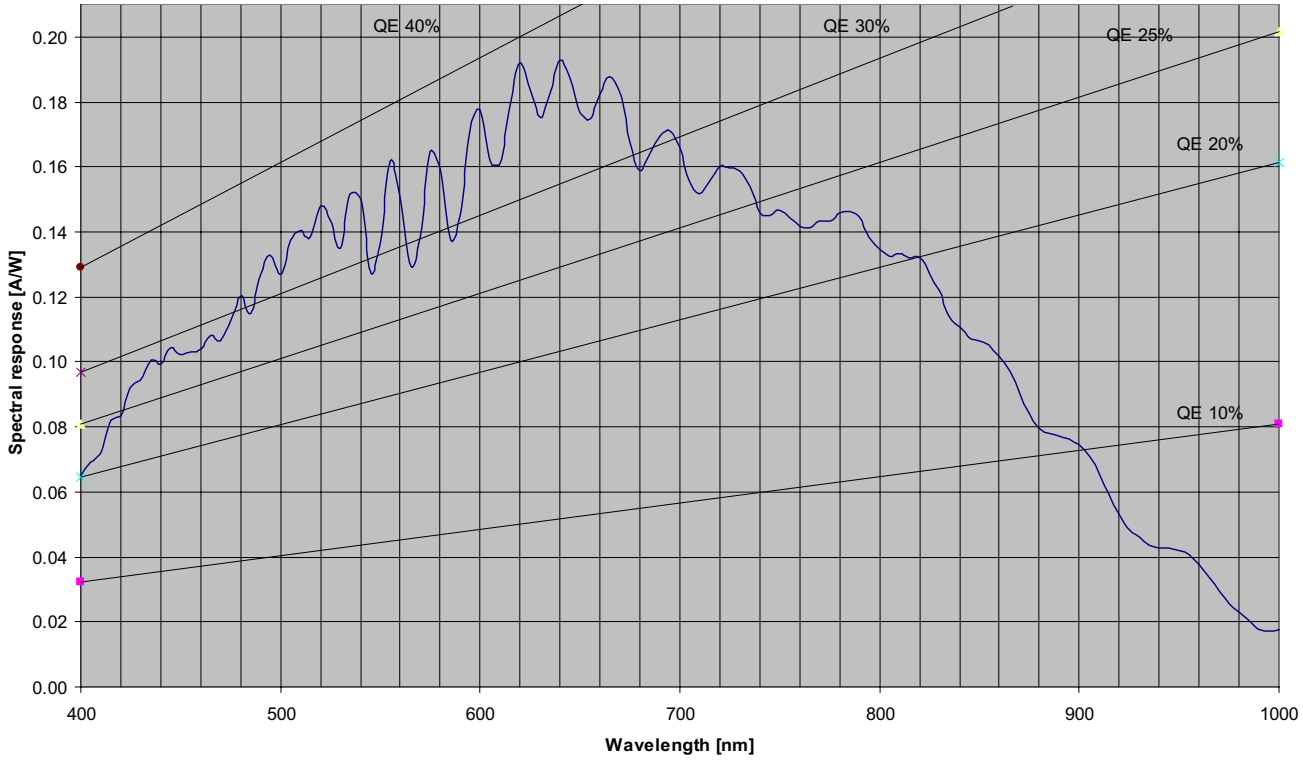


Figure 1 shows the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, e.g. interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is 37.5% approximately between 500 and 700 nm. In view of a fill factor of 60%, the QE is thus larger than 60% between 500 and 700 nm.

Photo-voltaic response curve

Figure 2. Photo-voltaic response curve

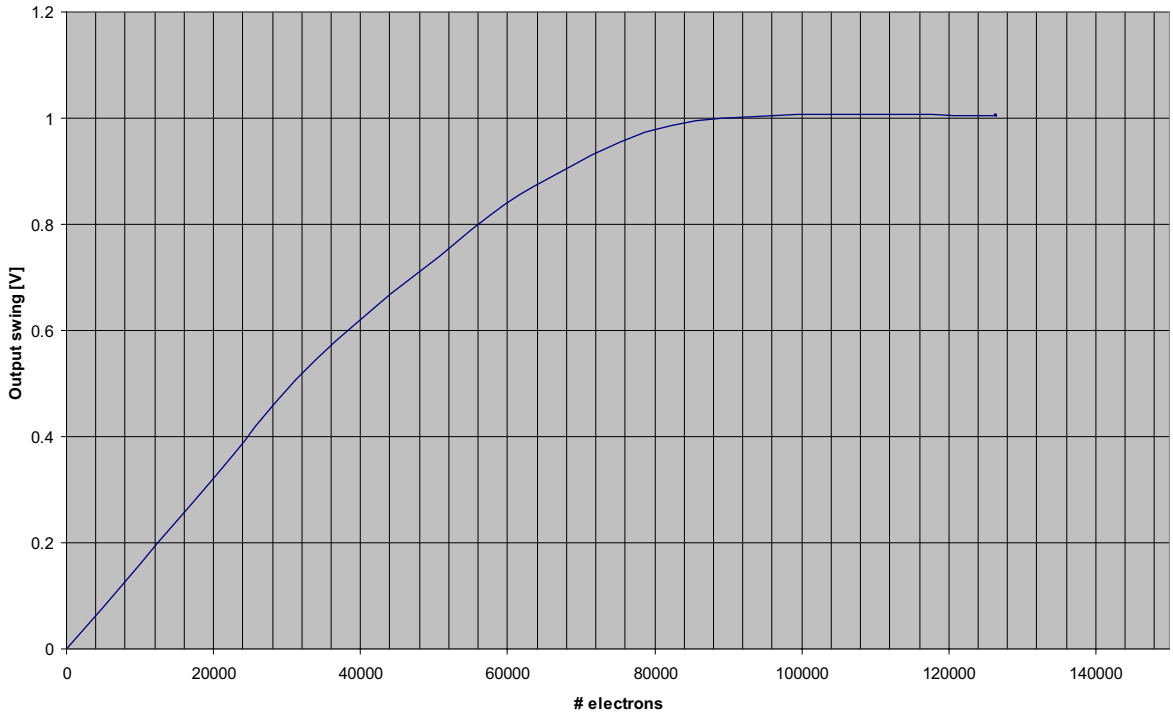


Figure 2 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The resulting voltage-electron curve is independent of any parameters. The voltage to electrons conversion gain is 13.5 µV/electron.

Note that the upper part of the curve (near saturation) is actually a logarithmic response.

Features and general specifications

Table 3. Features and general specifications

Feature	Specification/Description
Electronic shutter type	Full snapshot shutter (integration during read out is possible).
Windowing (ROI)	Randomly programmable ROI read out.
Sub-sampling and binning modes	2:1 subsampling and voltage averaging is possible (only in the X-direction).
Read out direction	Read out direction can be reversed in X and Y.
Extended dynamic range	Multiple slope (up to 90 dB optical dynamic range).
Analog output	The output rate of 66 Mpixels/s can be achieved with either 1 or 2 analog outputs.
Digital output	2 on-chip 10-bit ADC's @ 33 Msamples/s.
Supply voltage VDD	Nominal 2.5V (some supplies require 3.3V).
Logic levels	3.3V.
Operational temperature range	0°C to 60°C; with degradation of dark current.
Interface	Serial-to Parallel Interface (SPI).
Package	127 pin PGA package
Power dissipation	<200 mW
Mass	<100g

Table 3. Features and general specifications (continued)

Feature	Specification/Description
Output amplifiers	Differential
External output load	R > 10 kΩ C < 20 pF (<10 pF is advised)
Number of outputs	1 at 66 Mpixels/sec 2 at 33 Mpixels/sec

Electrical specifications

Absolute maximum ratings

VDD DC supply voltage -0.5 to 4.5 V

V_{IN} DC input voltage -0.5 to 3.8 V

V_{OUT} DC output voltage -0.5 to 3.8 V

I_{IO} DC current drain per pin; any single input or output. ± 50 mA

T_L Lead temperature (5 seconds soldering). 350 °C

- Absolute Ratings are those values beyond which damage to the device may occur.
- VDD = VDDD = VDDA (VDDD is supply to digital circuit, VDDA to analog circuit).

Recommended operating conditions

Table 4. Recommended operation conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vaa	Power supply column read out module		2.5		V
Va3	Power supply column read out module		3.3	3.3	V
Vdd	Power supply digital modules		2.5		V
Voo	Power supply output stages		2.5		V
Vres	Power supply reset drivers	2.5	3.5	3.8	V
Vres_ds	Power supply multiple slope reset driver	2.0	2.5	3.3	V
Vmem_h	Power supply memory element (high level)	2.5	3.3	3.5	V
Vmem_l	Power supply memory element (low level)	2.0	2.6	3.0	V
Vpix	Power supply pixel array	2.0	2.6	3.3	V
Vpre_l	Power supply for Precharge off-state	–0.4	0	0	V
T_A	Commercial operating temperature.	0	30	60	°C

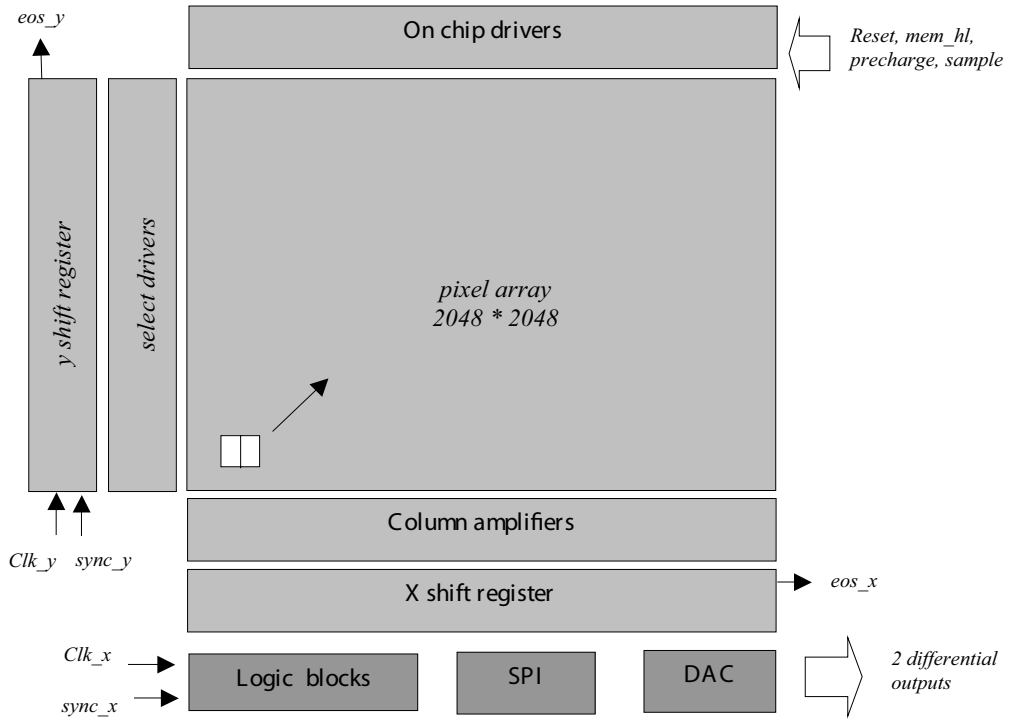
Notes
1. All parameters are characterized for DC conditions after thermal equilibrium has been established.
2. Unused inputs must always be tied to an appropriate logic level, e.g. either VDD or GND.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.

Sensor architecture

A schematic drawing of the architecture is given in the block diagram below. The image core consists of a pixel array, one X- and two Y-addressing registers (only one drawn), pixel array drivers and column amplifiers. The image sensor of 2048 * 2048 pixels is read out in progressive scan. One or two output amplifiers read out the image sensor. The output amplifiers are working at 66 MHz pixel rate nominal speed or each at 33 MHz pixel rate in case the 2 output amplifiers are used to read out the imager. The complete image sensor has been designed for operation up to 66 MHz.

The structure allows having a programmable addressing in the x-direction in steps of 2 and in the y-direction in steps of 2 (only even start addresses in X- and Y-direction are possible). The starting point of the address is uploadable by means of the Serial-Parallel Interface (SPI)

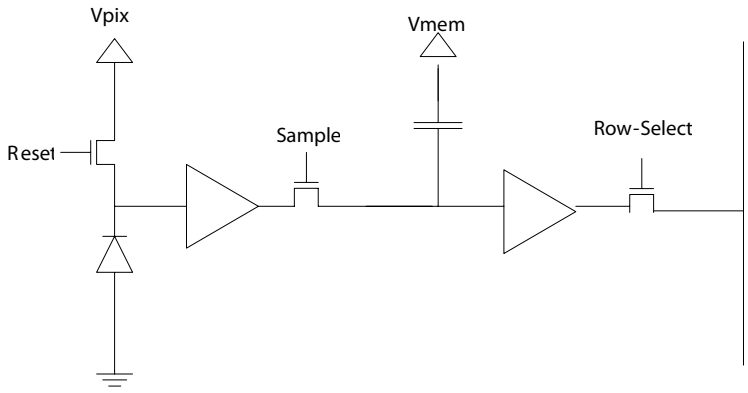
Figure 3. Block diagram of the image sensor



The 6-T pixel

To obtain the global shutter feature combined with a high sensitivity and good Parasitic Light Sensitivity (PLS), the pixel architecture given in the figure below is implemented.

Figure 4. 6T-pixel architecture



This pixel architecture is designed in a 12 * 12 μm^2 pixel pitch. The pixel is designed to meet the specifications as described in *Table 1*, *Table 2*, and *Table 3*.

Frame rate and windowing

Frame rate

To obtain a frame rate a 15 frames/sec, one needs 1 output amplifier, working at 66 MHz pixel rate or 2 output amplifiers working at 33 MHz each (assuming a Row Overhead Time (ROT) of 200 nsec).

The frame period of the LUPA-4000 sensor can be calculated as follows:

Frame period = FOT + (Nr. Lines * (ROT + pixel period * Nr. Pixels)

with: FOT: Frame Overhead Time = 5 μs.

Nr. Lines: Number of Lines read out each frame (Y).

Nr. Pixels: Number of pixels read out each line (X).

ROT: Row Overhead Time = 200 ns (nominal; can be further reduced).

Pixel period: 1/66 MHz = 15.15 ns.

Example read out of the full resolution at nominal speed (66 MHz pixel rate):

Frame period = 5 us + (2048 * (200 ns + 15.15 ns * 2048) = 64 ms => 15 fps.

ROI read out (windowing)

Windowing can easily be achieved by a serial-parallel uploadable interface in which the starting point of the x- and y-address is uploaded. This downloaded starting point initiates the shift register in the x- and y- direction triggered by the Sync_x and Sync_y pulse. The minimum step size for the x-address and the y-address is 2 (only even start addresses can be chosen). The size of both address registers is 10 bits. When for instance the addresses 0000000001 and 0000000001 are uploaded, the readout will start at line 2 and column 2.

Table 5. Frame rate as function of ROI read out and/or sub sampling

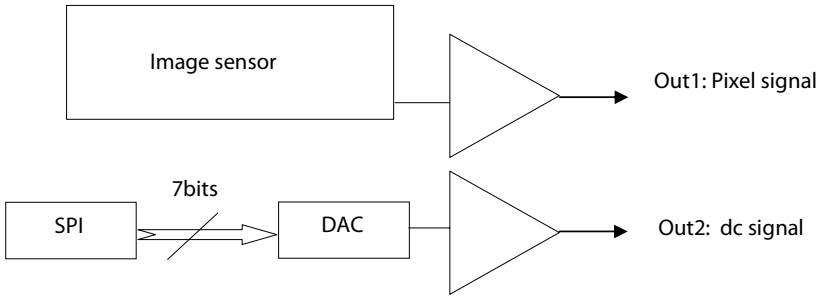
Image Resolution (X*Y)	Frame rate [frames/s]	Frame readout time [ms]	Comment
2048 x 2048	15	67	Full resolution.
1024 x 2048	31	32	Subsample in X-direction.
1024 x 1024	62	16	ROI read out.
640 x 480	210	4.7	ROI read out.

Output amplifier

1 output amplifier working at 66 Mpixels/sec is required to bring the whole pixel array of 2048 by 2048 pixels at the required frame rate to the outside world. A second output stage is also foreseen to convert the analog data on-chip by 2 10-bit ADC's each working at 33 MHz. By having a second output stage working in parallel, the pixel rate can be more relaxed to 33 MHz for both output amplifiers. Using only one output-stage, the output signal will be the result of multiplexing between the 2 internal buses. When using 2 output-stages, both outputs will be in phase.

Each output-stage has 2 outputs. One output is the pixel signal; the second output is a DC signal which offset can be programmed using a 7-bit word. The DC signal can be used for common mode rejection between the 2 signals. The disadvantage is an increase in power dissipation however this can be reduced by setting the highest DAC voltage by means of the SPI

Figure 5. Output stage architecture.



The output voltage of Out1 will be between 1.3V (dark level) and 0.3V (white level) and depends on process variations and voltage supply settings. The output voltage of Out2 is determined by the DAC.

Pixel array drivers

We have foreseen on this image sensor on chip drivers for the pixel array signals. Not only the driving on system level is easy and flexible, also the maximum currents applied to the sensor are controlled on chip. This means that the charging on sensor level is fixed and that the sensor cannot be overdriven from externally. In the paragraph on the timing, the operation of the on-chip drivers is explained more in detail.

Column amplifiers

The column amplifiers are designed for minimum power dissipation and minimum loss of signal for this reason multiple biasing signals are needed.

The column amplifiers also have the "voltage-averaging" feature integrated. In case of voltage averaging mode, the voltage average between 2 columns is taken and read out. In this mode only 2:1 pixels have to be read out.

To achieve the voltage-averaging mode, an additional external digital signal called "voltage-averaging" is required in combination with a bit from the SPI.

Analog to Digital Converter

The LUPA4000 has a two 10 bit flash analog digital converters running nominally at 33 Msamples/s. The ADC's are electrically separated from the image sensor. The inputs of the ADC should be tied externally to the outputs of the output amplifiers.

One ADC will sample the even columns and the other one will sample the odd columns. Although the input range of the ADC is between 1V and 2V and the output range of the analog signal is only between 0.3V and 1.3V, the analog output and digital input may be tied to each other directly. This is possible because there is an on chip level-shifter located in front of the ADC to lift up the analog signal to the ADC range.

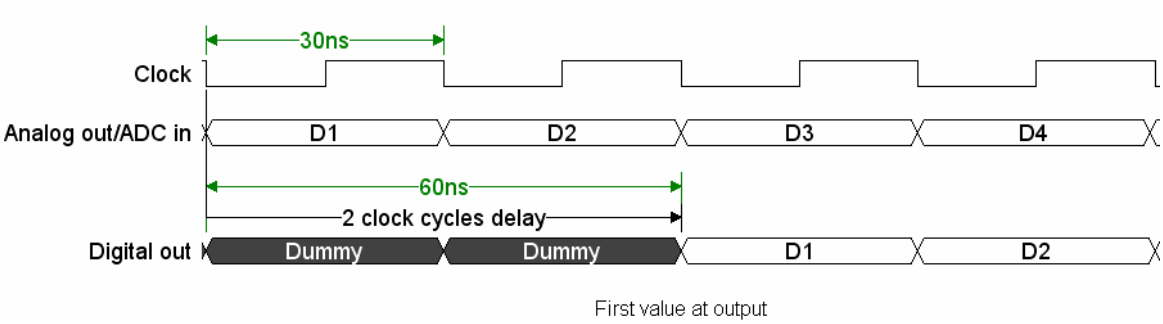
Table 6. ADC specifications

Parameter	Specification
Input range	1 - 2V (*)
Quantization	10 Bits
Nominal data rate	33 Msamples/s
DNL (linear conversion mode)	Typ. < 0.4 LSB RMS
INL (linear conversion mode)	Typ. < 3.5 LSB
Input capacitance	< 2 pF
Power dissipation @ 33 MHz	50 mW
Conversion law	Linear/Gamma-corrected

ADC timing

The ADC converts the pixel data on the falling edge of the ADC_CLOCK but it takes 2 clock cycles before this pixel data is at the output of the ADC. This pipeline delay is shown in *Figure* .

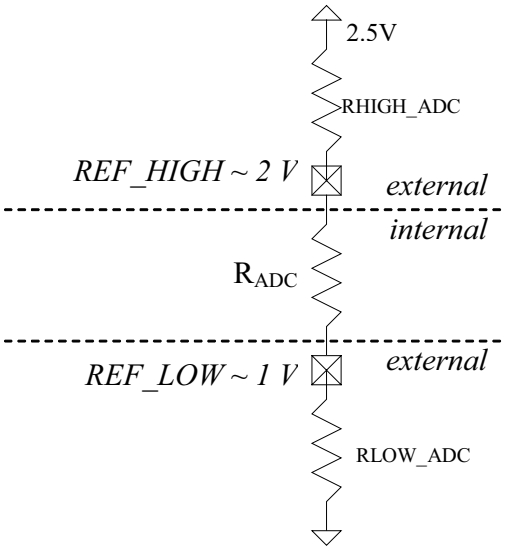
Figure 6. ADC timing



Note
4. The internal ADC range will be typ. 50 mV lower then the external applied ADC_VHIGH and ADC_VLOW voltages due to voltage drops over parasitic internal resistors in the ADC.

Setting of the ADC reference voltages

Figure 7. In- and external ADC connections



The internal resistor R_{ADC} has a value of approximately 300Ω.

This results in the values for the external resistors:

Resistor	Value (Ω)
R_{ADC_VHIGH}	75
R_{ADC}	300

Resistor	Value (Ω)
R_{ADC_VLOW}	220

The values of the resistors depend on the value of R_{ADC}. The voltage difference between ADC_VLOW and ADC_VHIGH should be at least 1.0V to assure proper working of the ADC.

Synchronous shutter

In a synchronous (snapshot) shutter light integration takes place on all pixels in parallel, although subsequent readout is sequential.

Figure 8. Synchronous shutter operation

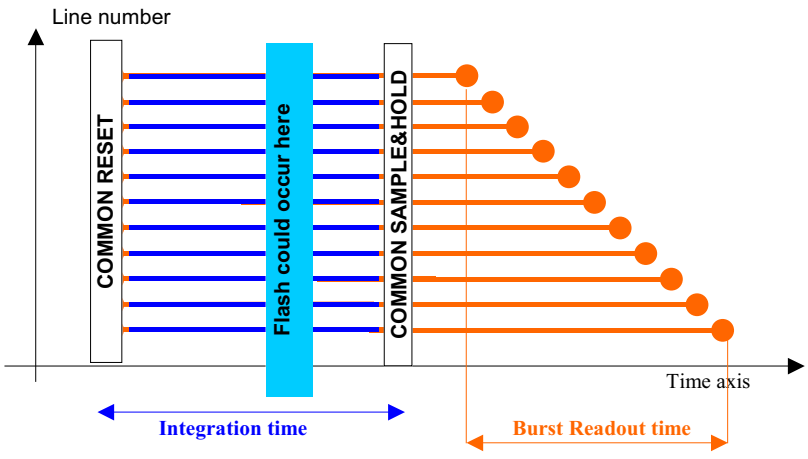
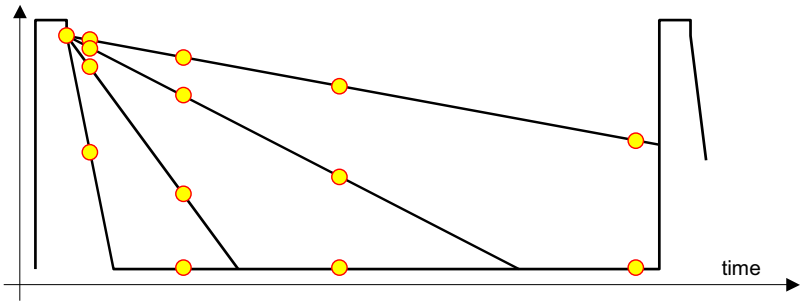


Figure 8 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and read out cycle can occur in parallel or in sequential mode. (ref. 4. Timing and read out of the image sensor)

Non-destructive readout (NDR)

The sensor can also be read out in a non-destructive way. After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels will saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, one has to use the later or latest samples.

Figure 9. Principle of non-destructive readout



Essentially an active pixel array is read multiple times, and reset only once. The external system intelligence takes care of the interpretation of the data. *Table 7* summarizes the advantages and disadvantages of non-destructive readout.

Table 7. Advantages and disadvantages of non-destructive readout.

Advantages	Disadvantages
Low noise - as it is true CDS.	System memory required to record the reset level and the intermediate samples.
High sensitivity - as the conversion capacitance is kept rather low.	Requires multiples readings of each pixel, thus higher data throughput.
High dynamic range - as the results includes signal for short and long integrations times.	Requires system level digital calculations.

Operation and signalling

One can distinguish the different signals into different groups:

- Power supplies and grounds
- Biasing and Analog signals
- Pixel array signals
- Digital signals
- Test signals

Power supplies and ground

Every module on chip, as there are: column amplifiers, output stages, digital modules, drivers has its own power supply and ground. Off chip the grounds can be combined, but not all power supplies may be combined. This results in several different power supplies, but this is required to reduce electrical cross-talk and to improve shielding, dynamic range and output swing.

On chip we have the ground lines of every module which are kept separately to improve shielding and electrical cross talk between them.

An overview of the supplies is given in *Table 8* and *Table 9*. *Table 9* summarizes the supplies related to the pixel array signals, where *Table 8* summarizes the supplies related with all other modules

Table 8. Power supplies

Name	DC Current	Max.current	Typ.	Max.	Description
Vaa	7 mA	50 mA	2.5V		Power supply column readout module.
Va3	10 mA	50 mA	3.3V	3.3V	Power supply column readout module. Should be tuneable to 3.3V max.
Vdd	1 mA	200 mA	2.5V		Power supply digital modules
Voo	20 mA	20 mA	2.5V		Power supply output stages
Vdda	1 mA	200 mA	2.5V		Analog supply of ADC circuitry
Vddd	1 mA	200 mA	2.5V		Digital supply of ADC circuitry

Table 9. Overview of the power supplies related to the pixel signals

Name	DC current	Max. current	Min.	Typ.	Max.	Description
Vres	1 mA	200 mA	2.5V	3.5V	3.8V	Power supply reset drivers.
Vres_ds	1 mA	200 mA	2.0V	2.5V	3.3V	Power supply dual slope reset drivers.
Vmem_h	1 mA	200 mA	2.5V	3.3V	3.5V	Power supply memory elements in pixel for high voltage level
Vmem_l	1 mA	200 mA	2.0V	2.5 V	3.0V	Power supply memory elements in pixel for low voltage level. Should be tuneable
Vdd	1 mA	200 mA	2.0V	2.5V	3.0V	Power supply for Sample
Vpix	12 mA	500 mA	2.0V	2.5V	3.3V	Power supply pixel array. Should be tuneable to 3.3V
Vpre_l	1 mA	200 mA	–400 mV	0V	0V	Power supply for Precharge in off-stat. May be connected to ground.

The maximum currents mentioned in *Table 8* and *Table 9* are peak currents which occur once per frame (except for Vres_ds in multiple slope mode). All power supplies should be able to deliver these currents except for Vmem_l and Vpre_l, which must be able to sink this current.

The maximum peak current for Vpix should not be higher than 500 mA. It is important to notice that no power supply filtering on chip is implemented and that noise on these power supplies can contribute immediately to the noise on the signal. Especially the voltage supplies Vpix and Vaa are important to be well noise free.

Start-up sequence

The LUPA-4000 will go in latch up (draw high current) as soon as all power supplies are turned on at the same time. The sensor will come out of latch-up and start working normally as soon as it is being clocked. A power supply with a 400 mA limit is recommended to avoid damage to the sensor. It is recommended to avoid the time that the device is in the latch-up state, so clocking of the sensor should start as soon as possible (i.e. as soon as the system is turned on).

In order to completely avoid latch-up of the image sensor, the next sequence should be taken into account:

- Apply Vdd
- Apply clocks and digital pulses to the sensor to count 2048 clocks and 2048 clock_y pulses to empty the shift registers
- Apply other supplies

Biasing and analog signals

The analog output levels that may be expected are between 0.3V for a white, saturated, pixel and 1.3V for a black pixel.

2 Output stages are foreseen, each consisting of 2 output amplifiers, resulting in 4 outputs. 1 Output amplifier is used for the analog signal resulting from the pixels. The second amplifier is used for a dc reference signal. The dc-level from the buffer is defined by a DAC, which is controlled by a 7-bit word downloaded in the SPI. Additionally, an extra bit in the SPI defines if 1 output or the 2 output stages are used.

Table 10 summarizes the biasing signals required to drive this image sensor. For optimisation reasons of the biasing of the column amplifiers with respect to power dissipation, we need several biasing resistors. This optimisation results in an increase of signal swing and dynamic range.

Table 10. Overview of bias signals

Signal	Comment	Related module	DC-level
Out_load	Connect with 60 KΩ to Voo and capacitor of 100 nF to Gnd	Output stage	0.7 V
dec_x_load	Connect with 2 MΩ to Vdd and capacitor of 100 nF to Gnd	X-addressing	0.4 V
muxbus_load	Connect with 25 KΩ to Vaa and capacitor of 100 nF to Gnd	Multiplex bus	0.8 V
nsf_load	Connect with 5 KΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	1.2 V
uni_load_fast	Connect with 10 KΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	1.2 V
uni_load	Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	0.5 V
pre_load	Connect with 3 KΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	1.4 V
col_load	Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	0.5 V
dec_y_load	Connect with 2 MΩ to Vdd and capacitor of 100 nF to Gnd	Y-addressing	0.4 V
psf_load	Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	0.5 V

Table 10. Overview of bias signals (continued)

Signal	Comment	Related module	DC-level
precharge_bias	Connect with 1kΩ to Vdd and capacitor of at least 200 nF to Gnd.	Pixel drivers	1.4V

Each biasing signal determines the operation of a corresponding module in the sense that it controls speed and dissipation. Some modules have 2 biasing resistors: one to achieve the high speed and another to minimize power dissipation.

Pixel array signals

The Pixel array of the image sensor requires digital control signals and several different power supplies. This paragraph explains the relation between the control signals and the applied supplies and the internal generated pixel array signals.

From *Figure 9* one can see that the internal generated pixel array signals are Reset, Sample, Precharge, Vmem and Row_select. These are internal generated signals derived by on chip drivers from external applied signals. Row_select is generated by the y addressing and will not be discussed in this paragraph.

The function of each of the signals is:

Reset: Resets the pixel and initiates the integration time. If reset is high than the photodiode is forced to a certain voltage, depending on Vpix, which is the pixel supply; and depending on the high level of reset signal. The higher these signals or supplies are, the higher the voltage-swing. The limitation on the high level of Reset and Vpix is 3.3V. Nevertheless, it has no sense increasing Vpix without increasing the reset level. The opposite does make sense. Additionally, it is this reset pulse that also controls the dual or multiple slope feature inside the pixel. By giving a reset pulse during integration, but not at full reset level, the photodiode is reset to a new value, only if his value is sufficient decreased due to light illumination.

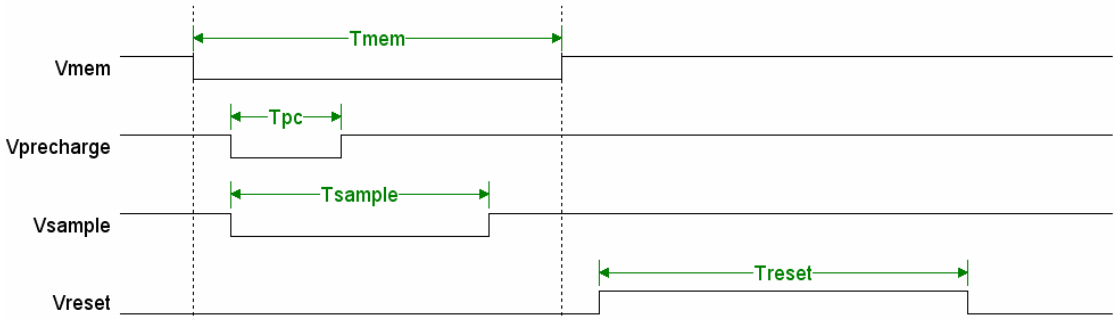
The low level of reset is 0V, but the high level is 2.5V or higher (3.3V) for the normal reset and a lower (<2.5V) level for the multiple slope reset.

Precharge: Precharge serves as a load for the first source follower in the pixel and is activated to overwrite the current information on the storage node by the new information on the photodiode. Precharge is controlled by an external digital signal between 0 and 2.5V.

Sample: Samples the photodiode information onto the memory element. This signal is also a standard digital level between 0 and 2.5V.

Vmem: this signal increases the information on the memory element with a certain offset. This way one can increase the output voltage variation. Vmem changes between Vmem_l (2.5V) and Vmem_h (3.3V).

Figure 10. Internal timing of the pixel. Levels are defined by the pixel array voltage supplies (For the correct polarities of the signals refer to *Table 11*)



The signals in *Figure 10* are generated from the on chip drivers. These on chip drivers need 2 types of signals to generate the exact type of signal. It needs digital control signals between 0 and 3.3V (internally converted to 2.5V) with normal driving capability and power supplies. The control signals are required to indicate the moment they need to occur and the power supplies indicate the level.

Vmem is made of a control signal Mem_hl and 2 supplies Vmem_h and Vmem_l. If the signal Mem_hl is the logic "0" than the internal signal Vmem is low, if Mem_hl is logic "1" the internal signal Vmem is high.

Reset is made by means of 2 control signals: Reset and Reset_ds and 2 supplies: Vres and Vres_ds. Depending on the signal that becomes active, the corresponding supply level is applied to the pixel.

Table 11 summarizes the relation between the internal and external pixel array signals.

Table 11. Overview of the in- and external pixel array signals

Internal Signal	Vlow	Vhigh	External control signal	Low DC-level	High DC-level
Precharge	0	0.45V	Precharge (AL)	Vpre_l	Controlled by bias-resistor
Sample	0	2.5V	Sample (AL)	Gnd	Vdd
Reset	0	2.5 - 3.3V	Reset (AH) & Reset_ds (AH)	Gnd	Vres & Vres_ds
Vmem	2.0- 2.5V	2.5-3.3V	Mem_hl (AL)	Vmem_l	Vmem_h

In case the dual slope operation is desired, one needs to give a second reset pulse to a lower reset level during integration. This can be done by the control signal Reset_ds and by the power supply Vres_ds that defines the level to which the pixel has to be reset.

Note that Reset is dominant over Reset_ds, which means that the high voltage level will be applied for reset, if both pulses occur at the same time.

Note that multiple slopes are possible having multiple Reset_ds pulses with a lower Vres_ds level for each pulse given within the same integration time

The rise and fall times of the internal generated signals are not very fast (200 nsec). In fact they are made rather slow to limit the maximum current through the power supply lines (Vmem_h, Vmem_l, Vres, Vres_ds, Vdd). Current limitation of those power supplies is not required. Nevertheless, it is advisable to limit the currents not higher than 400 mA.

The power supply Vmem_l must be able to sink this current because it must be able to discharge the internal capacitance from the level Vmem_h to the level Vmem_l. The external control signals should be capable of driving input capacitance of about 10 pF.

Digital signals

The digital signals control the readout of the image sensor. These signals are:

- Sync_y (AH): Starts the readout of the frame. This pulse synchronises the y-address register: active high. This signal is at the same time the end of the frame or window and determines the window width.
- Clock_y (AH): Clock of the y-register. On the rising edge of this clock, the next line is selected.
- Sync_x (AH): Starts the readout of the selected line at the address defined by the x-address register. This pulse synchronises the x-address register: active high. This signal is at the same time the end of the line and determines the window length.
- Clock_x (AH): Determines the pixel rate. A clock of 33 MHz is required to achieve a pixel rate of 66MHz.
- Spi_data (AH): the data for the SPI
- Spi_clock (AH): clock of the serial parallel interface. This clock downloads the data into the SPI register.
- Spi_load (AH): when the SPI register is uploaded, then the data will be internally available on the rising edge of SPI_load.
- Sh_kol (AL): control signal of the column readout. Is used in sample & hold mode and in binning mode.
- Norowsel (AH): Control signal of the column readout. (See timing).
- Pre_col (AL): Control signal of the column readout to reduce row blanking time.
- Voltage averaging (AH): Signal required obtaining voltage averaging of 2 pixels.

Test signals

The test structures implemented in this image sensor are:

- Array of pixels (6*12) which outputs are tied together: used for spectral response measurement.
- Temperature diode (2): Apply a forward current of 10-100 µA and measure the voltage V_T of the diode. V_T varies linear with the temperature (V_T decreases with approximately 1,6 mV/°C).
- End of scan pulses (do not use to trigger other signals):
  - Eos_x: end of scan signal: is an output signal, indicating when the end of the line is reached. Is not generated when doing windowing.
  - Eos_y: end of scan signal: is an output signal, indicating when the end of the frame is reached. Is not generated when doing windowing.
  - Eos_spi: output signal of the SPI to check if the data is transferred correctly through the SPI.

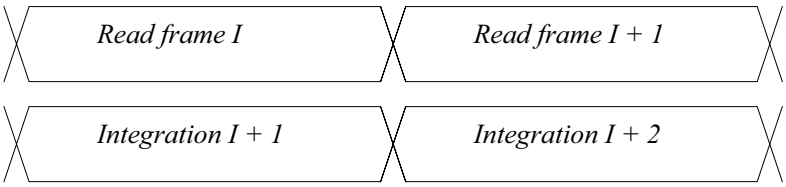
Notes
5. AH: Active High
6. AL: Active Low

Timing and read out of the image sensor

The timing of the LUPA-4000 sensor consists of 2 parts. The first part is related with the control of the pixels, the integration time and the signal level. The second part is related with the readout of the image sensor. As this image sensor is able for full synchronous shutter, integration time and readout can be in parallel or sequential.

In the parallel mode the integration time of the frame I is ongoing during readout of frame I-1. *Figure 11* shows this parallel timing structure

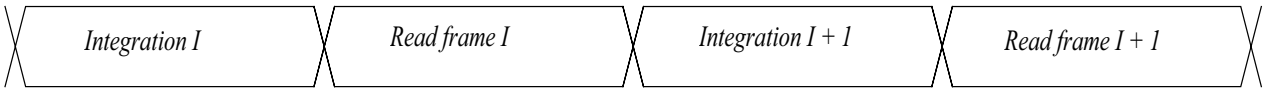
Figure 11. Integration and read out in parallel



The control of the readout of the frame and of the integration time are independent of each other with the only exception that the end of the integration time from frame I+1 is the beginning of the readout of frame I+1.

The LUPA-4000 sensor also can be used in sequential mode (triggered snapshot mode) where readout and integration will be sequentially. *Figure 12* shows this sequential timing sequence.

Figure 12. Integration and readout sequentially

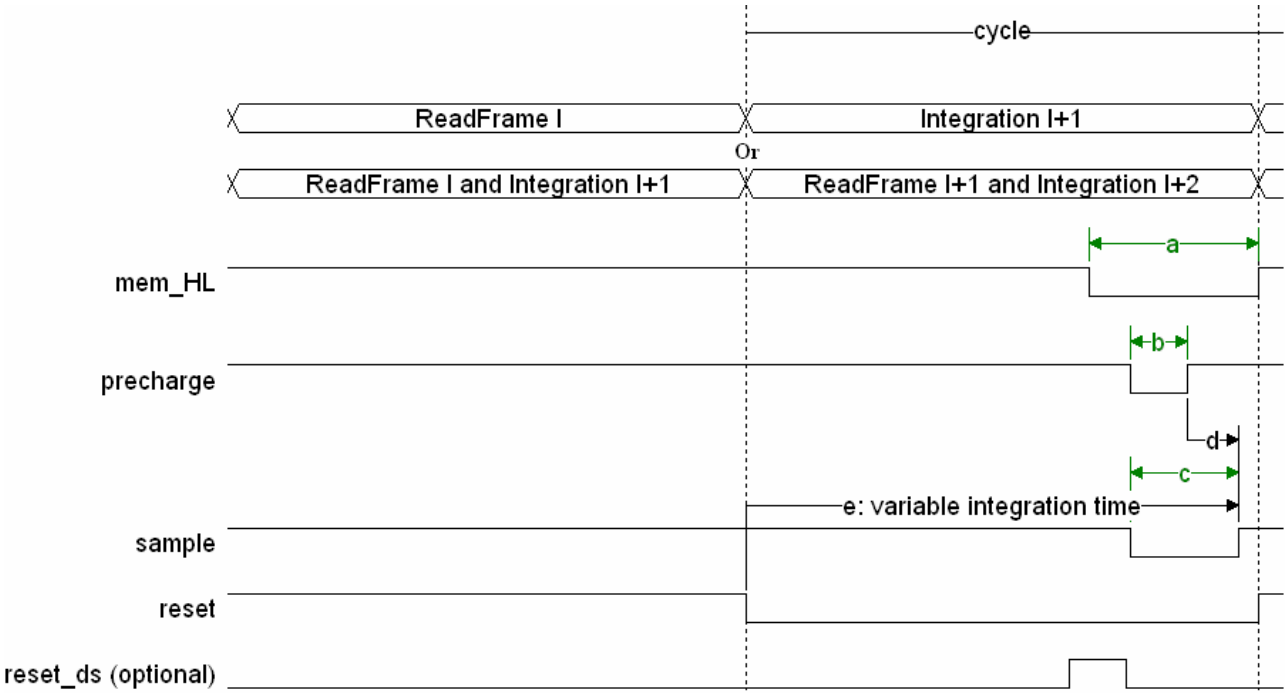


Timing of the pixel array

The first part of the timing is related with the timing of the pixel array. This implies the control of the integration time, the synchronous shutter operation and the sampling of the pixel information onto the memory element inside each pixel. The signals needed for this control are described in the previous paragraph 3.9 and in *Figure 10*.

Figure shows the external applied signals required to control the pixel array. At the end of the integration time from frame I+1, the signals Mem_hl, Precharge and Sample have to be given. The reset signal controls the integration time, which is defined as the time between the falling edge of reset and the rising edge of sample.

Figure 13. Timing of the pixel array: The integration time is determined by the falling edge of the reset pulse. The longer the pulse is high, the shorter the integration time. At the end of the integration time, the information has to be stored onto the memory element for readout.



Timing specifications for each signal are:

Table 12. Timing specifications

Symbol	Name	Value
a	Mem_HL	5 - 8,2 µsec
b	Precharge	3 - 6 µsec
c	Sample	5 - 8 µsec
d	Precharge-Sample	> 2 µsec
e	Integration time	> 1 µsec

- Falling edge of Precharge is equal or later than falling edge of Vmem.
- Sample is overlapping with precharge.
- Rising edge of Vmem is more than 200 nsec after rising edge of Sample.
- Rising edge of reset is equal or later than rising edge of Vmem

The timing of the pixel array is straightforward. Before the frame is read, the information on the photodiode needs to be stored onto the memory element inside the pixels. This is done by means of the signals Mem_hl, Precharge and Sample. When precharge is activated it serves as a load for the first source follower in the pixel. Sample stores the photodiode information onto the memory element. Mem_hl pumps up this value to reduce the loss of signal in the pixel and this signal must be the envelop of Precharge and Sample. After Mem_hl is high again, the readout of the pixel array can start. The frame blanking time or frame overhead time is thus the time that Mem_hl is low, which is about 5 µsec. Once the readout starts, the photodiodes can all be initialised by reset for the next integration time. The minimal integration time is the minimal time between the falling edge of reset and the rising edge of sample. Keeping the slow fall times of the corresponding internal generated signals in mind, the minimal integration time is about 2 µsec.

An additional reset pulse of minimum 2 μsec can be given during integration by asserting Reset_ds to implement the double slope integration mode.

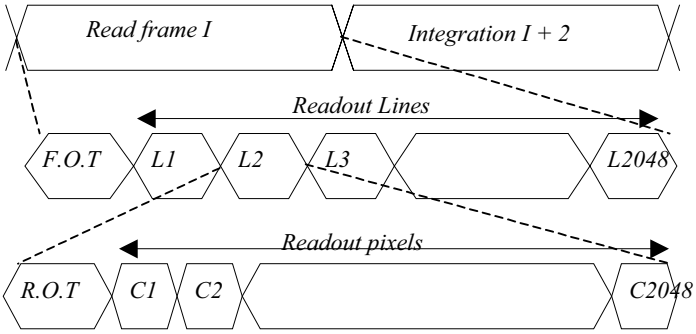
Read out of the image sensor

As soon as the information of the pixels is stored in to the memory element of each pixel, this information can be readout sequentially. As seen in the previous section, integration and readout can also be done in parallel.

The readout timing is straightforward and is basically controlled by means of sync and clock pulses.

Figure 14 shows the top level concept of this timing. The readout of a frame consists of the frame overhead time, the selection of the lines sequentially and the readout of the pixels of the selected line

Figure 14. Readout of the image sensor. F.O.T: Frame overhead time. R.O.T: Row overhead time. L: selection of line, C: Selection of column



The readout of an image consists of the FOT (Frame overhead time) and the sequential selection of all pixels. The FOT is the overhead time between 2 frames to transfer the information on the photodiode to the memory elements. From *Figure 13* it should be clear that this time is the time that Mem_hl is low (typically 5 μs). After the FOT the information is stored into the memory elements and a sequential selection of rows and columns makes sure the frame is read.

X- and Y- addressing

To readout a frame the lines are selected sequentially. *Figure 15* gives the timing to select the lines sequentially. This is done by means of a Clock_y and a Sync_y signal. The Sync_y signals synchronises the y-addressing and initialises the y-address selection registers. The start address is the address downloaded in the SPI multiplied by 2.

On the rising edge of Clock_y the next line is selected. The Sync_y signal is dominant and from the moment it occurs the y-address registers are initialised. If a Sync_y pulse is given before the end of the frame is reached, only a part of the frame will be read. To obtain a correct initialisation Sync_y must contain at least 1 rising edge of Clock_y when it is active.

Figure 15. X- and Y-addressing

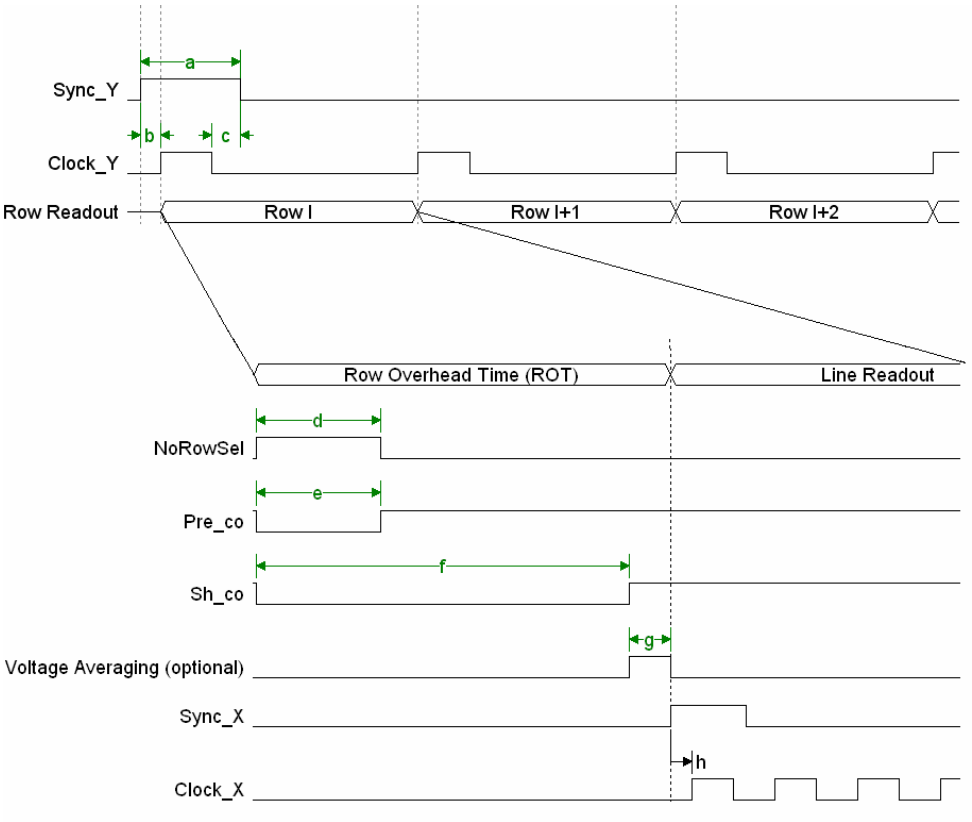


Table 13. Read-out timing specifications

Symbol	Name	Value
a	Sync_Y	>20 ns
b	Sync_Y-Clock_Y	>0 ns
c	Clock_Y-Sync_Y	>0 ns
d	NoRowSel	>50 ns
e	Pre_col	>50 ns
f	Sh_col	200 ns (more information on this timing can be found in section 4.2.2.a)
g	Voltage averaging	>20 ns
h	Sync_X-Clock_X	>0 ns

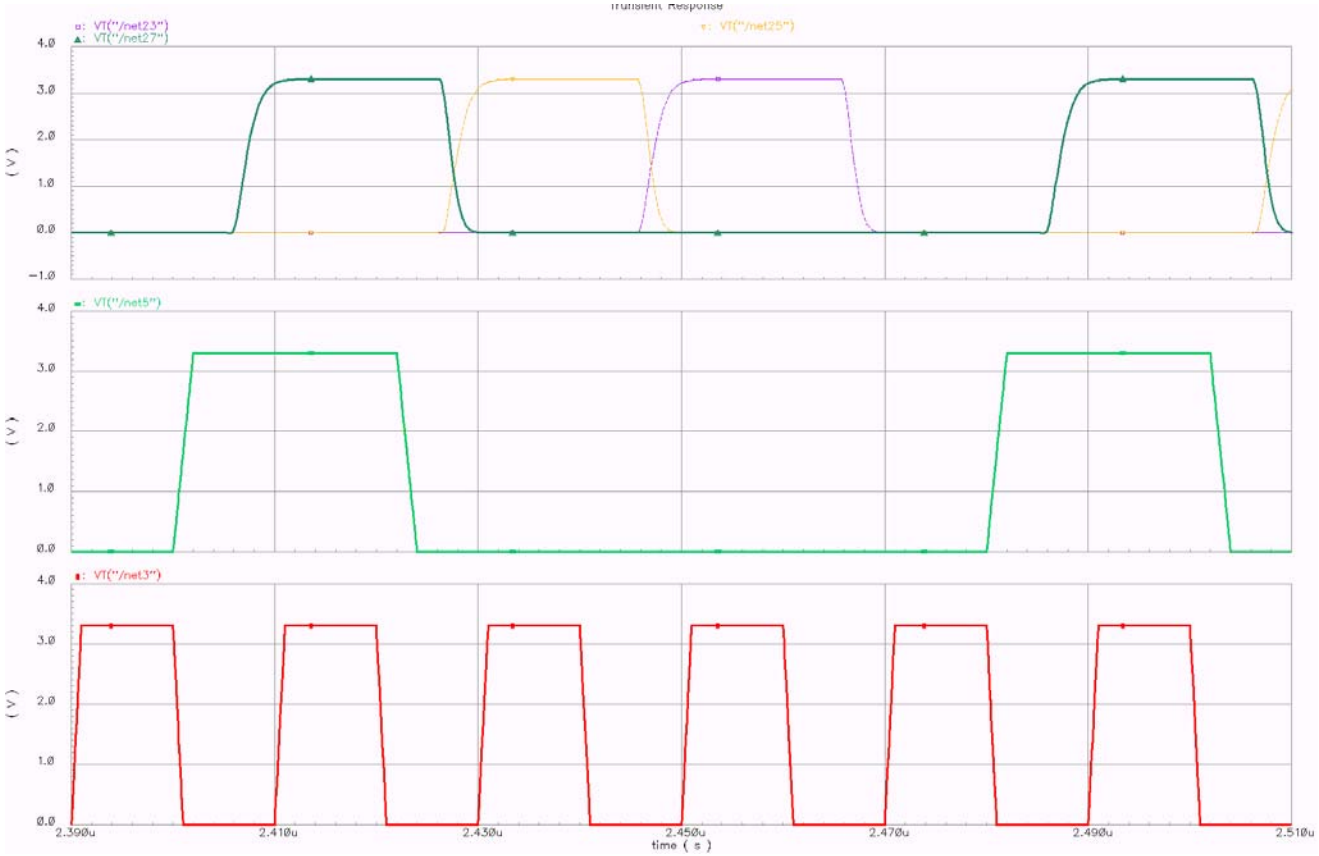
As soon as a new line is selected, it has to be read out by the output amplifiers. Before the pixels of the selected line can be multiplexed onto the output amplifiers, one has to wait a certain time, indicated as the ROT or Row overhead time shown in *Figure 15*. This is the time to get the data stable from the pixels to the output bus before the output stages. This ROT is in fact lost time and rather critical in a high-speed sensor. Different timings to reduce this ROT are explained in next paragraph.

During the selection of 1 line, 2048 pixels are selected. These 2048 pixels have to be readout by 1 (or 2) output amplifier.

Please note that the pixel rate is the double frequency of the Clock_x frequency. To obtain a pixel rate of 66 MHz, one needs to apply a pixel clock Clock_x of 33MHz. When only 1 analog output is used 2 pixels are output every Clock_x period. When Clock_x is high, the first pixel is selected, when Clock_x is low, the next pixel is selected. Consequently, during 1 complete period of Clock_x 2 pixels are readout by the output amplifier.

If 2 analog outputs are used each Clock-X period 1 pixel is presented at each output.

Figure 16. X-addressing. From bottom to top: Clock_x, Sync_x, internal selection pixel 1&2, internal selection pixel 3&4, internal selection pixel 5 & 6



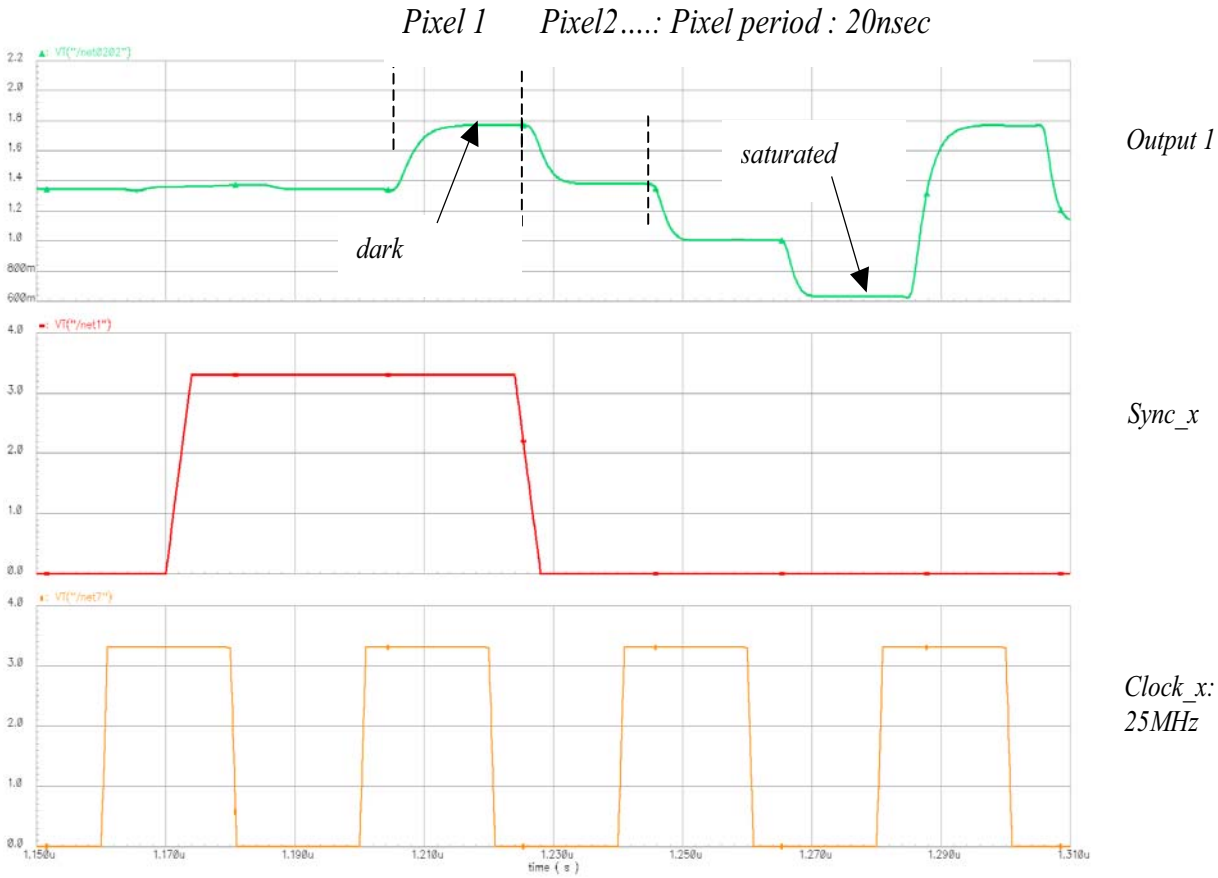
The first pixel that is selected is the x-address downloaded in the SPI. The starting address is the number downloaded into the SPI, multiplied with 2.

Windowing is achieved by a starting address downloaded in the SPI and the size of the window. In the x-direction, the size is determined by the moment a new Clock_y is given. In the y-direction, the sync_y pulse determines the size. Consequently, the best way to obtain a certain window is by using an internal counter in the controller.

Figure 16 is the simulation result after extraction of the layout module from a different sensor to show the principle. In this figure the pixel clock has a frequency of 50 MHz, which would result in a pixel rate of 100 Msamples/sec.

Figure shows the relation between the applied Clock_x and the output signal.

Figure 17. Output signal related to Clock_x signal. From bottom to top: Clock_x, Sync_x and output. The output level before the first pixel is the level of the last pixel of previous line



As soon as Sync_x is high and 1 rising edge of Clock_x occurs, the pixels are brought to the analog outputs. This is again the simulation result of a comparable sensor to show the principle.

Please note there is a time difference between the clock edge and the moment the data is seen at the output. As this time difference is very difficult to predict in advance, it is advisable to have the ADC sampling clock flexible to set an optimal Add sampling point. The time differences can easily vary between 5 - 15 nsec and have to be tested on the real devices.

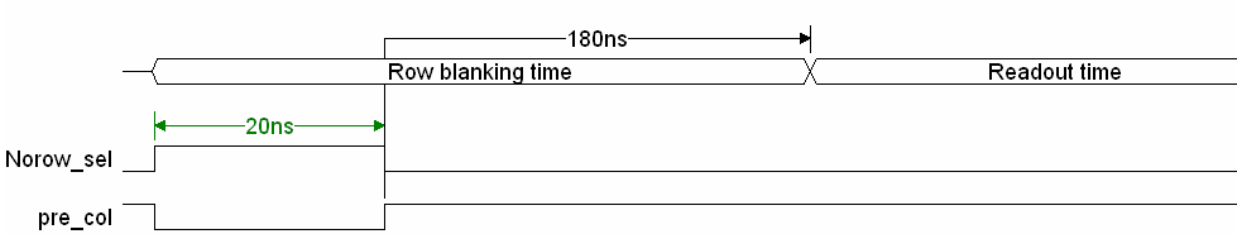
Reduced Row Overhead Time timing

The row overhead time is the time between the selection of lines that one has to wait to get the data stable at the column amplifiers.

This row overhead time is a loss in time, which should be reduced as much as possible.

Standard timing (200 ns)

Figure 18. Standard timing for the R.O.T. Only pre_col and Norowsel control signals are required



In this case the control signals Norowsel and pre_col are made active for about 20 nsec from the moment the next line is selected. The time these pulses have to be active is related with the biasing resistance Pre_load. The lower this resistance, the shorter the pulse duration of Norowsel and pre_col may be. After these pulses are given, one has to wait for at least 180 nsec before the first pixels can be sampled. For this mode Sh_col must be made active (low) all the time.

Back-up timing (ROT =100-200 ns)

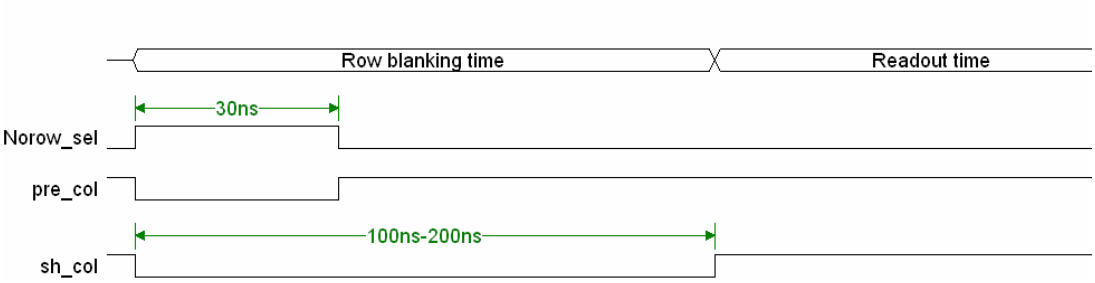
A straightforward way of reducing the R.O.T is by using a sample and hold function.

By means of Sh_col the analog data is tracked during the first 100 nsec during the selection of a new set of lines. After 100 nsec, the analog data is stored. The ROT is in this case reduced to 100 nsec, but as the internal data was not stable yet dynamic range is lost because not the complete analog levels are reached yet after 100 ns.

Figure 18 shows this principle. Sh_col is now a pulse of 100 ns-200 ns starting at the same moment as pre_col and Norowsel. The duration of Sh_col is equal to the ROT. The shorter this time the shorter the ROT will be however this lowers also the dynamic range.

In case "voltage averaging" is required, the sensor must work in this mode with Sh_col signal and a "voltage averaging" signal must be generated after Sh_col drops and before the readout starts (see *Figure 15*)

Figure 19. Reduced standard ROT by means of Sh_col signal. pre_col (short pulse), Norowsel (short pulse) and Sh_col (large pulse)



Precharging of the buses

This timing mode is exactly the same as the mode without sample and hold, except that the prebus1 and prebus2 signals are activated. It should be noticed that the precharging of the buses can be combined with all of the timing modes discussed above. The idea is to have a short pulse of about 5 ns to precharge the output buses to a well-known level. This mode makes the ghosting of bad columns impossible.

In this mode, Nsf_load must be made much larger (at least 1 Mohms).

Figure 20. X- and Y-addressing with precharging of the buses

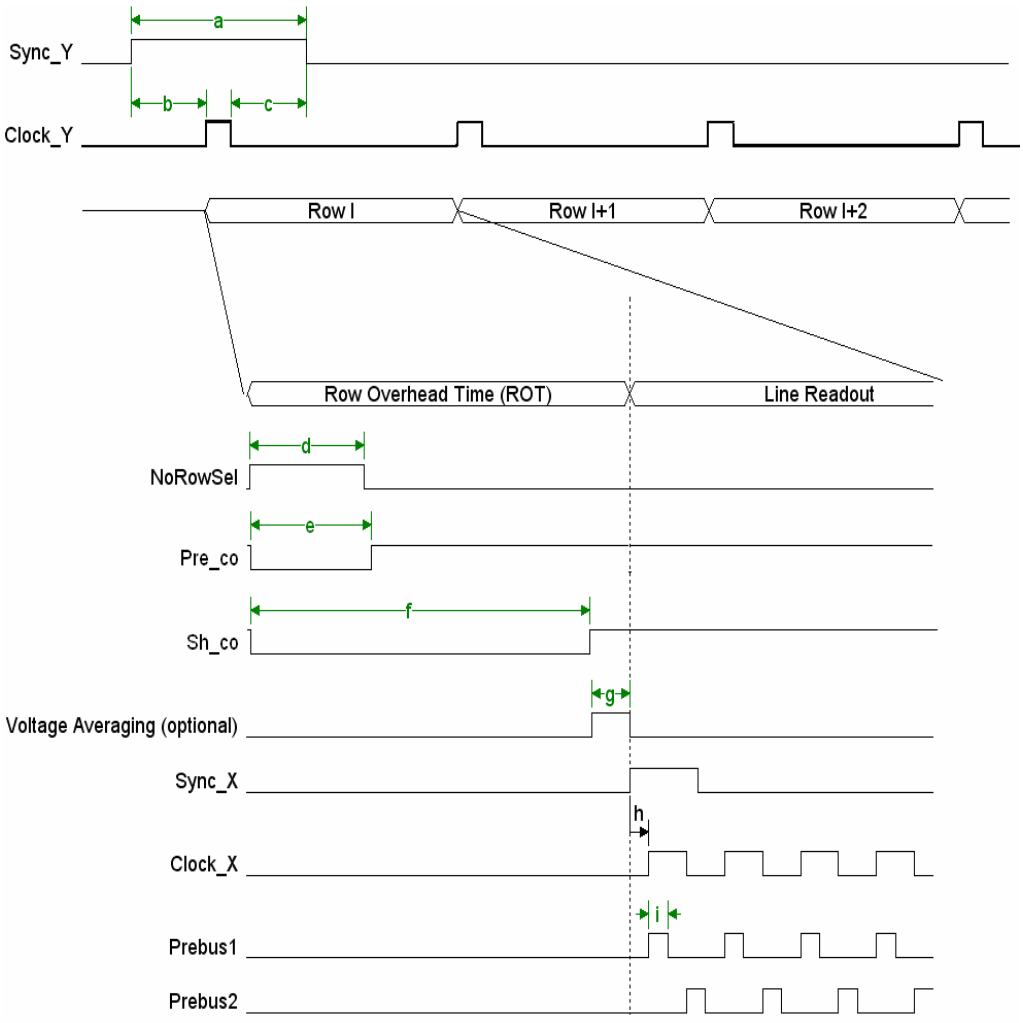


Table 14. Read-out timing specifications with precharching of the buses

Symbol	Name	Value
a	Sync_Y	>20 ns
b	Sync_Y-Clock_Y	>0 ns
c	Clock_Y-Sync_Y	>0 ns
d	NoRowSel	>50 ns
e	Pre_col	>50 ns
f	Sh_col	200 ns (or cst low, depending on timing mode)
g	Voltage averaging	>20 ns
h	Sync_X-Clock_X	>0 ns
i	Prebus pulse	As short as possible

Serial-Parallel-Interface (SPI)

The SPI is required to upload the different modes. *Table 15* shows the parameters and there bit position

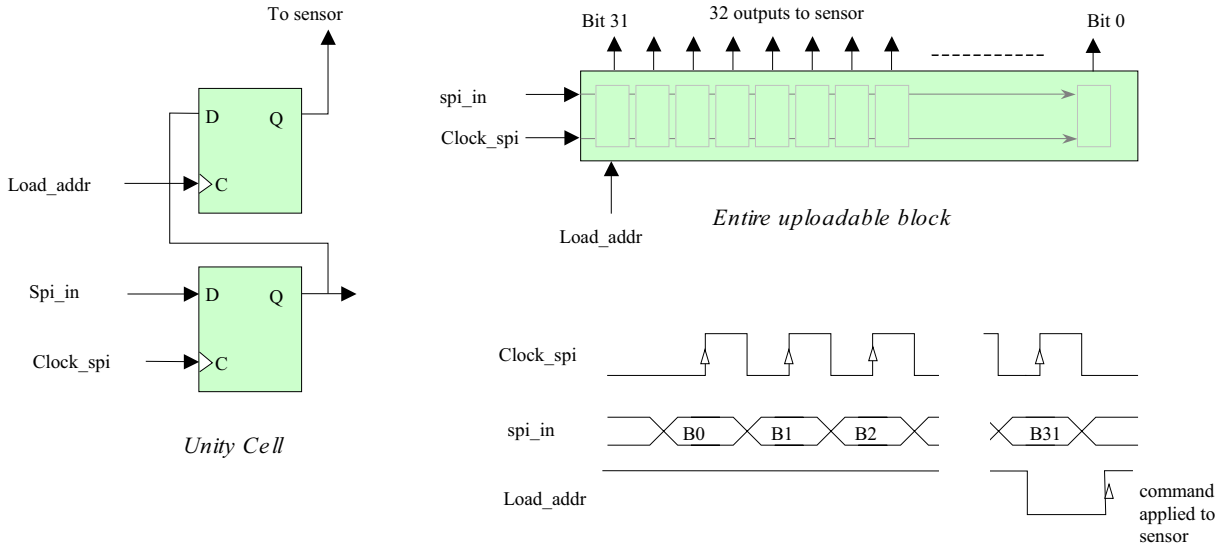
Table 15. SPI parameters

Parameter	Bit nr.	Remarks
Y-direction	0	1: from bottom to top
Y-address	1-10	Bit 1 is LSB
X-voltage averaging enable	11	1: Enabled
X-subsampling	12	1: Subsampling
X-direction	13	0: From left to right
X-address	14-23	Bit 14 is LSB
Nr output amplifiers	24	0: 1 Output
DAC	25-31	Bit 25 is LSB

When all zeros are loaded into the SPI, the sensor will start at pixel 0,0. The scanning will be from left to right and from top to bottom. There will be no sub-sampling or voltage averaging and only one output is used. The DAC will have the lowest level at its output.

When using sub sampling, only even X-addresses may be applied.

Figure 21. SPI block diagram and timing



Pin list

Table 16 is a list of all the pins and their functionalities.

Pad	Pin	Pin Name	Pin Type	Description
1	E1	sync_x	Input	Digital input. Synchronises the X-address register.
2	F1	eos_x	Testpin	Indicates when the end of the line is reached.
3	D2	vdd	Supply	Power supply digital modules.
4	G2	clock_x	Input	Digital input. Determines the pixel rate.
5	G1	eos_spi	Testpin	Checks if the data is transferred correctly through the SPI.
6	F2	spi_data	Input	Digital input. Data for the SPI.
7	H1	spi_load	Input	Digital input. Loads data into the SPI.
8	H2	spi_clock	Input	Digital input. Clock for the SPI.
9	J2	gndo	Ground	Ground output stages
10	J1	out2	Output	Analog output 2.
11	K1	out2DC	Output	Reference output 2.
12	M2	voo	Supply	Power supply output stages
13	L1	out1DC	Output	Reference output 1.
14	M1	out1	Output	Analog output 1.
15	N2	gndo	Ground	Ground output stages.
16	P1	vaa	Supply	Power supply analog modules.
17	P2	gnda	Ground	Ground analog modules.
18	N1	va3	Supply	Power supply column modules.
19	P3	vpix	Supply	Power supply pixel array.
20	Q1	psf_load	Input	Analog reference input. Biasing for column modules. Connect with R=1MΩ to Vaa and decouple with C=100nF to gnda.
21	Q2	nsf_load	Input	Analog reference input. Biasing for column modules. Connect with R=5kΩ to Vaa and decouple with C=100nF to gnda.
22	R1	muxbus_load	Input	Analog reference input. Biasing for multiplex bus. Connect with R=25kΩ to Vaa and decouple with C=100nF to gnda.
23	R2	uni_load_fast	Input	Analog reference input. Biasing for column modules. Connect with R=10kΩ to Vaa and decouple with C=100nF to gnda.
24	Q3	pre_load	Input	Analog reference input. Biasing for column modules. Connect with R=3kΩ to Vaa and decouple with C=100nF to gnda.
25	Q4	out_load	Input	Analog reference input. Biasing for output stage. Connect with R=60kΩ to Vaa and decouple with C=100nF to gnda.
26	N3	dec_x_load	Input	Analog reference input. Biasing for X-addressing. Connect with R=2MΩ to Vdd and decouple with C=100nF to gndd.
27	Q5	uni_load	Input	Analog reference input. Biasing for column modules. Connect with R=1MΩ to Vaa and decouple with C=100nF to gnda.
28	Q6	col_load	Input	Analog reference input. Biasing for column modules. Connect with R=1MΩ to Vaa and decouple with C=100nF to gnda.
29	Q7	dec_y_load	Input	Analog reference input. Biasing for Y-addressing. Connect with R=2MΩ to Vdd and decouple with C=100nF to gndd.
30	R3	vdd	Supply	Power supply digital modules.
31	M3	gndd	Ground	Ground digital modules.
32	L2	prebus1	Input	Digital input. Control signal to reduce readout time.
33	L3	prebus2	Input	Digital input. Control signal to reduce readout time.

Pad	Pin	Pin Name	Pin Type	Description
34	Q8	sh_col	Input	Digital input. Control signal of the column readout.
35	R4	pre_col	Input	Digital input. Control signal of the column readout to reduce row-blanking time.
36	R5	norowsel	Input	Digital input. Control signal of the column readout.
37	R6	clock_y	Input	Digital input. Clock of the Y-addressing.
38	R7	sync_y	Input	Digital input. Synchronises the Y-address register.
39	K2	eos_y_r	Testpin	Indicates when the end of frame is reached when scanning in the 'right' direction.
40	Q9	temp_diode_p	Testpin	Anode of temperature diode.
41	Q10	temp_diode_n	Testpin	Cathode of temperature diode.
42	R8	vpix	Supply	Power supply pixel array.
43	R9	vmem_l	Supply	Power supply Vmem drivers.
44	R10	vmem_h	Supply	Power supply Vmem drivers.
45	R11	vres	Supply	Power supply reset drivers.
46	Q11	vres_ds	Supply	Power supply reset drivers.
47	R12	ref_low	Input	Analog reference input. Low reference voltage of ADC. (see *Figure 7* for exact resistor value)
48	Q12	linear_conv	Input	Digital input. 0= linear conversion; 1= gamma correction.
49	P15	bit_9	Output	Digital output 1 <9> (MSB).
50	Q14	bit_8	Output	Digital output 1 <8>.
51	Q15	bit_7	Output	Digital output 1 <7>.
52	R13	bit_6	Output	Digital output 1 <6>.
53	R14	bit_5	Output	Digital output 1 <5>.
54	R15	bit_4	Output	Digital output 1 <4>.
55	P14	bit_3	Output	Digital output 1 <3>.
56	Q13	bit_2	Output	Digital output 1 <2>.
57	R16	bit_1	Output	Digital output 1 <1>.
58	Q16	bit_0	Output	Digital output 1 <0> (LSB).
59	P16	clock	Input	ADC clock input.
60	N14	gndd	Supply	Digital GND of ADC circuitry.
61	N15	vddd	Supply	Digital supply of ADC circuitry (nominal 2.5V).
62	L16	gnda	Supply	Analog GND of ADC circuitry.
63	L15	vdda	Supply	Analog supply of ADC circuitry (nominal 2.5V).
64	N16	bit_inv	Input	Digital input. 0=no inversion of output bits; 1 = inversion of output bits.
65	M16	CMD_SS	Input	Analog reference input. Biasing of second stage of ADC. Connect to VDDA with R=50 kΩ and decouple with C=100 nF to GNDa.
66	L14	analog_in	Input	Analog input of 1st ADC.
67	M15	CMD_FS	Input	Analog reference input. Biasing of first stage of ADC. Connect to VDDA with R=50 kΩand decouple with C=100 nF to GNDa.
68	M14	ref_high	Input	Analog reference input. High reference voltage of ADC. (see *Figure 7* for exact resistor value)
69	K14	vres_ds	Supply	Power supply reset drivers.
70	J14	vres	Supply	Power supply reset drivers.
71	J15	vpre_l	Supply	Power supply precharge drivers. Must be able to sink current. Can also be connected to ground.
72	J16	vdd	Supply	Power supply digital modules.

Pad	Pin	Pin Name	Pin Type	Description
73	K15	vmem_h	Supply	Power supply Vmem drivers.
74	K16	vmem_l	Supply	Power supply Vmem drivers.
75	H15	ref_low	Input	Analog reference input. Low reference voltage of ADC. (see *Figure 7* for exact resistor value)
76	H16	linear_conv	Input	Digital input. 0= linear conversion; 1= gamma correction.
77	G16	bit_9	Output	Digital output 2 <9> (MSB).
78	F16	bit_8	Output	Digital output 2 <8>.
79	E16	bit_7	Output	Digital output 2 <7>.
80	G15	bit_6	Output	Digital output 2 <6>.
81	G14	bit_5	Output	Digital output 2 <5>.
82	F14	bit_4	Output	Digital output 2 <4>.
83	E14	bit_3	Output	Digital output 2 <3>.
84	D16	bit_2	Output	Digital output 2 <2>.
85	E15	bit_1	Output	Digital output 2 <1>.
86	F15	bit_0	Output	Digital output 2 <0> (LSB).
87	D15	clock	Input	ADC clock input.
88	C15	gndd	Supply	Digital GND of ADC circuitry.
89	D14	vddd	Supply	Digital supply of ADC circuitry (nominal 2.5V).
90	B16	gnda	Supply	Analog GND of ADC circuitry.
91	B14	vdda	Supply	Analog supply of ADC circuitry (nominal 2.5V).
92	C16	bit_inv	Input	Digital input. 0=no inversion of output bits; 1 = inversion of output bits.
93	A16	CMD_SS	Input	Biasing of second stage of ADC. Connect to VDDA with R=50 kΩ and decouple with C=100 nF to GNDa.
94	B15	analog_in	Input	Analog input 2nd ADC.
95	A15	CMD_FS	Input	Analog reference input. Biasing of first stage of ADC. Connect to VDDA with R=50 kΩ and decouple with C=100 nF to GNDa.
96	A14	ref_high	Input	Analog reference input. High reference voltage of ADC. (see *Figure 7* for exact resistor value)
97	C14	vres_ds	Supply	Power supply reset drivers.
98	B13	vres	Supply	Power supply reset drivers.
99	A13	vmem_h	Supply	Power supply Vmem drivers.
100	A9	vmem_l	Supply	Power supply Vmem drivers.
101	A10	vpix	Supply	Power supply pixel array.
102	A11	reset	Input	Digital input. Control of reset signal in the pixel.
103	A12	reset_ds	Input	Digital input. Control of double slope reset in the pixel.
104	B7	mem_hl	Input	Digital input. Control of Vmem signal in pixel.
105	B8	precharge	Input	Digital input. Control of Vprecharge signal in pixel.
106	B9	sample	Input	Digital input. Control of Vsample signal in pixel.
107	B10	temp_diode_n	Testpin	Cathode of temperature diode.
108	B11	temp_diode_p	Testpin	Anode of temperature diode.
109	B6	precharge_bias	Input	Analog reference input. Biasing for pixel array. (see *Table 10* for exact resistor and capacitor value)
110	A8	photodiode	Testpin	Output photodiode.
111	A7	gndd	Ground	Ground digital modules.
112	B12	vdd	Supply	Power supply digital modules.

Pad	Pin	Pin Name	Pin Type	Description
113	A6	eos_y_l	Testpin	Indicates when the end of frame is reached when scanning in the 'left' direction.
114	A1	sync_y	Input	Digital input. Synchronises the Y-address register.
115	A5	clock_y	Input	Digital input. Clock of the Y-addressing.
116	A2	norowsel	Input	Digital input. Control signal of the column readout.
117	A3	volt. averaging	Input	Digital input. Control signal of the voltage averaging in the column readout.
118	B5	pre_col	Input	Digital input. Control signal of the column readout to reduce row-blanking time.
119	A4	sh_col	Input	Digital input. Control signal of the column readout.
120	B1	prebus2	Input	Digital input. Control signal to reduce readout time.
121	B2	prebus1	Input	Digital input. Control signal to reduce readout time.
122	C1	dec_y_load	Input	Analog reference input. Biasing for Y-addressing.
123	D1	vpix	Supply	Power supply pixel array.
124	B4	va3	Supply	Power supply column modules.
125	B3	gnda	Ground	Ground analog modules.
126	C2	vaa	Supply	Power supply analog modules.
127E2	E2	gndd	Ground	Ground digital modules.

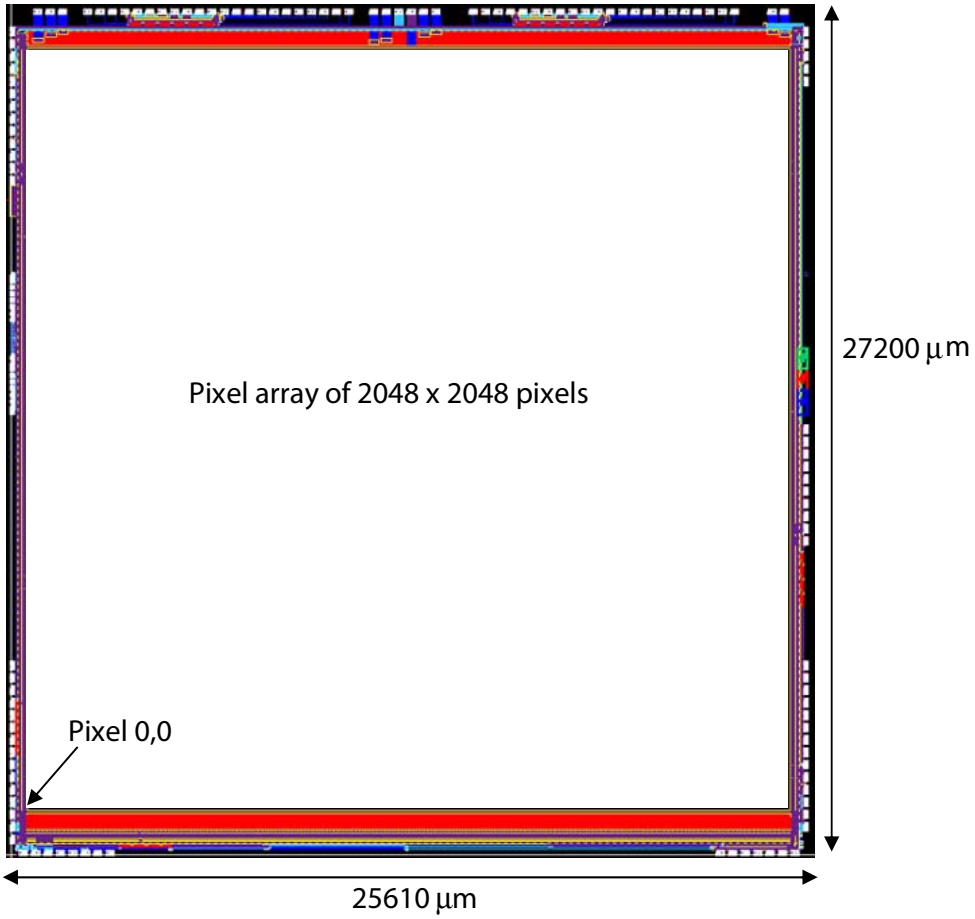
REMARKS:

1. All pins with the same name can be connected together.
2. All digital input are active high (unless mentioned otherwise).
3. All unused inputs should be tied to a non-active level (e.g. VDD or GND).

Geometry and Mechanical specifications

Bare die

Figure 22. Die figure of the LUPA-4000



Pixel 0,0 is located at 478 µm from the left side of the die and 1366 µm from the bottom side of the die.

Package drawing

The LUPA-4000 is packaged in a 127-pin PGA package.

Figure 23. Package drawing of the LUPA-4000 package

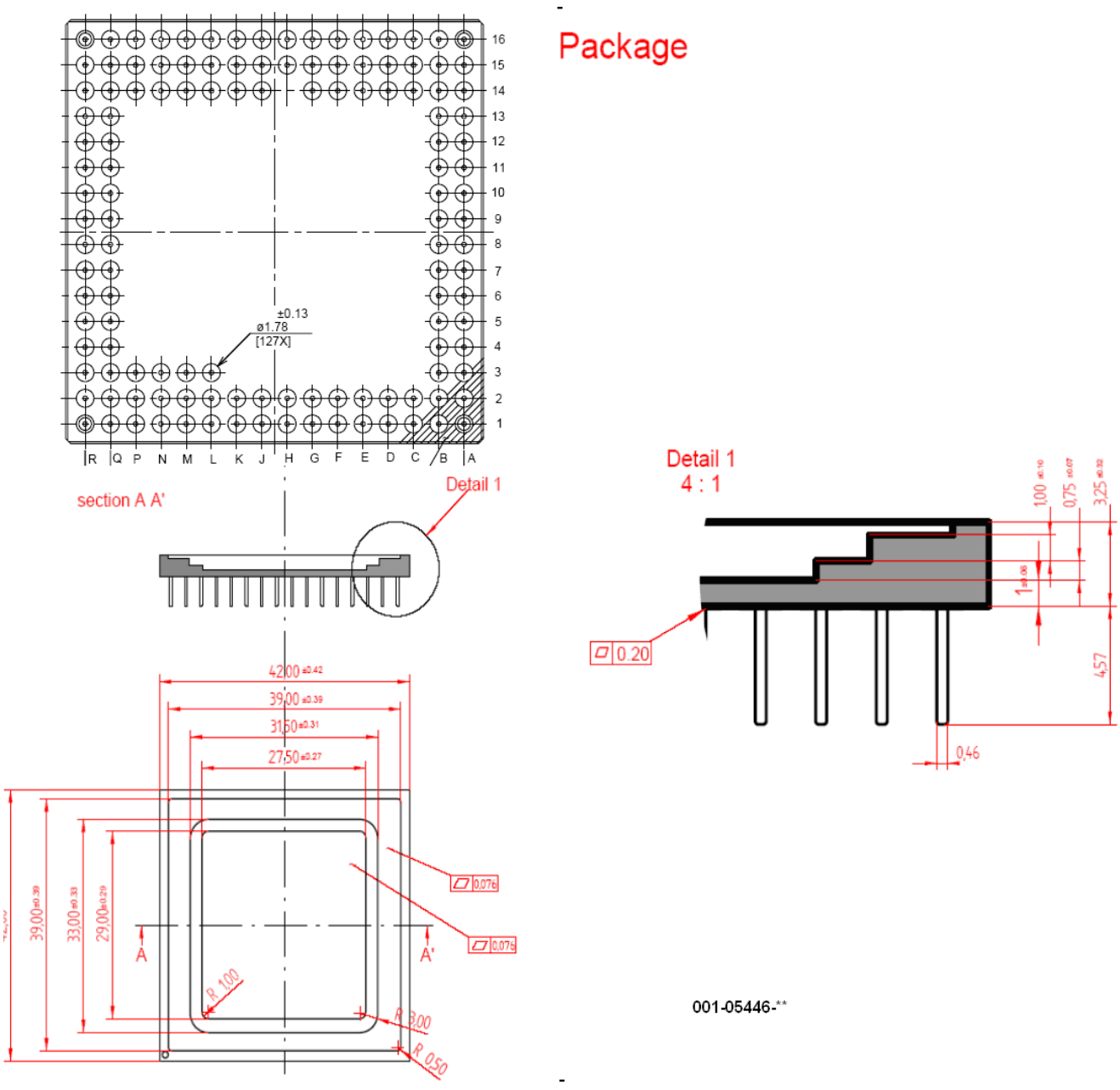
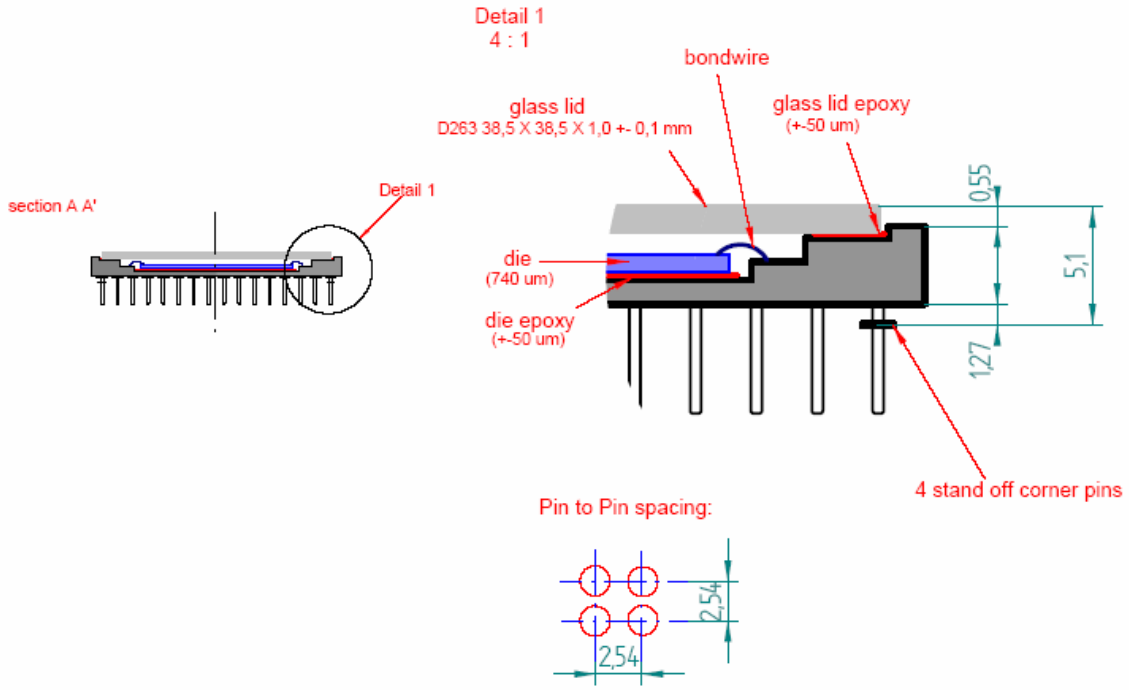


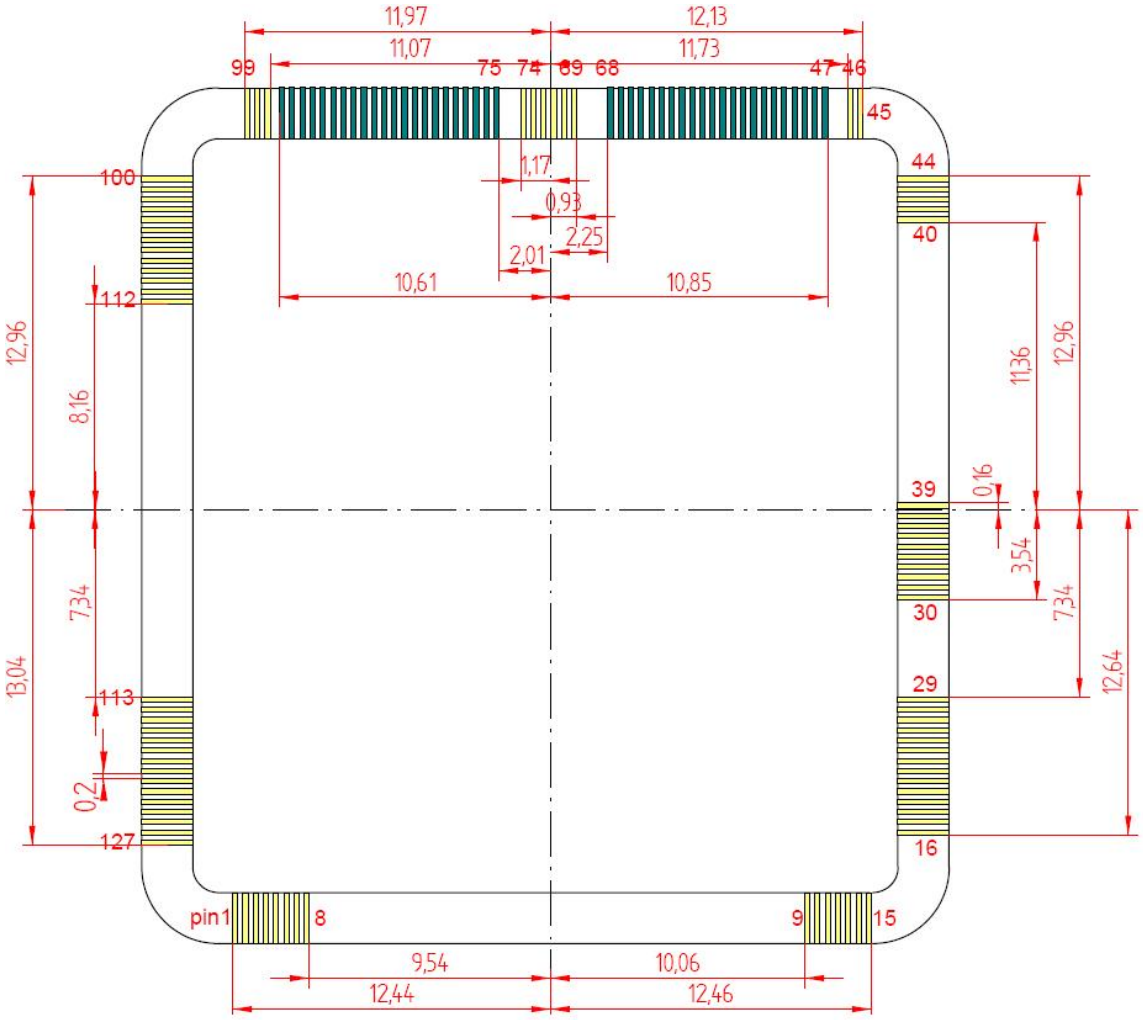
Figure 24. LUPA-4000 package specifications with die



Bonding pads

The bonding pads are located as indicated below.

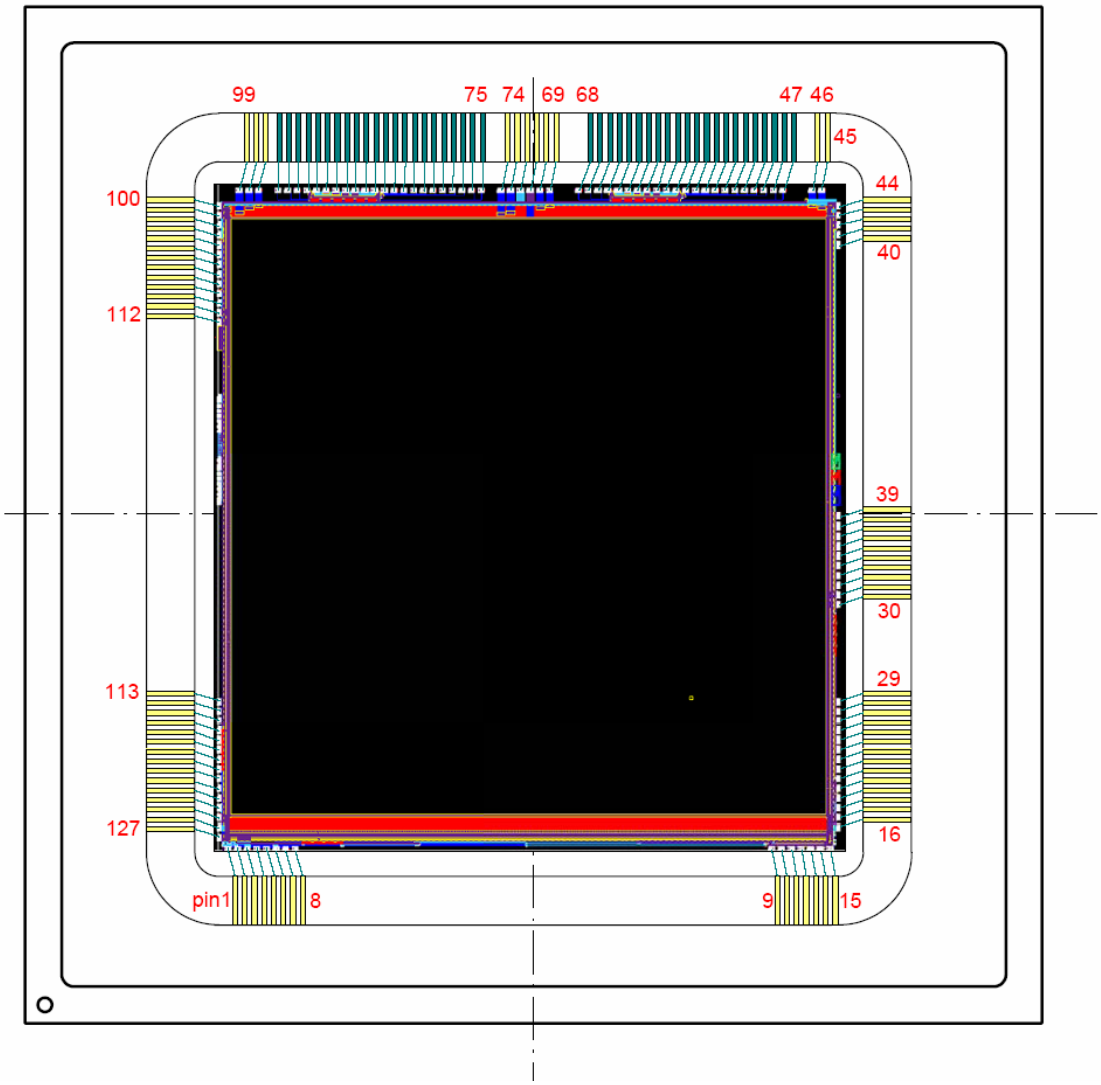
Figure 25. Placing of the bonding pads on the LUPA-4000 package



Bonding diagram

The die is bonded to the bonding pads of the package as indicated below

Figure 26. Bonding pads diagram of the LUPA-4000 package.

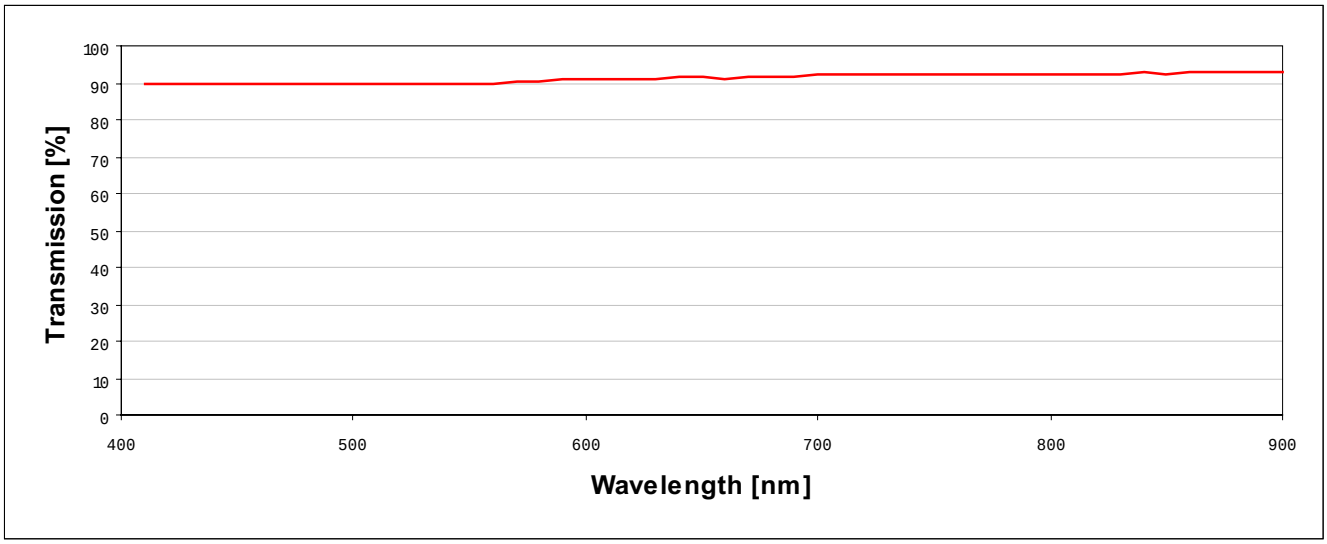


The die will be placed in the package in a way that the center of the light sensitive area will match the center of the package.

Glass transmittance

A D263 glass will be used as protection glass lid on top of the LUPA-4000 monochrome sensors. *Figure 24* shows the transmission characteristics of the D263 glass

Figure 27. Transmission characteristics of the D263 glass used as protective cover for the LUPA-4000 sensors



Handling and soldering precautions

Special care should be given when soldering image sensors with color filter arrays (RGB color filters), onto a circuit board, since color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end-users' assembly processes.

Board Assembly:

Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators should always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

Manual Soldering:

When a soldering iron is used the following conditions should be observed:

- Use a soldering iron with temperature control at the tip.
- The soldering iron tip temperature should not exceed 350°C.
- The soldering period for each pin should be less than 5 seconds.

Precautions and cleaning:

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass.

It is recommended that isopropyl alcohol (IPA) is used as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirmed beforehand whether the solvent will dissolve the package and/or the glass lid or not.

Ordering Information

FillFactory Part Number	Cypress Semiconductor Part Number
LUPA-4000-M	CYIL1SM4000AA-GBC

Disclaimer

The LUPA-4000 is only to be used for non-military applications. A strict exclusivity agreement prevents us to sell the LUPA-4000 to customers who intend to use it for military applications.

FillFactory image sensors are only warranted to meet the specifications as described in the production data sheet. Specifications are subject to change without notice.

Please contact info@FillFactory.com for more information.

APPENDIX A: LUPA-4000 evaluation system

For evaluating purposes an LUPA-4000 evaluation kit is available.

The LUPA-4000 evaluation kit consists of a multifunctional digital board (memory, sequencer and IEEE 1394 Fire Wire interface) and an analog image sensor board.

Visual Basic software (under Win 2000 or XP) allows the grabbing and display of images and movies from the sensor. All acquired images and movies can be stored in different file formats (8 or 16-bit). All setting can be adjusted on the fly to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state

Figure 28. Content of the LUPA-4000 evaluation kit

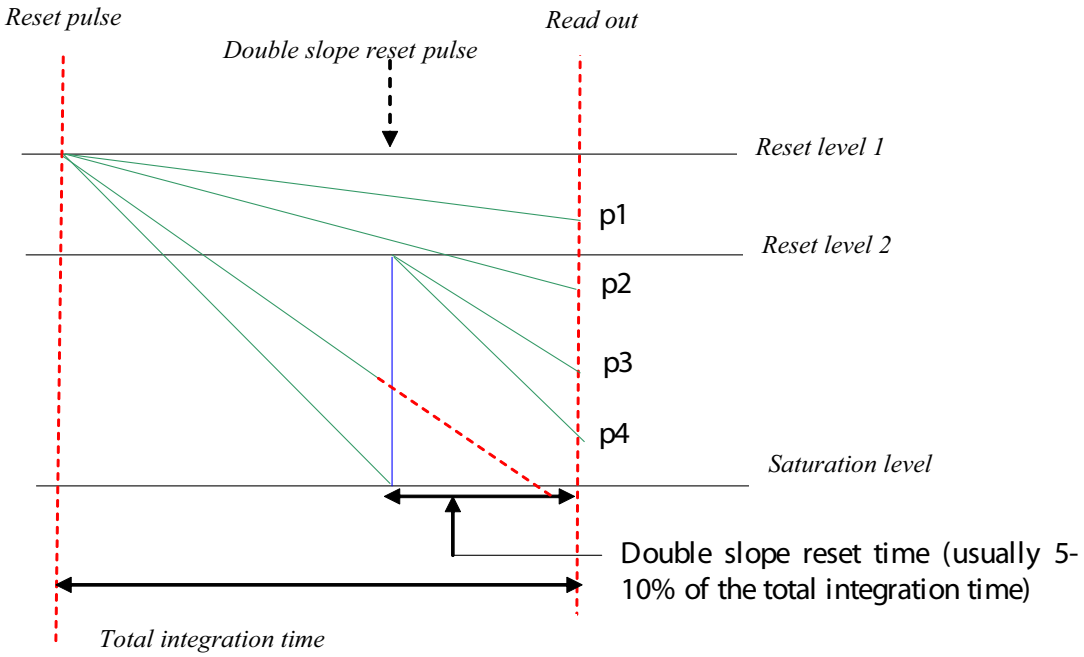
Please contact Fillfactory (info@Fillfactory.com) if you want any more information on the evaluation kit.

APPENDIX B: Frequently Asked Questions

Q: How does the dual (multiple) slope extended dynamic range mode works?

A:

Figure 29. Dual slope diagram



The green lines are the analog signal on the photodiode, which decrease as a result of exposure. The slope is determined by the amount of light at each pixel (the more light the steeper the slope). When the pixels reach the saturation level the analog signal will not change despite further exposure. As you can see without any double slope pulse pixels p3 and p4 will reach saturation before the sample moment of the analog values, no signal will be acquired without double slope. When double slope is enabled a second reset pulse will be given (blue line) at a certain time before the end of the integration time. This double slope reset pulse resets the analog signal of the pixels BELOW this level to the reset level. After the reset the analog signal starts to decrease with the same slope as before the double slope reset pulse. If the double slope reset pulse is placed at the end of the integration time (90% for instance) the analog signal that would have reach the saturation levels aren't saturated anymore (this increases the optical dynamic range) at read out. It's important to notice that pixel signals above the double slope reset level will not be influenced by this double slope reset pulse (p1 and p2).

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Document History Page

Document Title: LUPA-4000 4M PIXEL CMOS Image Sensor Document Number: 38-05712				
REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	310396	See ECN	FPW	Initial Cypress Release
*A	497132	See ECN	QGS	Converted to Frame file
*B	649219	See ECN	FPW	Ordering information update+ title update + package spec label