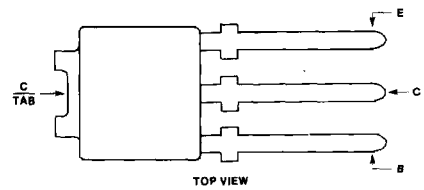
5-Ampere Silicon P-N-P Power Transistors

Features:
- *Low V_{CE} (sat)*
- *Fast switching speed*
- *Complementary to D72F5T1,2*

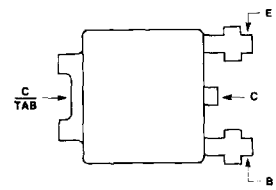
The D73F5T1 and D73F5T2 silicon p-n-p power transistors are designed for high current switching applications. They are intended for use in circuits such as converters, inverters, and pulse-width-modulated regulators.

The D73F5T1 is supplied in the JEDEC TO-251 package and the D73F5T2 is supplied in the JEDEC TO-252 surface-mount package.

TERMINAL DESIGNATION



TO-251AA



TO-252AA

92CS-43478

MAXIMUM RATINGS (T_A = 25°C) (unless otherwise specified)

RATING	SYMBOL	D73F5T1,2	UNITS
Collector-Emitter Voltage	V_{CEO}	-50	Volts
Collector-Base Voltage	V_{CBO}	-60	Volts
Emitter Base Voltage	V_{EBO}	-5	Volts
Collector Current — Continuous	I_C	-5	A
Base Current — Continuous	I_B	-1	A
Total Power Dissipation @ T_C = 25°C @ T_C = 25°C	P_D	1.0 20	Watts
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

THERMAL CHARACTERISTICS (1)

Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L	235	°C

(1) See page 7-16 for thermal considerations.

ELECTRICAL CHARACTERISTICS (T_A = 25°C) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10mA, I_B = 0)	$V_{(BR)CEO}$	-50	—	—	Volts
Collector Cutoff Current (V_{CB} = 50V, I_E = 0)	I_{CBO}	—	—	-1	μA
Emitter Cutoff Current (V_{EB} = 5V, I_C = 0)	I_{EBO}	—	—	-1	μA
SECOND BREAKDOWN					
Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 11			
ON CHARACTERISTICS					
DC Current Gain (I_C = -1A, V_{CE} = -1V)	h_{FE}	70	—	240	—
(I_C = -3A, V_{CE} = -1V)	h_{FE}	30	—	—	
Collector-Emitter Saturation Voltage (I_C = -3A, I_B = -0.15A)	$V_{CE(sat)}$	—	-0.2	-0.4	V
Base-Emitter Saturation Voltage (I_C = -3A, I_B = -0.15A)	$V_{BE(sat)}$	—	-0.9	-1.2	Volts
SWITCHING CHARACTERISTICS					
Turn-on Time	V_{CC} = -30V	t_{on}	—	0.1	—	μs
Storage Time	$-I_{B1} = I_{B2}$ = 0.15A	t_{stg}	—	1.0	—	
Fall Time	Duty Cycle ≦ 1%	t_f	—	0.1	—	

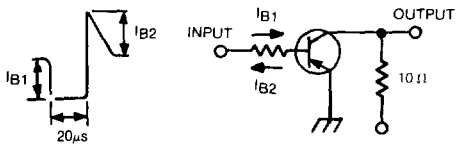


FIG. 1 SWITCHING TIME TEST CIRCUIT

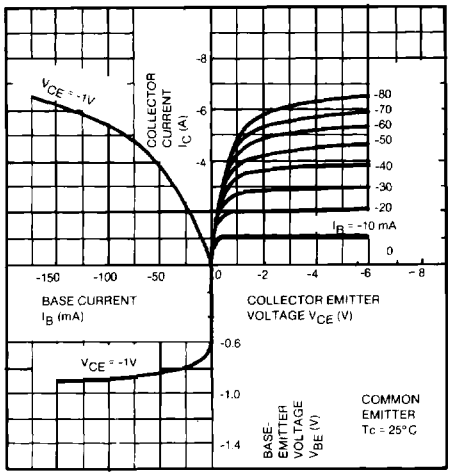


FIG. 2 STATIC CHARACTERISTICS

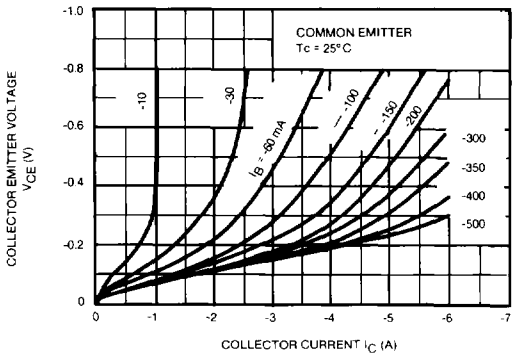


FIG. 3 V_{CE} - I_C

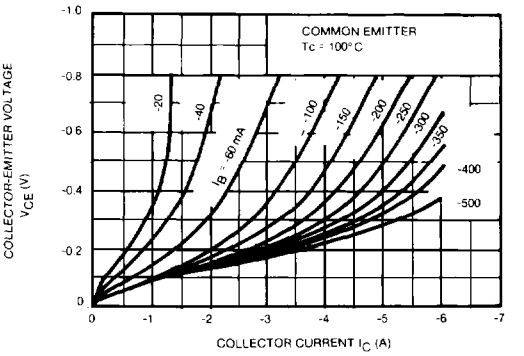


FIG. 4 V_{CE} - I_C

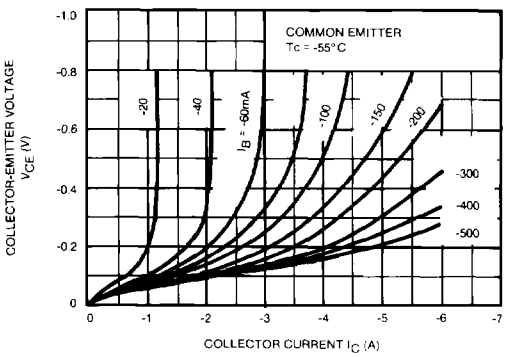


FIG. 5 V_{CE} - I_C

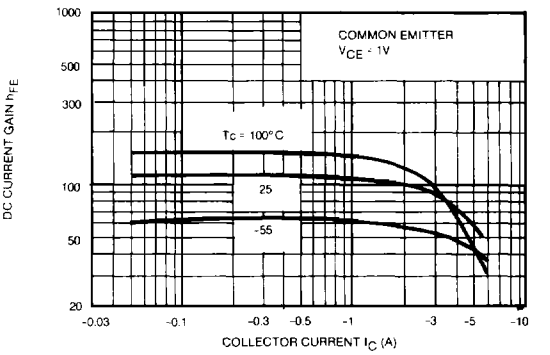


FIG. 6 h_{FE} - I_C

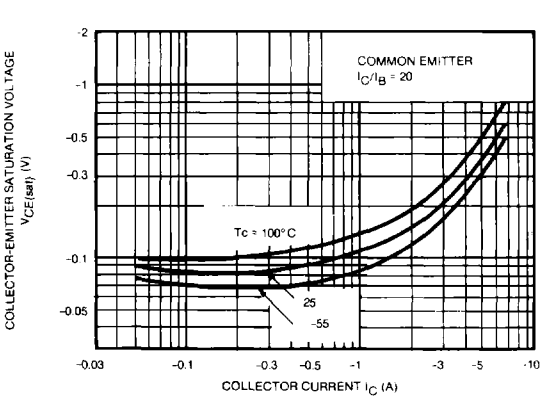


FIG. 7 $V_{CE(sat)}$ - I_C

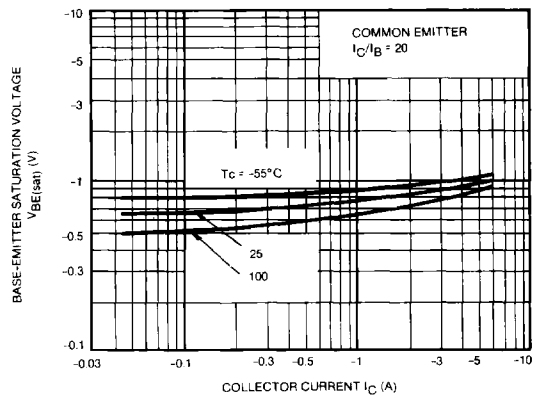


FIG. 8 $V_{BE(sat)}$ - I_C

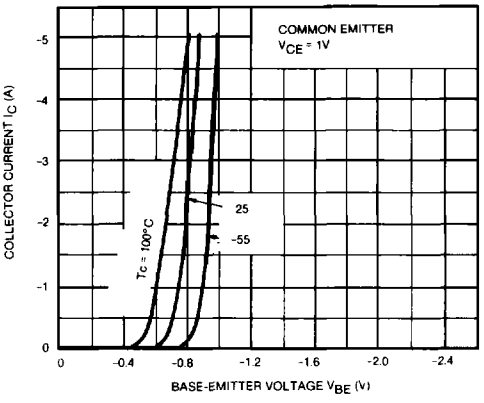


FIG. 9 I_C - V_{BE}

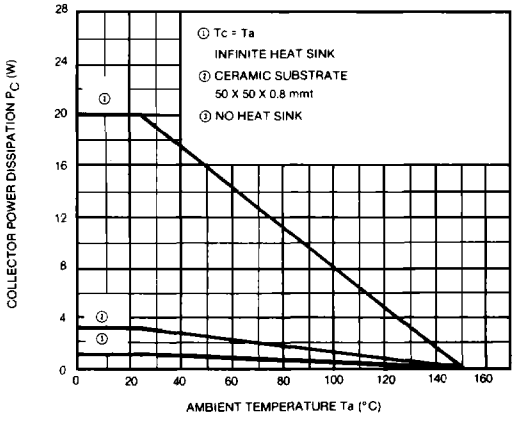


FIG. 10 P_C - Ta

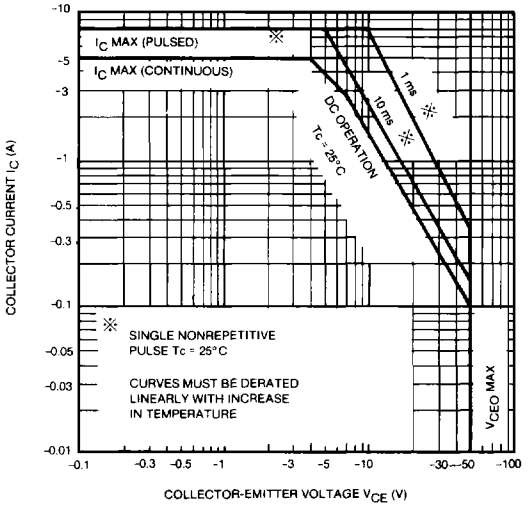


FIG. 11 SAFE OPERATING AREA