8251/Am9551

Programmable Communication Interface
iAPX86 Family

DISTINCTIVE CHARACTERISTICS

- Separate control and transmit register input buffers
- Synchronous or asynchronous serial data transfer
- Parity, overrun and framing errors detected
- Half or full duplex signalling
- Character length of 5, 6, 7 or 8 bits
- Internal or external synchronization
- Odd parity, even parity or no parity bit
- Modem interface controlled by processor
  - Programmable Sync pattern
  - Fully TTL compatible logic levels

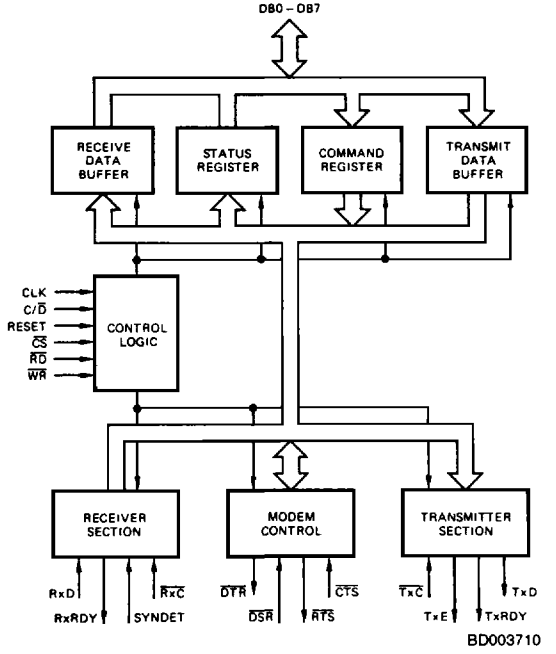
GENERAL DESCRIPTION

The 8251/Am9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream. Simultaneously, serial data can be received, converted into parallel form, deformatted, and then presented to the CPU. The USART can operate in an independent full duplex mode.

Data, Control, operation and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the 8251/Am9551 to service a wide range of communication disciplines and applications.

BLOCK DIAGRAM

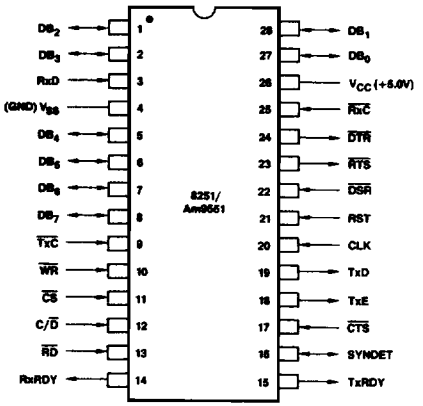


02334B

Refer to page 7-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-28, P-28

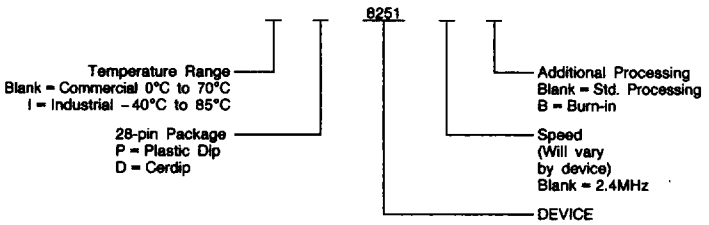


CD005481

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
8251	P, D, ID
8251B	P, D, ID
8251	/BXA

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

ORDERING INFORMATION

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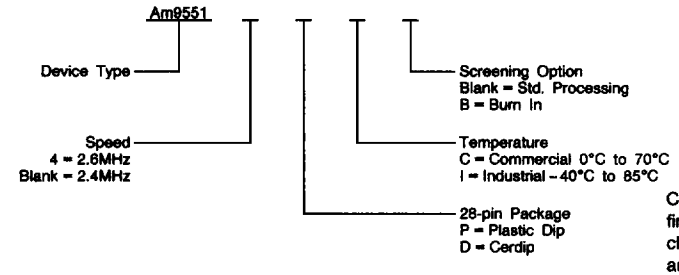


Valid Combinations	
Am9551	PC, DC, DI, DIB
Am9551-4	PC, DC, DI, DIB
Am9551-4	/BXA
Am9551	/BXA

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
27, 28, 1, 2, 5-8	Data Bus (DB_0-DB_7)	I/O	The Am9551 uses an 8-bit bidirectional data bus to exchange information with an associated processor. Internally, data is routed between the data bus buffers and the transmitter section or receiver section as selected by the Read ($\overline{RD}$) or Write ($\overline{WR}$) control inputs.
11	Chip Select ($\overline{CS}$)	I	The active low Chip Select input allows the Am9551 to be individually selected from other devices within its address range. When Chip Select is HIGH, reading or writing is inhibited, and the data bus output is in its high-impedance state.
21	Reset (RST)	I	The Am9551 will assume an Idle state when a high level is applied to the Reset input. When the Reset is returned LOW, the Am9551 will remain in the Idle state until it receives a new mode control instruction.
13	Read ($\overline{RD}$)	I	The active low Read input enables data to be transferred from the Am9551 to the processor.
10	Write ($\overline{WR}$)	I	The active low Write input enables data to be transferred from the processor to the Am9551.
12	Control/Data ($C\overline{D}$)	I	During a Read operation, if this input is at a high level, the status byte will be read, and if it is at a low level, the receive data will be read by the processor. When a Write operation is being performed, this input will indicate to the Am9551 that the bus information being written is a command if $C/\overline{D}$ is HIGH and data if $C/\overline{D}$ is LOW.
20	Clock (CLK)	I	This input is used for internal timing within the Am9551. It does not control the transmit or receive rate. However, it should be at least 30 times the receive or transmit rate in the synchronous mode and 4.5 times the receive or transmit rate in the asynchronous mode. The CLK frequency is also restricted by both an upper and a lower bound. This input is often connected to a clock from the associated processor.
3	Receiver Data (RxD)	I	Serial data is received from the communication line on this input.
25	Receiver Clock ($\overline{RxC}$)	I	The serial data on input RxD is clocked into the Am9551 by the $\overline{RxC}$ clock signal. In the synchronous mode, $\overline{RxC}$ is determined by the baud rate and supplied by the modem. In the asynchronous mode, $\overline{RxC}$ is 1, 16, or 64 times the baud rate as selected in the mode control instruction. Data is sampled by the Am9551 on the rising edge or $\overline{RxC}$.
14	Receiver Ready (RxRDY)	O	The RxRDY output signal indicates to the processor that data has been shifted into the receiver buffer from the receiver section and may be read. The signal is active high and will be reset when the buffer is read by the processor. RxRDY can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver may be running. If the processor does not read the receiver buffer before the next character is shifted from the receiver section, then an overrun error will be indicated in the status buffer.
16	Sync Detect (SYNDET)	I/O	This signal is used only in the synchronous mode. It can be either an output or input depending on whether the program is set for internal or external synchronization. As an output, a high level indicates when the sync character has been detected in the received data stream after the Internal Synchronization mode has been programmed. If the Am9551 is programmed to utilize two sync characters, then SYNDET will go to a high level when the last bit of the second sync character is received. SYNDET is reset when the status buffer is read or when a Reset signal is activated. SYNDET will perform as an input when the External Synchronization mode is programmed. External logic can supply a positive-going signal to indicate to the Am9551 that synchronization has been attained. This will cause it to initialize the assembly of characters on the next falling edge of $\overline{RxC}$. To successfully achieve synchronization, the SYNDET signal should be maintained in a high condition for at least one full period of $\overline{RxC}$.
19	Transmit Data (TxD)	O	Serial data is transmitted to the communication line on this output.
9	Transmitter Clock ($\overline{TxC}$)	O	The serial data on TxD is clocked out with the $\overline{TxC}$ signal. The relationship between clock rate and baud rate is similar to that for RxC. Data is shifted out of the Am9551 on the falling edge of $\overline{TxC}$.
15	Transmitter Ready (TxRDY)	O	The TxRDY output signal goes HIGH when data in the Transmit Data Buffer has been shifted into the transmitter section allowing the Transmit Data Buffer to accept the next byte from the processor. TxRDY will be reset when information is written into the Transmit Data Buffer. Loading command register also resets TxRDY. TxRDY will be available on this output pin only when the Am9551 is enabled to transmit (CTS = 0, TxEN = 1). However, the TxRDY bit in the status Buffer will always be set when the Transmit Data Buffer is empty regardless of the state of TxEN and CTS.
18	Transmitter Empty (TxE)	O	The TxE output signal goes HIGH when the Transmitter section has transmitted its data and is empty. The signal will remain HIGH until a new data byte is shifted from the Transmit Data Buffer to the Transmitter section. In the synchronous mode if the processor does not load a new byte into the buffer in time, TxE will, independent of the status of the TxEN bit in the command register, momentarily go to a high level as SYNC characters are loaded into the Transmitter Section.
24	Data Terminal Ready ($\overline{DTR}$)	O	This signal is a general purpose output which reflects the state of bit 1 in the Command instruction. It is commonly connected to an associated modem to indicate that the Am9551 is ready.
22	Data Set Ready ($\overline{DSR}$)	I	This is a general purpose input signal and forms part of the status byte that may be read by the processor. DSR is generally used as a response to DTR, by the Modem, to indicate that it is ready. The signal acts only as a flag and does not control any internal logic.
23	Request to Send ($\overline{RTS}$)	O	This is a general purpose output, similar to $\overline{DTR}$, and reflects the state of bit 5 in Command Instruction. It is normally used to initiate a data transmission by requesting the modem to prepare to send.
17	Clear to Send ($\overline{CTS}$)	I	This is a general purpose input signal used to enable the 8251/Am9551 to transmit data if the TxEN bit in the Command byte is a one. $\overline{CTS}$ is generally used as a response to RTS by a modem to indicate that transmission may begin. Designers not using $\overline{CTS}$ in their systems should remember to tie it LOW so that 8251/Am9551 data transmission will not be disabled.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Am9551 DATA → DATA BUS
0	1	0	0	DATA BUS → Am9551 DATA
1	0	1	0	Am9551 STATUS → DATA BUS
1	1	0	0	DATA BUS → Am9551 COMMAND
X	X	X	1	DATA BUS → THREE-STATE

3

PROGRAMMING INFORMATION

The microcomputer program controlling the Am9551 performs these tasks:

- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which have been received

Control codes determine the mode in which the Am9551 will operate and are used to set or reset control signals output by the Am9551.

The Status register contents will be read by the program monitoring this device's operation to determine error conditions and when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

Initializing the Am9551

The Am9551 may be initialized following a system reset or prior to starting a new serial I/O sequence. The USART must be reset following power up and subsequently may be reset at any time following completion of one activity and preceding a new set of operations. Following a reset, the Am9551 enters an Idle state in which it can neither transmit nor receive data.

The Am9551 is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the Am9551, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters and then a command.

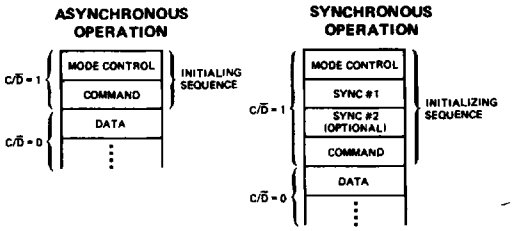


Figure 1. Control Word Sequence for Initialization

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input: either following an external Reset signal or following an internal Reset command.

MODE CONTROL CODES

The Am9551 interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven, or eight data bits, an optional parity bit, a preceding start bit, plus 1, 1½, or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

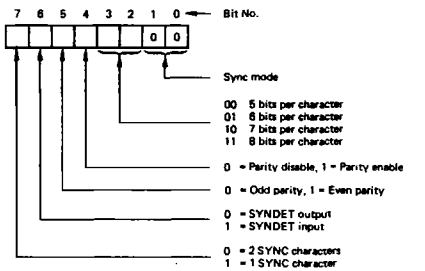


Figure 2. Synchronous Mode Control Code

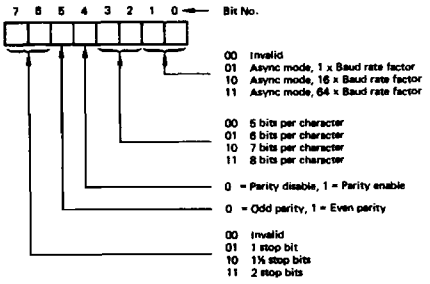


Figure 3. Asynchronous Mode Control Code

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream to establish synchronization.

Command Words

Command words are used to initiate specific functions within the Am9551, such as "reset all error flags" or "start searching for sync." Consequently, Command Words may be issued by

the micro-processor to the Am9551 at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

Figure 4 shows the format for the Command Word.

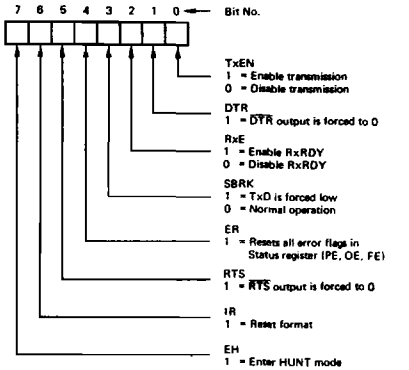


Figure 4. Am9551 Control Command

Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission from the Am9551 cannot take place unless TxEN is set in the command register. Figure 5 defines the way in which TxEN, TxE and TxRDY combine to control transmitter operations.

Bit 1 is the Data Terminal Ready (DTR) bit. When the DTR command bit is set, the $\overline{DTR}$ output connection is active (low). DTR is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Character Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the Am9551 to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transmitted with the ER bit set, all three error flags in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the Am9551. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit (RTS), sets a latch to reflect the RTS signal level. The output of this latch is created independently of other signals in the Am9551. As a result, data transfers may be made by the microprocessor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of RTS.

Bit 6, the Internal Reset (IR), causes the Am9551 to return to the Idle mode. All functions within the Am9551 cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a microprocessor program, the Am9551 must first be reset. Either the external reset connection can be activated, or the Internal Reset Command can be sent to the Am9551. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the Am9551 when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the Am9551, or when SYNC characters are recognized.

TxEN	Txe	TxRDY	
1	1	1	Transmit Output Register and Transmit Character Buffer empty. TxD continues to mark if Am9551 is in the asynchronous mode. TxD will send Sync pattern if Am9551 is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is *shifting a character. Transmit* Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Figure 5. Operation of the Transmitter Section as a *Function of* TxE, TxRDY and TxEN

Status Register

The Status Register maintains information about the current operational status of the Am9551. Figure 6 shows the fomat of the Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the Am9551 can accept a new character for transmission.

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor.

FE is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect character bit format as specified by the current mode.

SYNDET is the synchronous mode status bit associated with internal sync detection.

DSR is the status bit set by the external Data Set Ready signal to indicate that the communication Data Set is operational. All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset only by command.

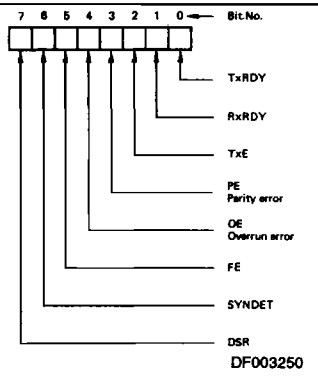


Figure 6. The Am9551 Status Register

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to +7.0V
All Signal Voltages
with Respect to V_{SS} ..... −0.5V to +7.0V
Power Dissipation 1.0W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Part Number	T_A	V_{CC}
8251 Am9551 Am9551-4	0°C to 70°C	5V ±5%

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (Note 1)

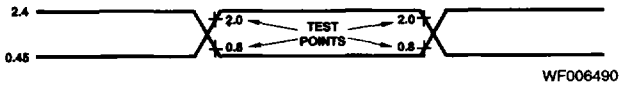
Parameters	Description	Test Conditions	8251			Am9551			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$				2.4			Volts
		$I_{OH} = -100\mu A$	2.4						
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$						0.45	Volts
		$I_{OL} = 1.6mA$			0.45				
V_{IH}	Input HIGH Voltage		2.2		V_{CC}	2.2		V_{CC}	Volts
V_{IL}	Input LOW Voltage		−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			10			10	μA
I_{DL}	Data Bus Leakage	$V_{OUT} = 0.45V$			−50			−50	μA
		$V_{OUT} = V_{CC}$			10			10	
I_{CC}	V_{CC} Supply Current	$T_A = +25°C$		45			45		mA
		$T_A = 0°C$			80			80	
C_O	Output Capacitance	fc = 1.0MHz, Inputs = 0V						15	pF
C_I	Input Capacitance				10			10	pF
$C_{I/O}$	I/O Capacitance				20			20	pF

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 2)

Parameters	Description		8251 Min	8251 Max	Am9551 Min	Am9551 Max	Am9551-4 Min	Am9551-4 Max	Units
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{READ}$ Low Set-up Time		50		50		50		ns
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{WRITE}$ Low Set-up Time		20		20		20		ns
t_{CR}	$\overline{DSR}$, $\overline{DTS}$ to $\overline{READ}$ Low Set-up Time			16		16		16	tCY
t_{CY}	Clock Period		.420	1.35	.380	1.35	.380	1.35	μs
t_{DF}	$\overline{READ}$ High to Data Bus Off Delay		25	200	25	200	25	200	ns
t_{DTx}	TxC Low to TxD Delay			1.0		1.0		1.0	μs
t_{DW}	Data to $\overline{WRITE}$ High Set-up Time		200		150		100		ns
t_{ES}	External SYNDET to RxC Low Set-up Time			16		16		16	tCY
t_{HRx}	Sampling Pulse to Rx Data Hold Time		2.0		2.0		2.0		μs
t_{IS}	Data Bit (Center) to Internal SYNDET Delay			25		25		25	tCY
$t_{\phi W}$	Clock Pulse Width		220	0.7tCY	175	0.7tCY	175	0.7tCY	ns
t_R, t_F	Clock Rise & Fall Time		0	50	0	50	0	50	ns
t_{RA}	$\overline{READ}$ High to $\overline{CS}$, C/D Hold Time		5.0		5.0		5.0		ns
t_{RD}	$\overline{READ}$ Low to Data Bus On Delay			350		250		180	ns
t_{RPD}	Receiver Clock High Time	1xBaud Rate	15		15		15		tCY
		16x & 64x Baud Rate	3.0		3.0		3.0		
t_{RPW}	Receiver Clock Low Time	1x Baud Rate	12		12		12		tCY
		16x & 64x Baud Rate	1.0		1.0		1.0		
t_{RR}	$\overline{READ}$ Pulse Width		430		380		250		ns
t_{RV}	Time Between $\overline{WRITE}$ Pulses During Initialization (Note 3)		6.0		6.0		6.0		tCY
t_{Rx}	Data Bit (Center) to RxRDY Delay			20		20		20	tCY
t_{SRx}	Rx Data to Sampling Pulse Set-up Time		2.0		2.0		2.0		μs
t_{TPD}	Transmitter Clock High Time	1x Baud Rate	15		15		15		tCY
		16x & 64x Baud Rate	3.0		3.0		3.0		
t_{TPW}	Transmitter Clock Low Time	1x Baud Rate	12		12		12		tCY
		16x & 64x Baud Rate	1.0		1.0		1.0		
t_{Tx}	Data Bit (Center) to TxRDY Delay			16		16		16	tCY
t_{TxE}	Data Bit (Center) to Tx EMPTY Delay			16		16		16	tCY
t_{WA}	$\overline{WRITE}$ High to $\overline{CS}$, C/D Hold Time		20		20		20		ns
t_{WC}	$\overline{WRITE}$ High to TxE, $\overline{DTR}$, $\overline{RTS}$ Delay			16		16		16	tCY
t_{WD}	$\overline{WRITE}$ High to Data Hold Time		40		40		40		ns
t_{WW}	$\overline{WRITE}$ Pulse Width		400		380		250		ns
f_{Rx}	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	DC	520	
f_{Tx}	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	DC	520	

Notes:
1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. Test conditions include: transition times ≤ 20ns, output loading of 1 TTL gate plus 100pF, input and output timing reference levels of 0.8V and 2.0V.
3. This time period between write pulses is specified for initialization purposes only when MODE, SYNC 1, SYNC 2, COMMAND and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
4. Reset Pulse Width = 6tCY min.
5. Switching Characteristics parameters are listed in alphabetical order.

SWITCHING TEST INPUT/OUTPUT WAVEFORM

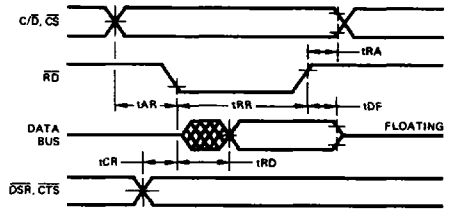


WF006490

AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

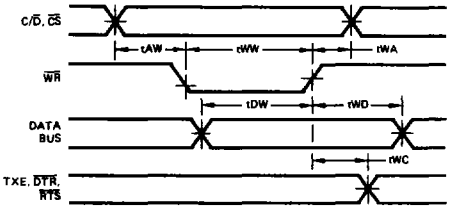
SWITCHING WAVEFORMS

READ OPERATION



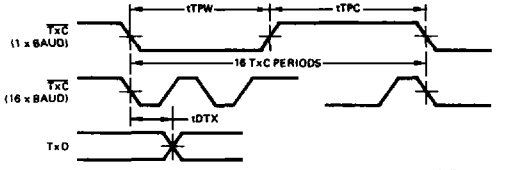
WF006500

WRITE OPERATION



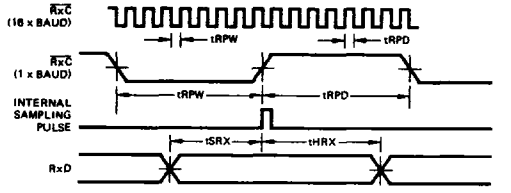
WF006510

TRANSMITTER CLOCK AND DATA



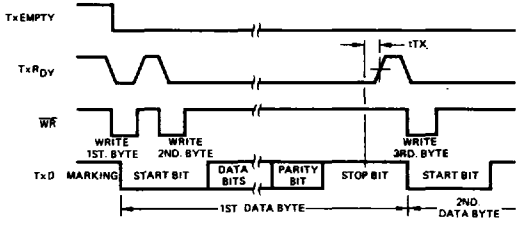
WF006520

RECEIVER CLOCK AND DATA



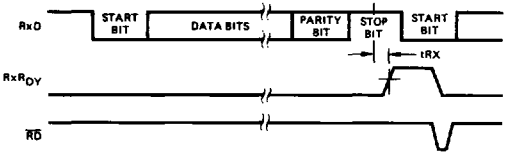
WF006530

TxRD TIMING (ASYNC MODE)



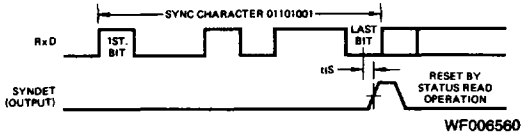
WF006540

RxRDY TIMING (ASYNC MODE)



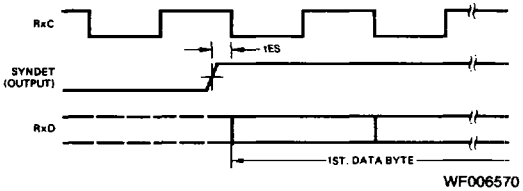
WF006550

INTERNAL SYNC DETECT (SYNC MODE ONLY)



WF006560

EXTERNAL SYNC DETECT (SYNC MODE ONLY)



WF006570

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Refer to page 7-1 for Essential Information on Military Devices