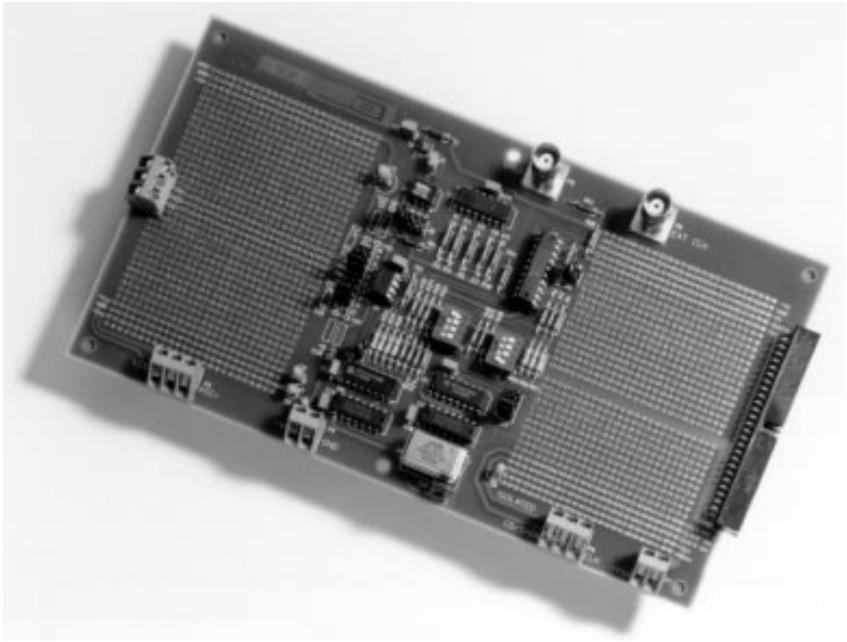
BURR - BROWN®

DEM-ADS78DIP

EVALUATION FIXTURE



FEATURES

- ANALOG BREADBOARD AREA
- DIGITAL BREADBOARD AREA
- FLEXIBLE CLOCK PROGRAMMING
- FLEXIBLE REFERENCE VOLTAGE PROGRAMMING
- STAND-ALONE CAPABILITY

APPLICATIONS

- SMALL DYNAMIC RANGE DIGITIZING
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY OPERATED SYSTEMS

DESCRIPTION

The DEM-ADS78DIP evaluation fixture is designed for quick evaluation of Burr-Brown's line of 8-pin plastic DIP analog-to-digital converter including, ADS1286, ADS7816, ADS7817, ADS7818, ADS7822, ADS7834, and ADS7835. Although these products are available in other package types, such as MSOP, SSOP, and SOIC, the DEM-ADS78DIP provides an excellent way to evaluate all of these products in their DIP packages with one board. The board has features that allow the user to evaluate all the functions of these A/D converters. The options offered to the user includes an easily configurable voltage reference, a flexible clock generator circuit, an analog breadboard, digital breadboard and an isolated digital breadboard areas. Optional power supply connections are also available on the DEM-ADS78DIP board to assist in the evaluation of possible transducer input circuits on the analog breadboard as well as digital isolation circuits on the isolated digital breadboard. The DEM-ADS78DIP has been designed to accommodate stand-alone operation, allowing the user to easily connect to an external processor.

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USING THE VARIOUS A/D CONVERTERS WITH THIS BOARD

The product line that is compatible with this evaluation fixture is listed in Table I. This product line features low power operation with automatic power down, asynchronous serial interface and a differential input. The reference voltage can be varied in order to change the input range and consequently the LSB size. Low power, automatic power down, and small size make these A/D converters ideal for battery operated systems. They are also ideal for remote or isolated data acquisition applications. Although this evaluation fixture is designed to evaluate the devices in an 8-pin DIP, each product has a surface-mount option available.

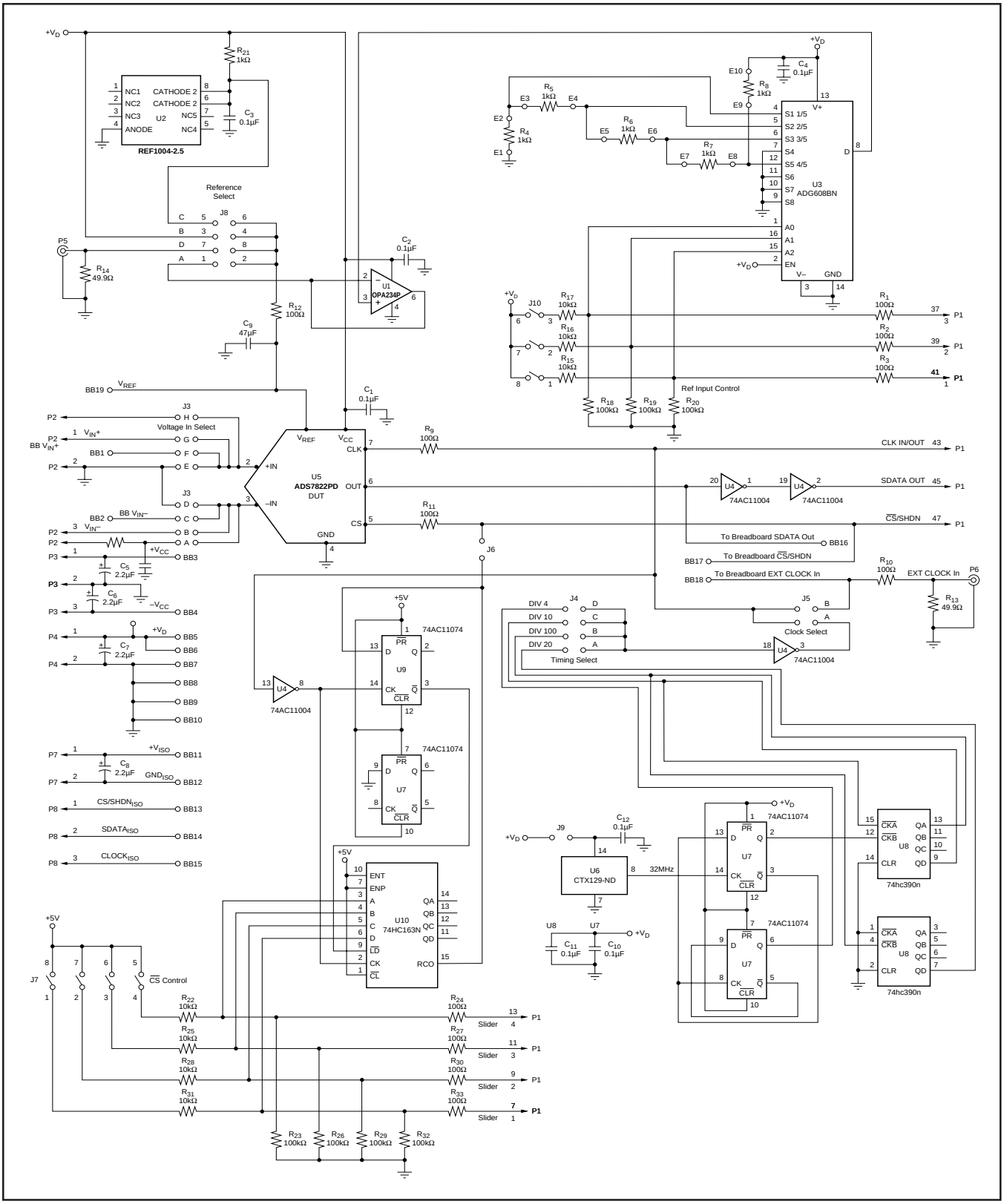

FIGURE 1. DEM-ADS78DIP Circuit Diagram.

PRODUCT	CLOCK RATE	SAMPLE RATE	V_{REF} RANGE
ADS1286	320kHz	20kHz	0.1V - 5V
ADS7816	3.2MHz	200kHz	0.1V - 5V
ADS7817	3.2MHz	200kHz	0.4V - 5V
ADS7818	8MHz	500kHz	2V - 2.55V
ADS7822	1.6MHz	100kHz	0.1V - 5V
ADS7834	8MHz	500kHz	2V - 2.55V
ADS7835	8MHz	500kHz	2V - 2.55V

TABLE I. Some of the Products that can be Demonstrated with this Fixture are Shown Above.

DEM-ADS78DIP BOARD DESCRIPTION

A circuit diagram of the DEM-ADS78DIP is shown in Figure 1. This demonstration fixture has four fundamental active sections on the board which eases the evaluation process of the Device Under Test (DUT). These sections are the analog input, the voltage reference block, clock generation network and the digital interface. Each section is configurable to accommodate the differences between the 8-pin DIP A/D products available from Burr-Brown. The DUT socket (U5) allows for the easy evaluation of any number of A/D converters without doing tedious soldering and desoldering. Additionally, analog and digital breadboard sections are available in the event the user requires further customization of the circuit.

The power supply terminal block P4 should be connected with $+V_D$ = +5V (nominal). P3 and P7 are available as optional supply terminal blocks to be powered at the discretion of the user.

There are five jumpers (J3, J4, J5, J8, and J9) on the board that allow the flexibility needed during the evaluation phase of the DUT. J4 is directly connected to the clock generation network. This network divides the oscillator clock, U6, by 4 10, 20, or 100. To further enhance the flexibility of the clocking capability, J5 can be used to jumper an external clock into the circuit. Finally, J8 can be used to select the voltage reference source to the DUT pin 1 (V_{REF}). The jumper options are listed in Tables II through VI. Each of the four active sections and the three breadboard sections are discussed below.

ANALOG INPUT SECTION

The analog inputs of the DUT are accessible from the terminal block P2 or from the center signal busses on the analog breadboard area. In all cases, J3 must be properly configured.

The inverting and non-inverting analog inputs of the A/D converter (DUT in U5 socket) are available from pins 3 and 2, inclusive. These pins are connected to the four pins on the jumper, J3. The inverting input of the A/D converter (DUT pin 3) can be connected to the pins of J3-A, J3-B, J3-C and J3-D. The non-inverting input of the A/D converter (DUT pin 2) can be connected to the pins of J3-H, J3-G, J3-F and J3-E. This type of flexibility allows the user to easily attach the inputs of the DUT to the input terminal block, P2, the breadboard, or ground. The input jumper connections (J3) are shown in Figure 2 and summarized in Table II.

Optional R || C input networks (J3-A and J3-H) are designed to allow the user to generate a DC offset off set from the power supply to the input pin(s) or design an R || C low pass filter. Both configurations are shown in Figure 3.

JUMPER POSITION	DESCRIPTION
A	Connects pin 3 of DUT (V_{IN}–) to P2 through adjustable R || C network.
B	Connects pin 3 of the DUT (V_{IN}–) directly to the input connector P2 : V_{IN}–
C	Connects pin 3 of the DUT (V_{IN}–) to the breadboard bus in the center of the analog breadboard area.
D	Connects pin 3 of the DUT (V_{IN}–) to GND.
E	Connects pin 2 of the DUT (V_{IN}+) to GND.
F	Configures pin 2 of the DUT (V_{IN}+) directly to the breadboard bus.
G	Configures pin 2 of the DUT (V_{IN}+) to the input connector P2: V_{IN}+
H	Connects pin 2 of the DUT (V_{IN}+) to R2 through adjustable R || C network.

TABLE II. J3: Input Configuration Jumper. Both inputs to the DUT (pins 2 and 3) must be connected to one of the three options described above in order to obtain a sensible output.

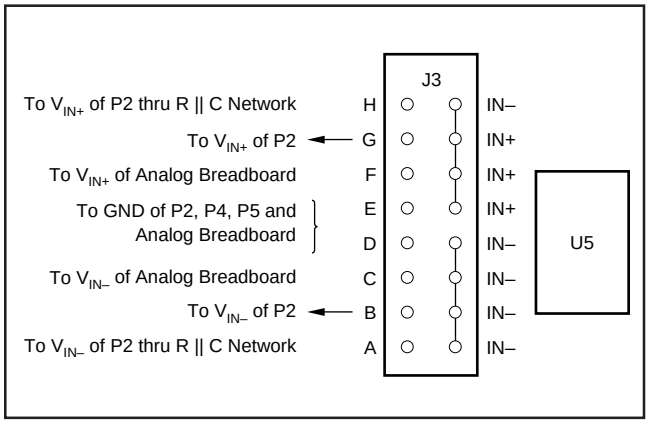

FIGURE 2. Analog Input Jumper Configuration, J3.

The analog breadboard section, located nearest to the DUT, is provided to allow the user to configure their own front end circuits. Nine power and signal busses in conjunction with two supply terminals provide enough flexibility for this area, making it easy to build any desired analog and/or reference circuit. The nine power and signal busses are separated into three groups; (a) V_{REF}, GND, $+V_D$, (b) V_{IN}+, GND, V_{IN}–, and (c) $+V_{CC}$, GND, $–V_{CC}$ (see Figure 4 for detailed layout).

V_{REF} is connected directly to the A/D converter's reference pin (pin 1). This allows the user to design and build custom reference circuits on the analog breadboard. If the V_{REF} bus

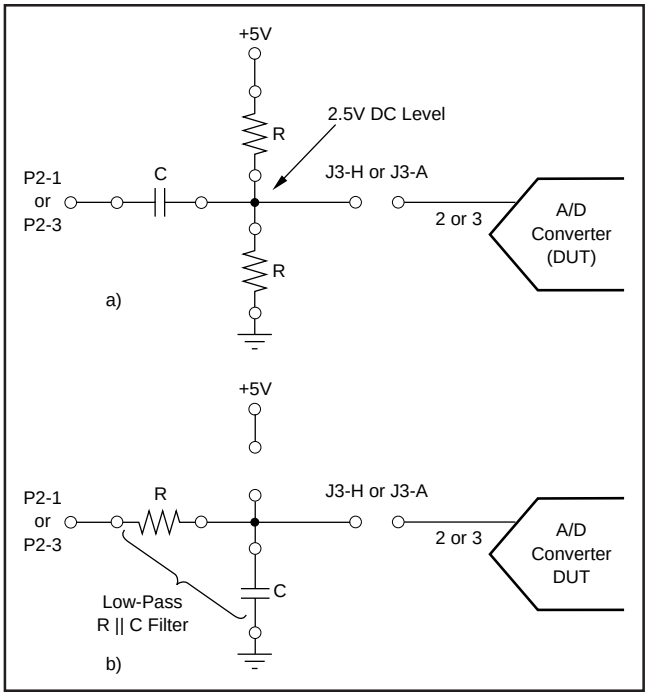

FIGURE 3. The R || C network at the input of the DUT (J3-H and J3-A) can be configured to provide a dc level shift (a) for the input signal at P2 or a low pass filter (b).

is used, J8 should be open. A GND is in between the V_{REF} and the $+V_D$ busses. This is the same GND that is connected to the power supply terminal, P4. The third bus in this area is $+V_D$. $+V_D$ is powered from the terminal block, P4. This terminal block powers the DUT and must be in compliance with the DUT's specified power supply range. This terminal block also supplies power to the other devices on the board.

$V_{IN}+$ and $V_{IN}–$, along with another GND bus, are placed through the center of the analog breadboard area. $V_{IN}+$ and $V_{IN}–$ are made available on the analog breadboard by connecting the appropriate jumper with J3 (as described in Table II). The GND bus is also connected to the power supply terminal, P4.

The third group power consists of $V_{CC}+$, GND, and $V_{CC}–$. $V_{CC}+$ and $V_{CC}–$ are independent supplies that are powered through the supply terminal, P3.

Note: Some of the DUT devices for this board have power supply pin labels of $+V_{CC}$ in their data sheet. This is not the same as the $V_{CC}+$ connection on the board.

These supplies can be any value, dependent on the user's needs. All GND connections on the analog breadboard area are also used as the ground reference for the devices installed on the remainder of the board.

CLOCK CIRCUITRY

The clock section of the board consists of U6, U7, U8, U9, U10, J4, J6, J7, J9, and P6. A 32MHz oscillator chip is installed in the U6 socket. This chip can be replaced as deemed necessary by the user. U7 and U8 are used to divide the clock signal from U6 by 4, 10, 20 and 100, as described in Table III. This entire clock section can be powered down by removing the J9 jumper top. An external clock can be connected via the BNC connector, P6 (EXT CLK). The best performance is achieved with a 50% clock duty cycle (in the case of J4-A and J4-D). The external clock instead of J4-B and J4-C is recommended for best results. In all cases, refer to Table III and IV for the correct jumper configuration.

JUMPER POSITION	DESCRIPTION	FACTORY FREQUENCY	BEST SUITED FOR
A	Divides the clock oscillator, U6, by 20.	1.6MHz	ADS7822
B	Divides the clock oscillator, U6, by 100.	320kHz	ADS1286
C	Divides the clock oscillator, U6, by 10.	3.2MHz	ADS7616 ADS7817
D	Divides the clock oscillator, U6, by 4.	8MHz	ADS7818 ADS7834 ADS7835

TABLE III. J4: Clock Divider Control. The stated factory frequency assumes a 32MHz clock oscillator is inserted in U6.

JUMPER POSITION	DESCRIPTION
A	Selects the clock input to the DUT to come from the Clock Divider portion of the demo board. Use J4 to configure the desired frequency.
B	Selects the clock input to the DUT to come from the External Clock BNC connector, P6.

TABLE IV. J5: External Clock Control.

U9, U10, J6 and J7 are provided to control the function of $\overline{CS}$ to the device. U10 is a 4-bit Synchronous Binary Center. In conjunction with U9 (D-type Flip Flop) and J7 the $\overline{CS}$ can be programmed for 12-bit, 10-bit or 8-bit operation. Refer to Table V for details. J6 disconnects this function completely.

SLIDER POSITION				DESCRIPTION
1	2	3	4	
Off	Off	Off	Off	17 clock cycles
Off	Off	Off	On	16 clock cycles per conversion for 12-bit operation.
Off	Off	On	Off	15 clock cycles
Off	Off	On	On	14 clock cycles per conversion for 10-bit operation.
Off	On	Off	Off	13 clock cycles
Off	On	Off	On	12 clock cycles per conversion for 8-bit operation
Off	On	On	Off	11 clock cycles
Off	On	On	On	10 clock cycles
On	Off	Off	Off	9 clock cycles, etc.

TABLE V. J7; $\overline{CS}$ Control.

VOLTAGE REFERENCE BLOCK

The voltage that is supplied to the A/D converter can be provided through one of five sources; an external reference (P5, V_{REF}), a precision 2.5V reference (U2), a digital programmable reference (U3 and J10), the power supply or

J10 SWITCH POSITIONS 4	3	2	1	MATHEMATICAL VALUE (If E1 through E10 are changed by user)	FACTORY SET VOLTAGE
X	OFF	OFF	OFF	$+V_D$ (R4)/(R4 + R5 + R6 + R7 +R8)	1V
X	OFF	OFF	ON	$+V_D$ (R4 + R5 + R6 + R7)/(R4 + R5 + R6 + R7 + R8)	4V
X	OFF	ON	OFF	$+V_D$ (R4 + R5 + R6)/(R4 + R5 + R6 + R7 + R8)	3V
X	ON	OFF	OFF	$+V_D$ (R4 + R5)/(R4 + R5 + R6 + R7 + R8)	2V
X	ON	ON	ON		0V
X	OFF	ON	ON		
X	ON	OFF	ON		
X	ON	ON	OFF		

TABLE VII. J10: Multiplexed Reference Voltage Selection. All other switch settings are invalid, however, other combinations will not cause damage. (X = Don't Care).

JUMPER POSITION	DESCRIPTION
A	The Voltage Reference Input to the DUT is selected to be the digitally programmable reference, implemented with U3, J10, R4, R5, R6, R7 and R8. This voltage reference function is fully implemented with the selection of this jumper in conjunction with instructions for J10 found in Table V.
B	The Voltage Reference Input to the DUT is selected to be the power supply voltage, $+V_D$.
C	The Voltage Reference Input to the DUT is selected to be connected to the REF1004-2.5, a 2.5V precision reference (U2).
D	The Voltage Reference Input to the DUT is selected to come from the V_{REF} BNC connector, P5.
No Jumper Top	If the A/D converter has an internal reference (such as the ADS7818) or if reference circuit is built on the analog breadboard area and soldered to the V_{REF} bus.

TABLE VI. J8 : Reference Voltage Configuration.

P1 CONNECTOR PIN	DESCRIPTION
All even pins	GND
41	Interface through J10 to A2 of U3 (analog multiplexer) Slider 1, Table VII
39	Interface through J10 to A1 of U3 (analog multiplexer) Slider 2, Table VII
37	Interface through J10 to A0 of U3 (analog multiplexer) Slider 3, Table VII
43	Clock interface to the DUT and clock section on the board
45	DATA OUT interface from the DUT
47	$\overline{CS}$/SHDN interface to the DUT
13	Interface through J7 ($\overline{CS}$ control), Slider 4, Table V
11	Interface through J7 ($\overline{CS}$ control), Slider 3, Table V
9	Interface through J7 ($\overline{CS}$ control), Slider 2, Table V
7	Interface through J7 ($\overline{CS}$ control), Slider 1, Table V

TABLE VIII. P1 Interface to the DEM-ADS78DIP Evaluation Fixture.

from a circuit built on the analog breadboard area. The origin of the voltage reference is configured using jumper, J8, per Table VI.

If the jumper top for J8 is placed in position A, an analog multiplexer (U3) is used to switch in various voltages to the reference pin of the DUT. The sockets E1 through E10 allow for easy insertion of standard through-hole resistors. With these sockets the user can easily configure a custom array of reference voltages for the DUT. See Table VII for details.

DIGITAL BREADBOARD

Non-isolated Digital Breadboard Area

The non-isolated digital breadboard area shown in Figure 4 has five power/signal busses available. $+V_D$ is connected directly to the power terminal, P4, having a nominal voltage of +5V. The bus GND is directly connected to the board ground plane. $\overline{CS}$ is connected directly to the DUT's $\overline{CS}$/SHDN (pin $\overline{5}$). SDATA is connected directly to the $\overline{DUT}$'s D_{OUT} (pin 6). CLK is connected directly to the clocking network (per Tables III and IV) and to the DUT's DCLOCK (pin 7).

Isolated Digital Breadboard Area

The isolated digital breadboard section is laid out in such a way that the power supply terminals P3 (V_{CC}+, V_{CC}–, GND) and P4 ($+V_D$, GND) are not connected to the power planes in this section (see Figure 6). The two terminal blocks, P8 and P7, are provided to allow the user easy access to the power busses $\overline{CS}/SHDN_{ISO}$ (P8), $SDATA_{ISO}$ (P8), CLK_{ISO} (P8), $+V_{ISO}$ (P7) and GND_{ISO} (P7).

This breadboard section was designed to allow the user to breadboard an isolated power and isolated signal interface to the DEM-ADS78DIP board. This is accomplished by separating the power and ground planes of the isolated breadboard section from the rest of the board.

This area is not designed to withstand high isolation voltages. It has been included to help the designer evaluate the effects of isolated power sources such as DC to DC converters.

DIGITAL INTERFACE

The A/D converter, analog multiplexer (U3) and the on-board clock are all accessible through the digital interface socket, P1. All even pins of P1 are connected to the board GND (per power terminal, P4). See Table VIII for more details.

The remainder of the layout information is shown in Figures 4 through 7. Table IX summarizes the external terminal connections to the DEM-ADS78DIP board as well as the connections from the breadboard to the evaluation fixture circuitry. The parts list for this evaluation fixture is listed in Table X.

DESCRIPTION	DUT PIN NAME	DUT PIN NUMBER	BREADBOARD BUS NAME	TERMINAL #/PIN
A/D Voltage Reference	V_{REF}	1	V_{REF}	P5
A/D Non-inverting Input	+IN	2	V_{IN}+	P2/1
A/D Inverting Input	–IN	3	V_{IN}–	P2/3
A/D Ground	GND	4	GND	P2/2
				P3/2
				P4/2 P1 All Even Pins
A/D Chip Select /Shut Down	CS/SHDN	5	CS	P1/47
A/D Digital Out	D_{OUT}	6	SDATA	P1/45
A/D Clock Input	DCLOCK	7	CLK	P1/43
A/D Power Supply	$+V_{CC}$	8	$+V_D$	P4/1
Auxiliary Breadboard Power Supply			$+V_{CC}$	P3/1
Auxiliary Breadboard Power Supply			$-V_{CC}$	P3/3
Isolated Bus			$\overline{CS}/SHDN_{ISO}$	P8/1
Isolated Bus			$\overline{SDATA}_{ISO}$	P8/2
Isolated Bus			$\overline{CLOCK}_{ISO}$	P8/3
Isolated Power			$+V_{ISO}$	P7/1
Isolated Ground Plane			GND_{ISO}	P7/2

TABLE IX. General Summary of External Pin Connections and Breadboard Bus Connections for the DEM-ADS78DIP Evaluation Fixture.

DESIGNATOR	DESCRIPTION	PART NUMBER	QTY	VENDOR(S)
U1	Single-Supply Op Amp, PDIP	OPA234P	1	Burr-Brown
U2	2.5V Reference, Surface Mount	REF1004C-2.5	1	Burr-Brown
U3	Single-Supply Analog Multiplexer	ADG608BN	1	Analog Devices
U4	Digital Buffer	74AC11004	1	T.I.
U5	DUT 8-pin, 12-Bit A/D Converter	ADS7816P	1	Burr-Brown
U6	32MHz Clock Oscillator	CTX129-ND	1	CTS (DigiKey #)
U7, U9	Dual D-Type Flip-Flop	74AC11074	2	T.I.
U10	4-Bit Synchronous Binary Counter	74HC163N	1	T.I.
U8	Dual Decade Counter	74HC390N	1	T.I.
R1-R3, R9-R12, R24, R27, R30, R33	100Ω, 0.125W, 1% MF Resistor	RN55C1000F	11	Dale
R4-R8, R21	1kΩ, 0.125W, 1%, MF Resistor	RN55C1001F	6	Dale
R15-R17, R22, R25, R28, R31	10kΩ, 0.125W, 1%, MF Resistor	RN55C1002F	7	Dale
R18-R20, R23, R26, R29, R32	100kΩ, 0.125W, 1%, MF Resistor	RN55C1003F	7	Dale
R13, R14	49.9Ω, 0.125W, 1%, MF Resistor	RN55C49R9	2	Dale
C1-C4, C10-C14	0.1µF, 50VX7R Ceramic Capacitor	CK05BX104K	9	Kemet
C9	47µF, 10V, 10%, Tantalum Dipped Radial	T350H476K010AS	1	Kemet
C5-C8	2.2µF, Tantalum Dipped/Radial, 25V, 10%	T350B225K025AS	4	Kemet
P1	25 x 2 Contact, Right-angle, Connector	IDH-50LP-SR3-TG	1	Robinson-Nugent
P2, P3, P8	3-Pin Term Block	ED300/3	3	On-Shore Technology
P4, P7	2-Pin Term Block	ED300/2	3	On-Shore Technology
P5, P6	BNC Connector, PCB Mount	KC-79-274-M06	2	King
J10, J7	Switch Low-Profile DIP	LD04	2	C&K Components
	Jumper Tops	SNT-100-BK-T-H	6	Samtec
	DEM-ADS78DIP Board	A2206-1 Rev C	1	Burr-Brown
U4 Socket	20-pin, DUT Socket	520AG-11-DES	1	Aries
U5 Socket	8-pin DUT Socket	508AG-11-DES	1	Augat
U6 Socket	14-pin Oscillator Socket	1107741	1	Augat

TABLE X. Parts List.

DESCRIPTION	PART NUMBER	QTY	VENDOR(S)
8-pin A/D Converter	ADS7822P	1	Burr-Brown
8-pin A/D Converter	ADS7817P	1	Burr-Brown
ADS7816 Product Data Sheet	PDS-1355	1	Burr-Brown
ADS7817 Product Data Sheet	PDS-1369	1	Burr-Brown
ADS7822 Product Data Sheet	PDS-1358	1	Burr-Brown
DEM-ADS78DIP Product Data Sheet	LI-491	1	Burr-Brown

TABLE XI. Packing List.

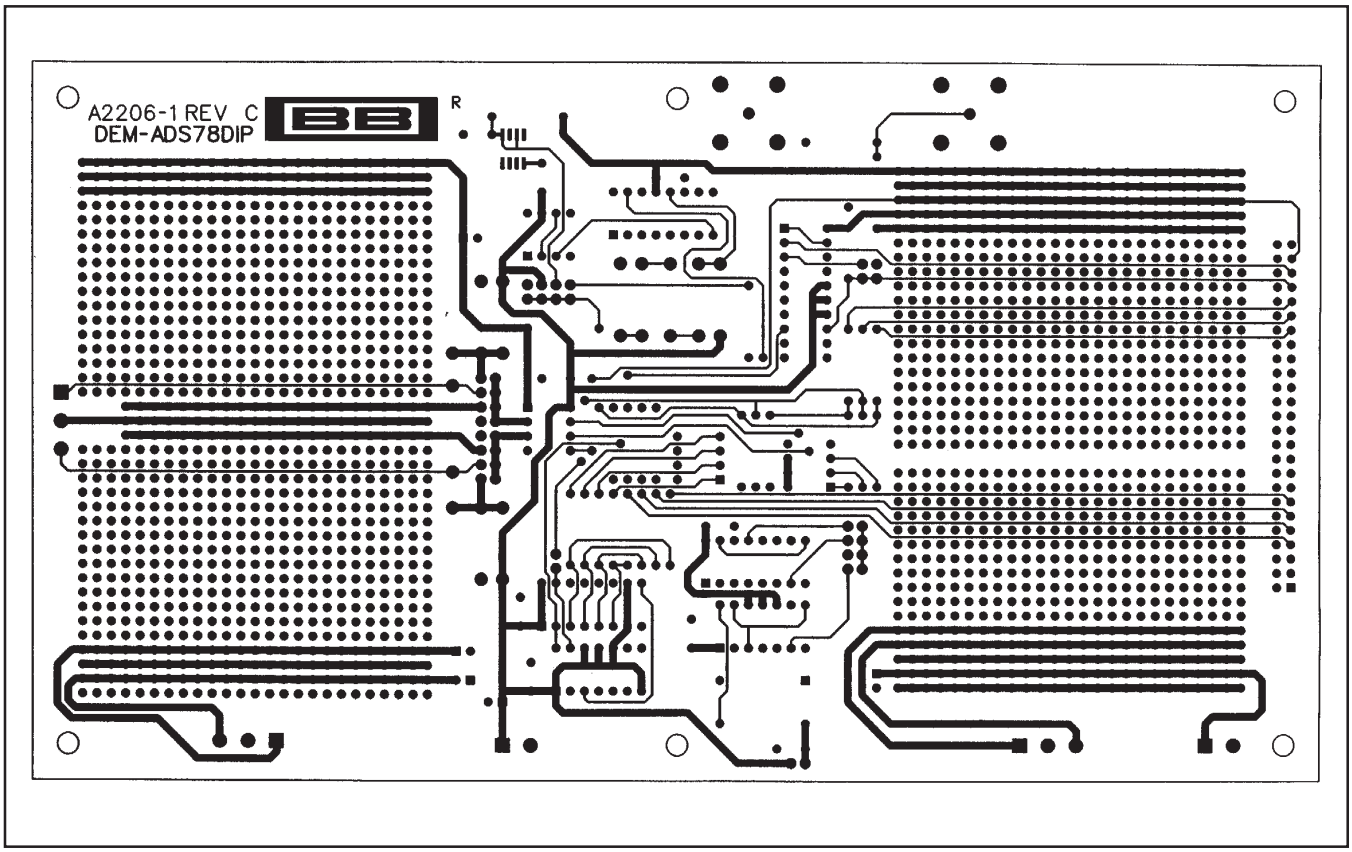

FIGURE 4. Component Side.

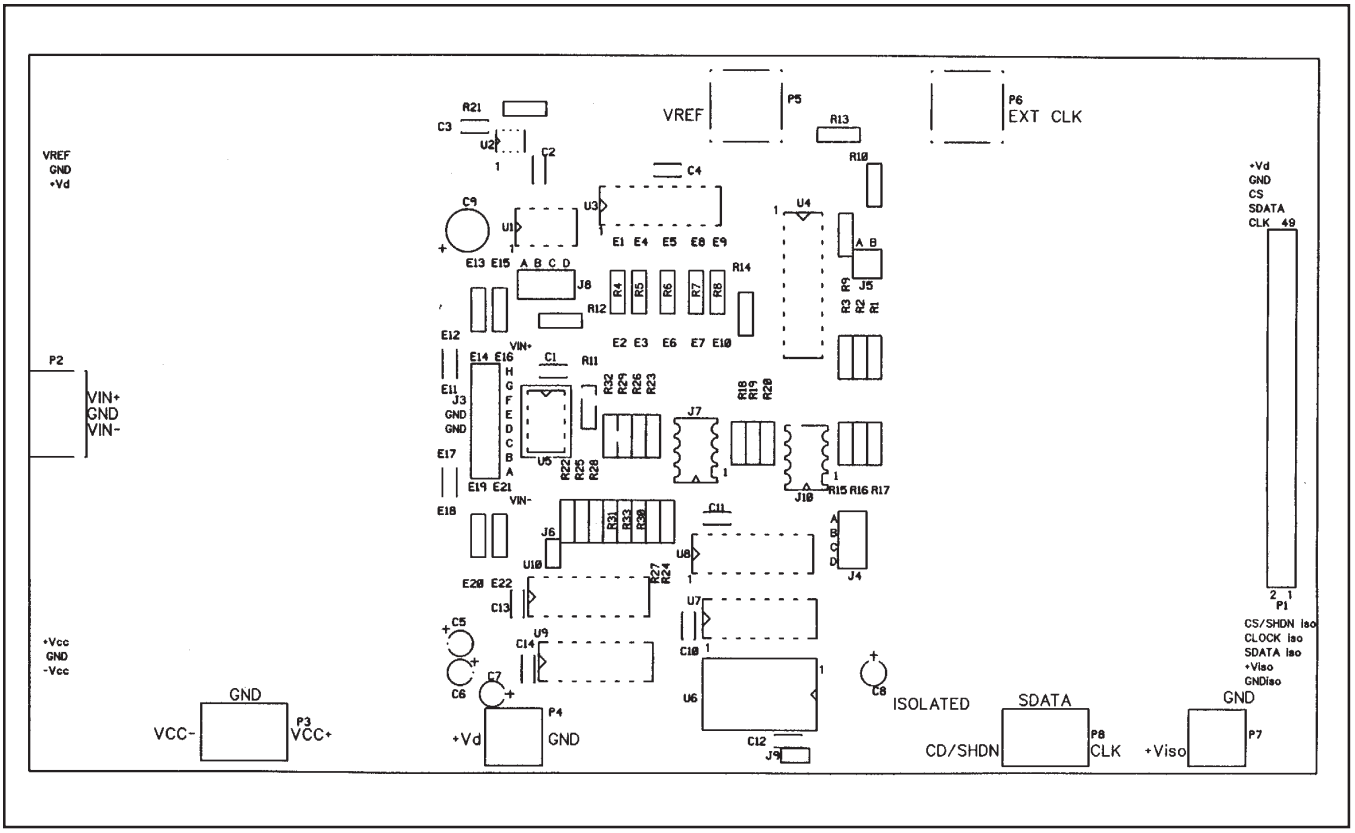

FIGURE 5. Silkscreen.

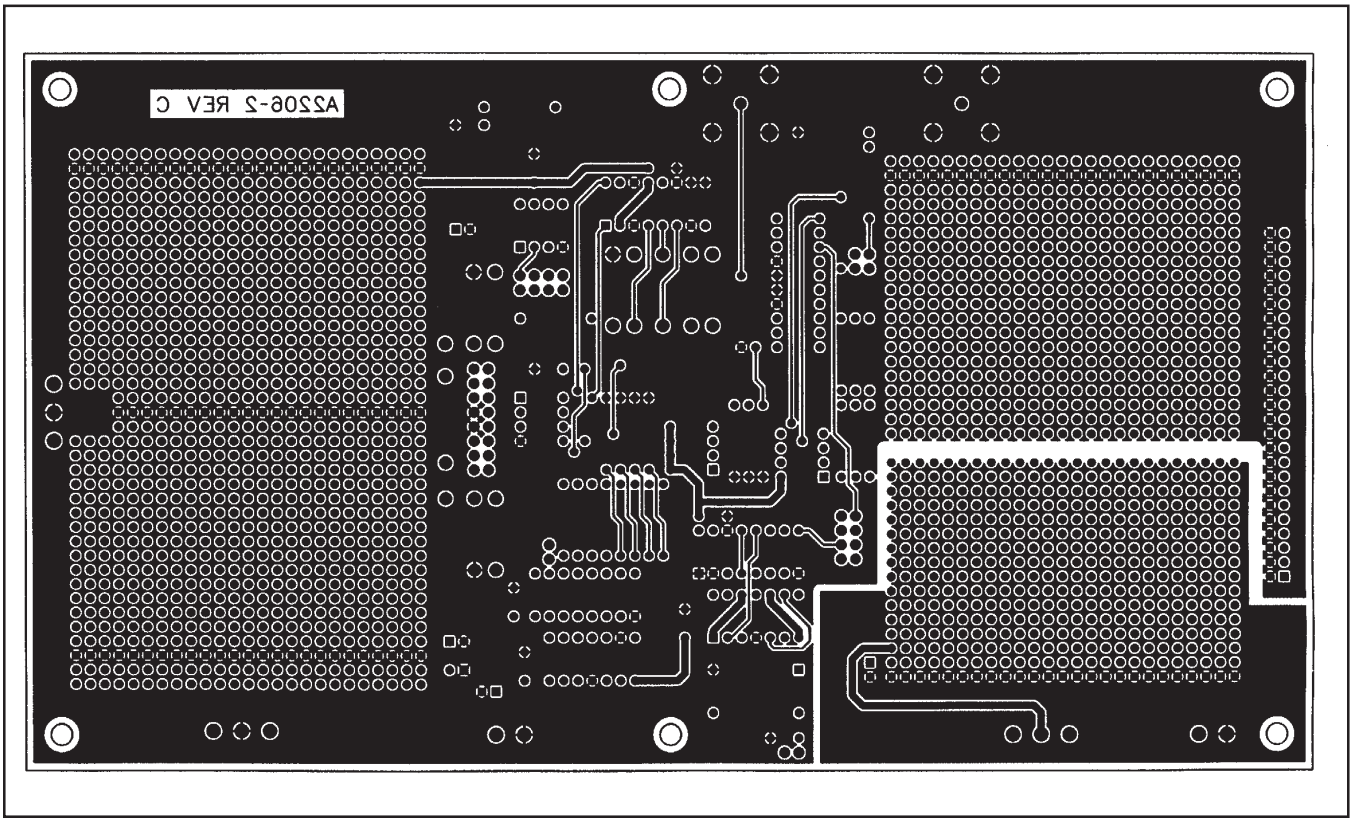

FIGURE 6. Solder Side.

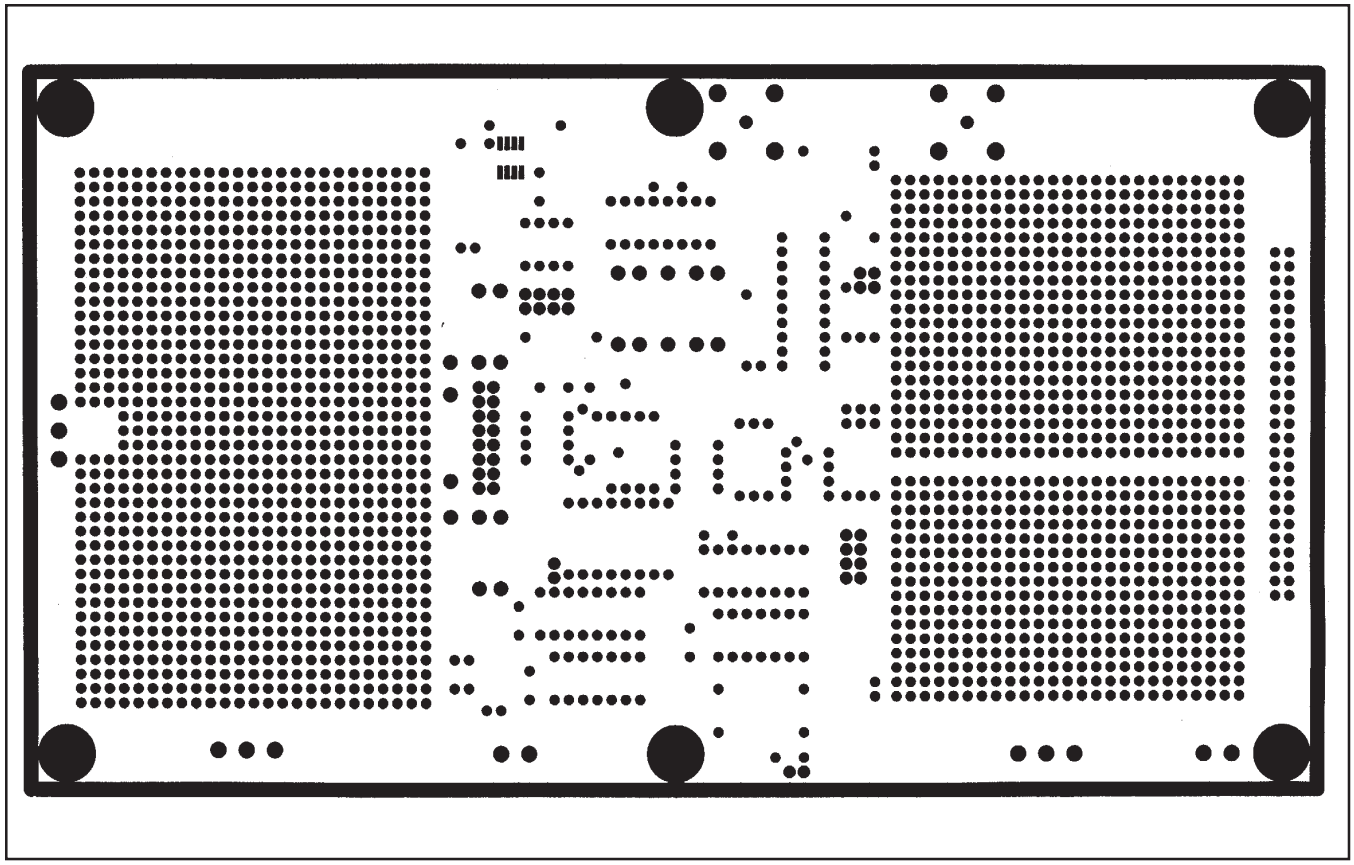

FIGURE 7. Top Soldermask.