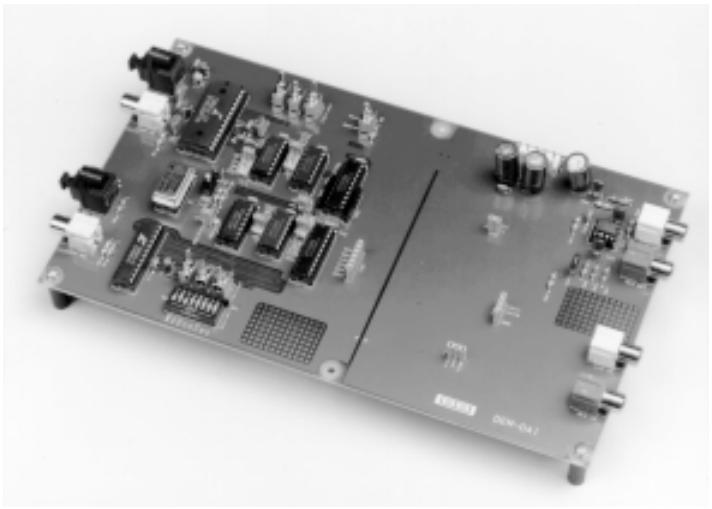
BURR - BROWN®

DEM-DAI
EVALUATION FIXTURE



FEATURES

- DIGITAL AUDIO RECEIVER AND TRANSMITTER SUPPORTS S/PDIF DIGITAL AUDIO INTERFACE (both RCA coaxial cable and optical connections)
- PROGRAMMABLE SYSTEM CLOCK SOURCE: Digital Audio Receiver or Crystal Oscillator
- PROGRAMMABLE SYSTEM CLOCK RATE: 256f_S, 384f_S, or 512f_S
- NORMAL OR INVERTED SYSTEM CLOCK INPUT FOR DIGITAL AUDIO TRANSMITTER
- MASTER OR SLAVE MODE OPERATION
- RECEIVER AND TRANSMITTER MODE SELECTION VIA TOGGLE SWITCHES
- DIP SWITCH FOR SETTING DIGITAL TRANSMITTER FLAGS
- HEADER CONNECTIONS ACCEPT DEM-PCM DEMO BOARDS
- RCA JACKS FOR STEREO AUDIO INPUTS AND OUTPUTS
- ON-BOARD STEREO DAC POST FILTER
- POWER SUPPLY CONNECTOR FOR DIGITAL AND ANALOG POWER SUPPLIES
- OPERATES FROM A SINGLE +5V SUPPLY FOR THE DIGITAL AUDIO INTERFACE SECTION
- DAC POST FILTER OPERATES FROM ±5V TO ±15V

DESCRIPTION

The DEM-DAI demonstration board provides a standard platform for evaluating Burr-Brown digital audio products including stereo DAC, ADC and CODEC devices. The DEM-DAI board includes a digital audio receiver and transmitter, along with their associated support circuitry. The receiver and transmitter accept and output S/PDIF digital audio streams via RCA and optical connections. The DEM-DAI board also includes an on-board crystal oscillator/divider circuit for generating the required audio clocks independent of the digital audio receiver.

In addition to the digital audio interface and timing circuits, there are connectors for DEM-PCM demo boards, power supplies, and stereo audio inputs and outputs. On-board switches and jumpers are used to configure the DEM-DAI board for use with a variety of DEM-PCM demo boards. An on-board DAC post filter circuit is also included and is located near the stereo audio output connectors.

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Printed in U.S.A. December, 1998

HARDWARE DESCRIPTION

A functional block diagram of the DEM-DAI board is shown in Figure 1. It illustrates the basic connections between the receiver, transmitter, crystal oscillator/divider, configuration controls, and the PCM demo board. Connectors for external interfaces are also shown. The following paragraphs provide a more detailed description of various blocks and options.

DIGITAL AUDIO RECEIVER

The DEM-DAI board includes a digital audio receiver (Crystal Semiconductor CS8412). This receiver provides the interface to a S/PDIF digital audio source, such as an Audio Precision System One or Two, a DAT, CD, or DVD player. For more information, consult the Crystal data sheet for this device.

Operational details for this device, as related to the DEM-DAI board, are provided in the section entitled "Setting the Configuration Controls" in this data sheet.

DIGITAL AUDIO TRANSMITTER

The DEM-DAI board includes a digital audio transmitter (Crystal Semiconductor CS8402A). This transmitter provides the interface to a S/PDIF digital audio receiver, such as an Audio Precision System One or Two, or an A/V receiver. For more information, consult the Crystal data sheet for this device.

Operational details for this device, as related to the DEM-DAI board, are provided in the section entitled "Setting the Configuration Controls" in this data sheet.

CLOCK SOURCES

The DEM-DAI board supports two sources for the system clock, and three sources for the left/right clock (LRCK) and bit clock (BCK). The system clock can be generated by the digital audio receiver or the crystal oscillator/divider circuit. The LRCIN and BCK can be generated by the digital audio receiver, the crystal oscillator/divider circuit, or by a Master mode PCM device, such as the PCM1800 Stereo ADC.

See the section entitled "Typical DEM-DAI Test Configurations" for more information regarding the setup for testing PCM audio products.

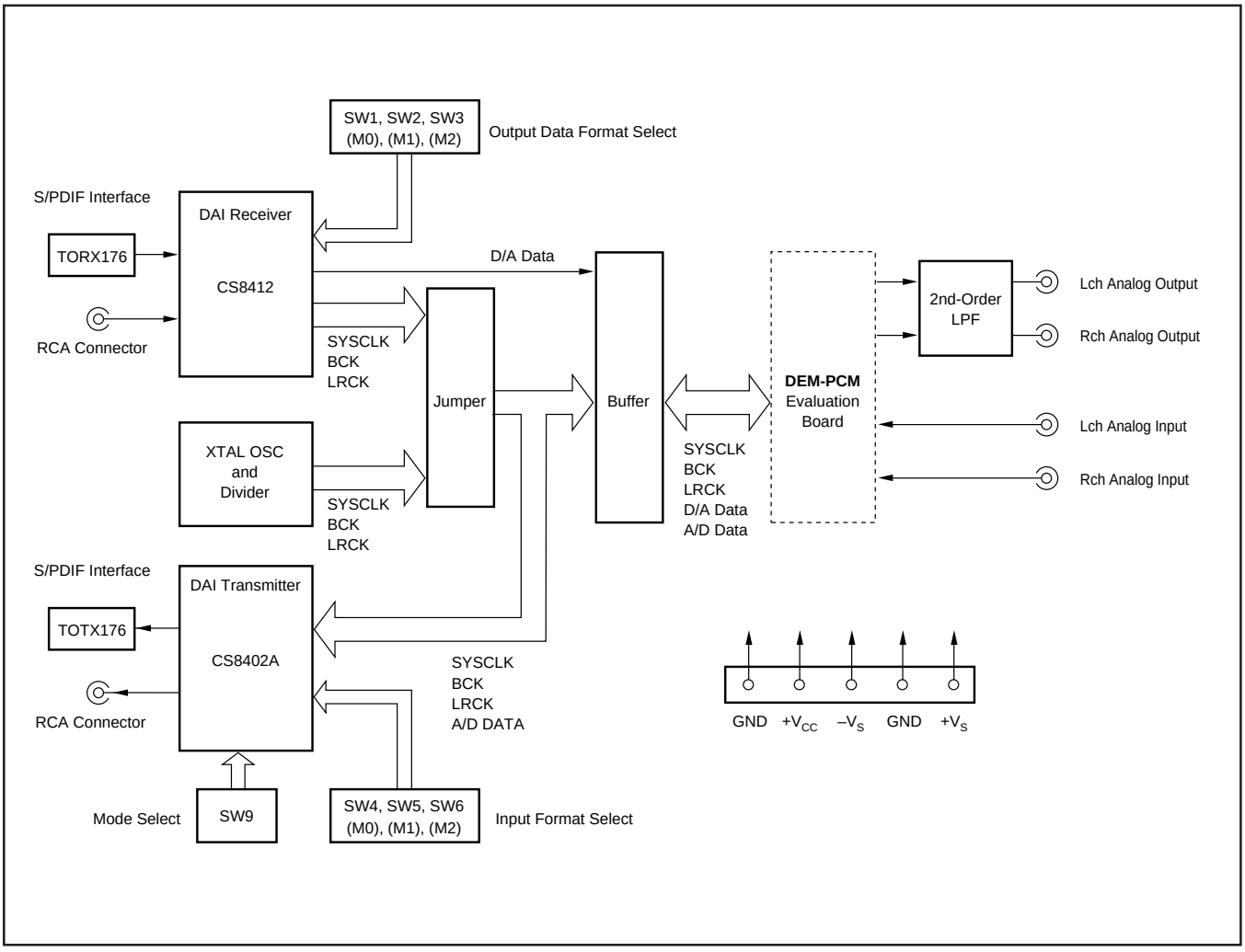


FIGURE 1. DEM-DAI Functional Diagram.

AUDIO INPUTS AND OUTPUTS

Analog-to-digital converter (ADC) and digital-to-analog converter (DAC) analog audio connections are made via RCA connectors, and can be sourced or measured using an analyzer, such as the Audio Precision System One or Two. The RCA jacks also provide simple interconnection with consumer and professional audio systems.

ON-BOARD DAC POST FILTER

The DEM-DAI board includes an on-board DAC post filter. This is a second-order lowpass active filter configured in a multiple feedback arrangement. The filter is comprised of op amp U11 and its associated circuitry. The OPA2134 dual op amp is the recommended device for U11.

CONFIGURATION CONTROLS

The DEM-DAI board includes a number of switches and jumpers which are used to configure the digital audio interface and clocks. See the section entitled "Setting the Configuration Controls" for details on configuring DEM-DAI board options.

POWER SUPPLIES

Power supply connections for both the digital audio interface and DAC post filter circuit are provided using connector CN1.

DEMO BOARD INTERFACE

DEM-PCM demo boards which are compatible with the DEM-DAI board are connected using headers CN2 through CN5.

CN2 provides the connection to the system clock and the audio serial port interface.

CN3 connects the left and right DAC outputs to the on-board post filter, with the output of the filters connected to RCA jacks J3 and J4.

CN4 connects the left and right ADC inputs to the J5 and J6 RCA jacks.

CN5 connects to the $+V_{CC}$ power supply and ground.

SETTING THE CONFIGURATION CONTROLS

This section describes the controls used to set the configuration of the DEM-DAI board.

MODE SWITCHES

Switches SW1, SW2, and SW3 are used to set the output data format generated by the digital audio receiver. Table I shows the switch settings and the corresponding format selections. Figures 2a through 2d show the LRCK, BCK, and output data (DATAIN) waveforms for each format. The PCM device format selection, made through either hardware or software controls on the corresponding DEM-PCM demo board, must match the format selection made with switches SW1 through SW3.

SW3 (M2)	SW2 (M1)	SW1 (M0)	FORMAT
L	L	L	16-Bit to 24-Bit, Left-Justified
L	H	L	I^2S
H	L	H	16-Bit, MSB-First, Right-Justified
H	H	L	18-Bit, MSB-First, Right-Justified

TABLE I. Digital Audio Receiver Output Data Format.

Switches SW4, SW5, and SW6 are used to set the input data format required for the digital audio transmitter. Table II shows the switch settings and the corresponding format selections. Figures 3a through 3d show the LRCK, BCK, and input data (DATAOUT) waveforms for each format. The PCM device format selection, made through either hardware or software controls on the corresponding DEM-PCM demo board, must match the format selection made with switches SW4 through SW6.

SW6 (M2)	SW5 (M1)	SW4 (M0)	FORMAT
L	L	H	16-Bit to 24-Bit, Left-Justified
H	L	L	I^2S
H	L	H	16-Bit, MSB-First, Right-Justified
H	H	L	18-Bit, MSB-First, Right-Justified

TABLE II. Digital Audio Transmitter Input Data Format.

When using the DEM-DAI board to test PCM DACs and the transmitter is not in use, it is recommended that switches SW4, SW5, and SW6 be set to match the settings of SW1, SW2, and SW3 to ensure proper DEM-DAI board operation.

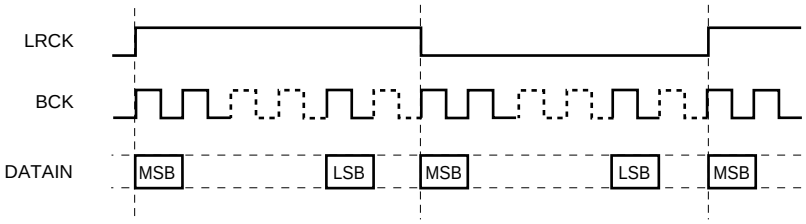
Switch SW7 is used to select Master or Slave mode for devices which support them. In Master mode, the PCM device generates LRCK and BCK. In Slave mode, the LRCK and BCK are generated by either the digital audio receiver or the crystal oscillator/divider circuit, and is then provided to the corresponding PCM device. The Master/Slave mode selection on the DEM-PCM demo board must correspond directly to the selection made with SW7. Table III shows the switch settings and corresponding mode selections.

SW7	MODE
SLAVE	Slave Mode: LRCK and BCK generated by DIR or crystal oscillator/divider.
MASTER	Master Mode: LRCK and BCK generated by PCM device.

TABLE III. Master/Slave Mode Selection.

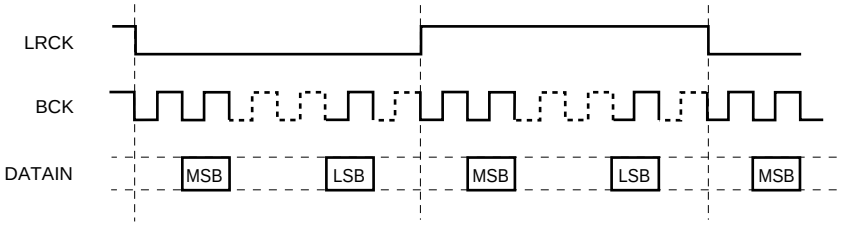
a) Format: 16-Bit to 24-Bit, Left-Justified

SW3	SW2	SW1
L	L	L



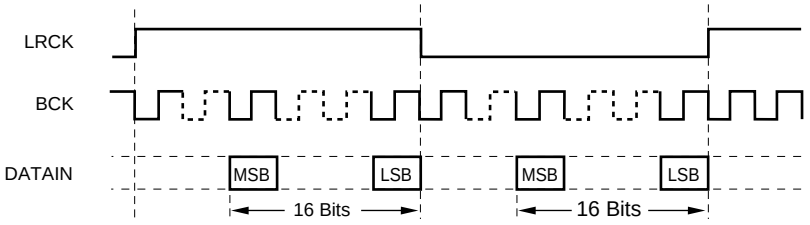
b) Format: 16-Bit to 24-Bit, I²S

SW3	SW2	SW1
L	H	L



c) Format: 16-Bit, MSB-First, Right-Justified

SW3	SW2	SW1
H	L	H



d) Format: 18-Bit, MSB-First, Right-Justified

SW3	SW2	SW1
H	H	L

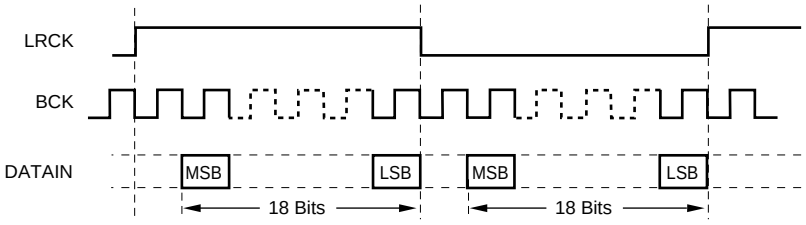
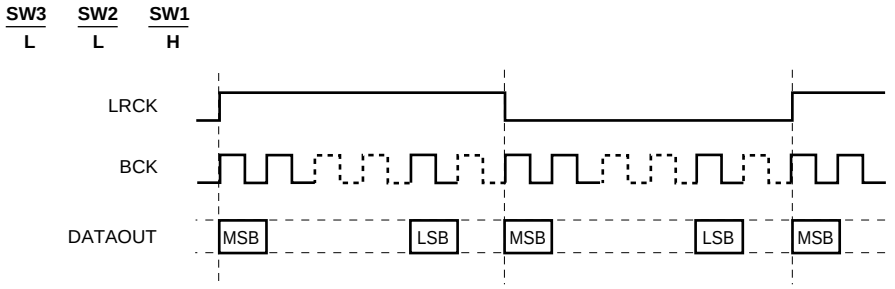
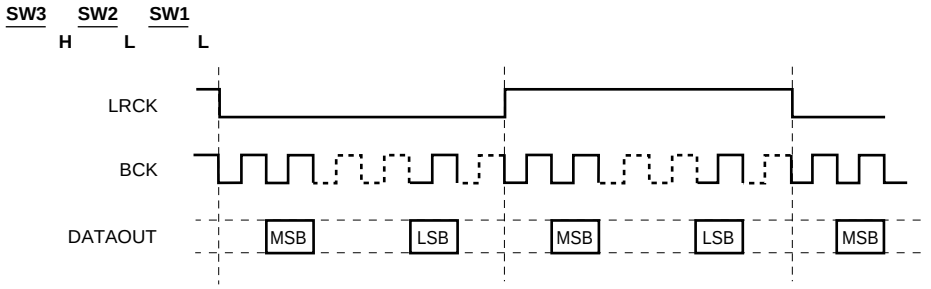


FIGURE 2. Digital Audio Receiver Output Data Formats.

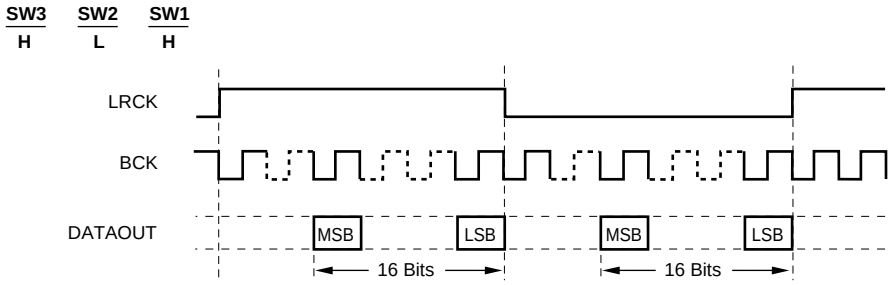
a) Format: 16-Bit to 24-Bit, Left-Justified



b) Format: 16-Bit to 24-Bit, I²S



c) Format: 16-Bit, MSB-First, Right-Justified



d) Format: 18-Bit, MSB-First, Right-Justified

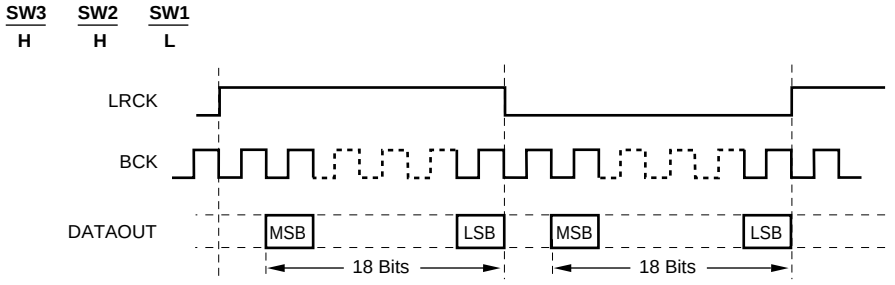


FIGURE 3. Digital Audio Transmitter Input Data Formats.

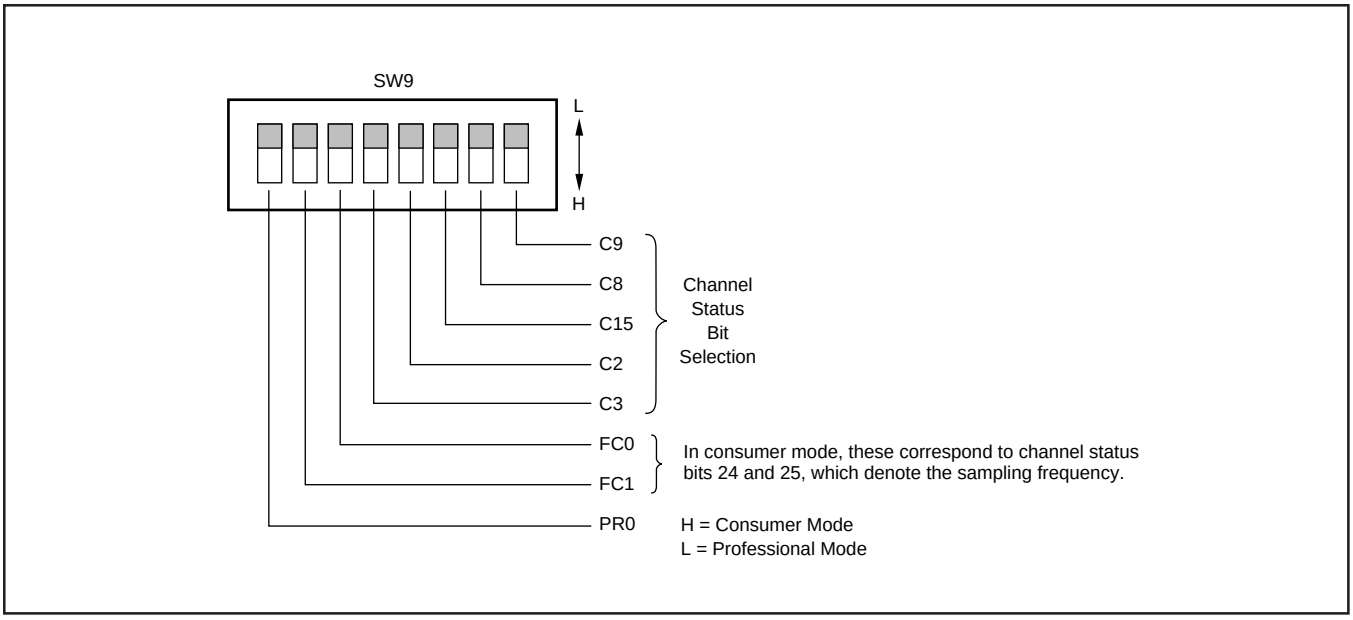


FIGURE 4. Digital Audio Transmitter Status Bit Switch.

DIGITAL AUDIO TRANSMITTER FLAGS

Switch SW9 is a DIP switch used to setup additional digital audio transmitter options. Figure 4 shows an illustration of SW9, with each switch labeled with its appropriate designator. The following paragraphs explains the function of each of the DIP switch segments.

The PRO switch is used to select Consumer or Professional mode. Set this switch HIGH for Consumer mode, and LOW for Professional mode. This pin should also be set LOW when using the transmitter in Transparent mode.

The PRO switch selection, either Consumer or Professional, defines the function of the next seven switches. For most DEM-DAI applications, set the mode to Consumer (PRO = HIGH). Only the consumer definitions are given here. Consult the CS8402A data sheet for information regarding the Professional mode definitions.

FC0 and FC1, corresponding to channel status bits 24 and 25, denote the sampling frequency. Table IV shows the switch settings and their corresponding selections.

FC0	FC1	SAMPLING FREQUENCY
0	0	44.1kHz
0	1	48kHz
1	0	32kHz
1	1	44.1kHz (CD submode)

TABLE IV. Sampling Frequency Flag Settings.

The remaining five switches correspond to channel status bit selections. C2, C3, C8,C9, and C15 correspond to channel status bits 2, 3, 8, 9, and 15. Consult the AES specification or the CS8402A data sheet for the definition of these bits in Consumer and Professional modes.

JUMPERS

There are six jumpers that are used to setup clocking options. They are described in the following paragraphs.

JP1 is used to select the system clock source. Figure 5 shows the header block with descriptions for each of the three options.

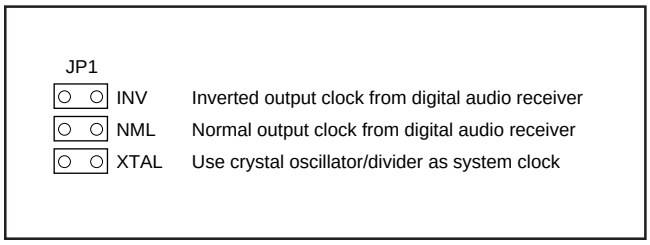


FIGURE 5. System Clock Source Selection.

JP2 is used to select the bit clock (BCK) source. Figure 6 shows the header block with descriptions for each of the four options. Regardless of the BCK source selected, the bit clock rate will be 64 • f_S.

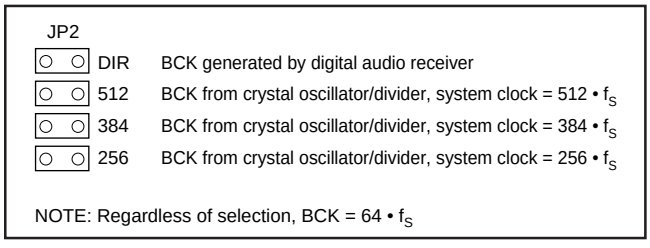


FIGURE 6. Bit Clock Source Selection.

JP3 is used to select the left/right clock (LRCK) source. Figure 7 shows the header block with descriptions for each of the four options. The left/right clock rate is equal to the sampling frequency.

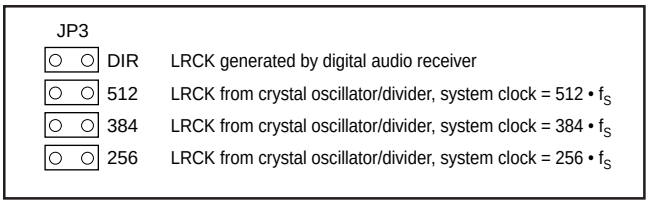


FIGURE 7. Word Clock Source Selection.

JP4 is used to select the system clock rate when using the crystal oscillator as the system clock source. Figure 8 shows the header block with descriptions for the two available options. The 256/512 • f_S rate is determined by the frequency of the crystal oscillator used.

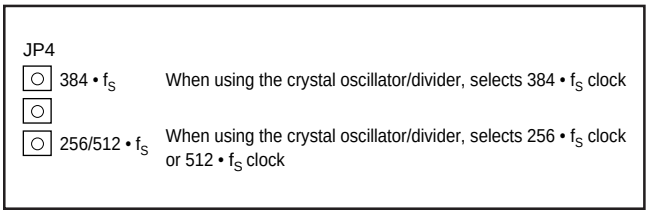


FIGURE 8. System Clock Rate Selection When Using the Crystal Oscillator/Divider.

JP5 is used to select the source of the digital audio transmitter's system clock. Figure 9 shows the header block with descriptions for each of the four options. Regardless of the source selected, the rate will be 128 • f_S.

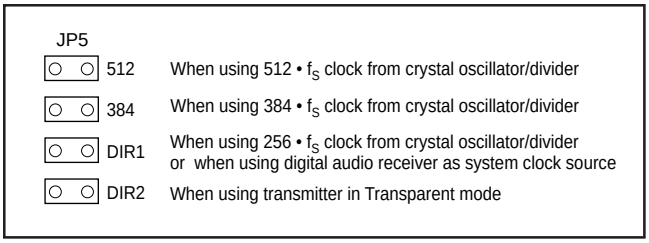


FIGURE 9. Digital Audio Transmitter Source Selection.

JP6 is used to select the polarity of the bit clock (BCK) used for the digital audio transmitter. Figure 10 shows the header block with descriptions for the two available options.

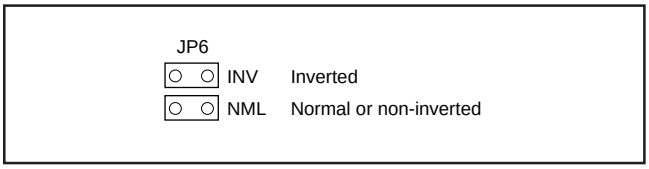


FIGURE 10. Digital Audio Transmitter BCK Polarity Selection.

TYPICAL DEM-DAI TEST CONFIGURATIONS

This section provides general information for configuring the DEM-DAI board for testing Burr-Brown's PCM audio devices. Refer to the individual PCM product and demonstration board data sheets for more detailed information regarding product operation and demo board configuration.

D/A CONVERTERS

The general test configuration for PCM DACs is shown in Figure 11. This setup uses the CS8412 receiver to recover the audio clocks and data from a S/PDIF data stream. The system clock, left/right clock, bit clock, and data are then routed from the receiver to the DEM-PCM demo board to operate the PCM DAC. The left and right outputs of the DAC are routed to the on-board post filters to remove out-of-band noise and otherwise band limit the output signal. The output of the filters is available at the J3 and J4 RCA connectors.

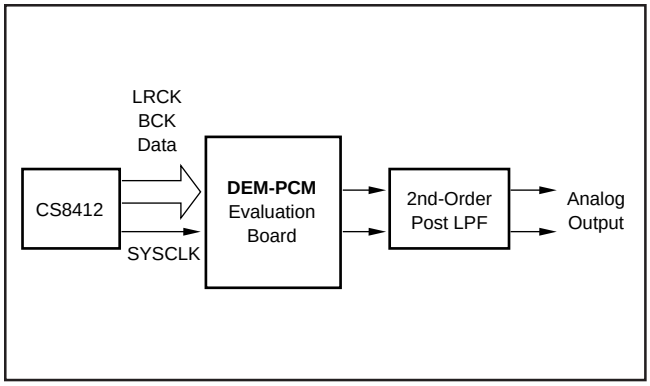


FIGURE 11. DAC Configuration.

Table V shows the DEM-DAI board switch and jumper configurations for PCM DAC testing.

SWITCH/JUMPER	CONFIGURATION
SW1, SW2, SW3	Setup to match the corresponding DAC data format.
SW4, SW5, SW6	Setup to match SW1, SW2, and SW3.
SW7	Set to Slave mode.
SW9	PRO = H; FC0 and FC1 = sample rate in use; all others = L.
JP1	Set to NML.
JP2	Set to DIR.
JP3	Set to DIR.
JP4	Not used, but set to 256/512 • f_S.
JP5	Set to DIR1.
JP6	Not used, but set to NML.

TABLE V. Switch and Jumper Settings for PCM DAC Testing.

A/D CONVERTERS

There are three configurations for testing PCM ADC products. They are shown in Figures 12, 13, and 14.

This includes two Slave mode configurations and one Master mode configuration.

Figure 12 shows the ADC Slave Configuration #1. This setup uses the CS8412 receiver to recover the audio clocks from a S/PDIF data stream. The clocks are supplied to both the ADC and the CS8402A transmitter. Data from the ADC is routed to the CS8402A transmitter and output as a S/PDIF data stream on both an optical transmitter (U10) and a RCA connector (J2).

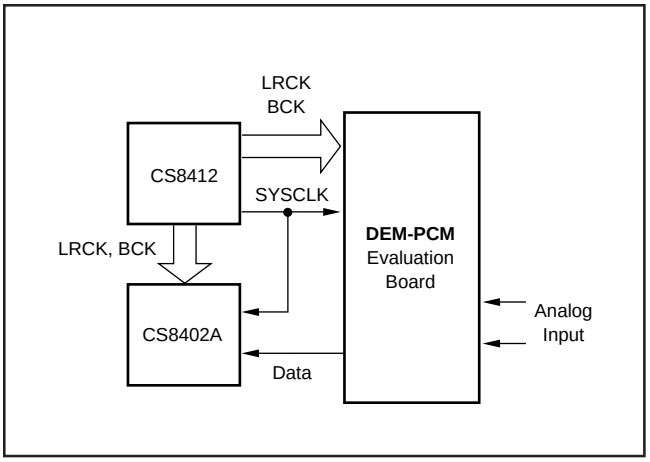


FIGURE 12. ADC Slave Configuration #1.

Table VI shows the DEM-DAI board switch and jumper configurations for ADC Slave Configuration #1.

SWITCH/JUMPER	CONFIGURATION
SW1, SW2, SW3	Setup to match the corresponding ADC data format.
SW4, SW5, SW6	Setup to match the corresponding ADC data format.
SW7	Set to Slave mode.
SW9	PRO = H; FC0 and FC1 = sample rate in use; all others = L.
JP1	Set to NML.
JP2	Set to DIR.
JP3	Set to DIR.
JP4	Not used, but set to 256/512 • f_S.
JP5	Set to DIR1.
JP6	Set to NML.

TABLE VI. Switch and Jumper Settings for ADC Slave Configuration #1.

Figure 13 shows the ADC Slave Configuration #2. The crystal oscillator/divider circuit is used to generate the clocks for the ADC and CS8402A transmitter. The CS8412 receiver is not used in this configuration. Data from the ADC is routed to the CS8402A and transmitted as an S/PDIF data stream at both optical (U10) and RCA (J2) connectors.

Unlike ADC Slave Configuration #1, the user must choose the system clock rate and configure the jumpers for system, left/right, and bit clocks accordingly. As an example, if you select the system clock to be 512 • f_S, then jumpers JP2 through JP5 must be set for 512 • f_S operation.

ADC Slave Configuration #2 does not support I^2S format. It only supports standard right or left justified data formats.

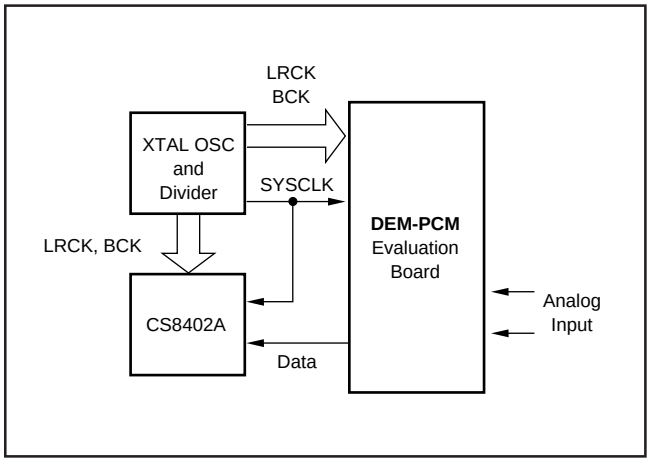


FIGURE 13. ADC Slave Configuration #2.

Table 7 shows the DEM-DAI board switch and jumper configurations for ADC Slave Configuration #2

SWITCH/JUMPER	CONFIGURATION
SW1, SW2, SW3	Setup to match the SW4, SW5, and SW6 settings.
SW4, SW5, SW6	Setup to match the corresponding ADC data format.
SW7	Set to Slave mode.
SW9	PRO = H; FC0 and FC1 = sample rate in use; all others = L.
JP1	Set to XTAL.
JP2	Set to 256, 384, or 512.
JP3	Set to 256, 384, or 512.
JP4	Set to 256/512 • f_S or 384 • f_S.
JP5	Set to 384 • f_S, 512 • f_S, or DIR1 (for 256 • f_S XTAL operation).
JP6	Set to NML.

TABLE VII. Switch and Jumper Settings for ADC Slave Configuration #2.

Figure 14 shows the ADC Master configuration. The ADC generates all of the serial interface clocks in this configuration. The system clock is derived from the crystal oscillator/divider circuit. The clocks and data from the ADC are routed to the CS8402A and transmitted as a S/PDIF data stream at both optical (U10) and RCA (J2) connectors.

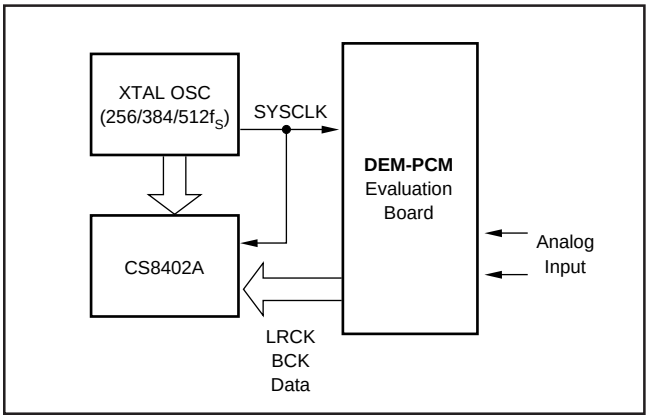


FIGURE 14. ADC Master Configuration.

Table VIII shows the DEM-DAI board switch and jumper configurations for ADC Master configuration.

SWITCH/JUMPER	CONFIGURATION
SW1, SW2, SW3	Setup to match the SW4, SW5, and SW6 settings.
SW4, SW5, SW6	Setup to match the corresponding ADC data format.
SW7	Set to Master mode.
SW9	PRO = H; FC0 and FC1 = sample rate in use; all others = L.
JP1	Set to XTAL.
JP2	Remove jumper.
JP3	Remove jumper.
JP4	Set to 256/512 • f_S or 384 • f_S.
JP5	Set to 384 • f_S, 512 • f_S, or DIR1 (for 256 • f_S XTAL operation).
JP6	Set to NML.

TABLE VIII. Switch and Jumper Settings for ADC Master Configuration.

STEREO AUDIO CODEC

Figure 15 shows the CODEC configuration. In this mode, the CS8412 is used to recover the audio clocks and data from a S/PDIF data stream. The clocks are supplied to the CODEC and the CS8402A transmitter. Data flows from the CS8412 receiver to the CODEC data input, and from the CODEC data output to the CS8402A transmitter.

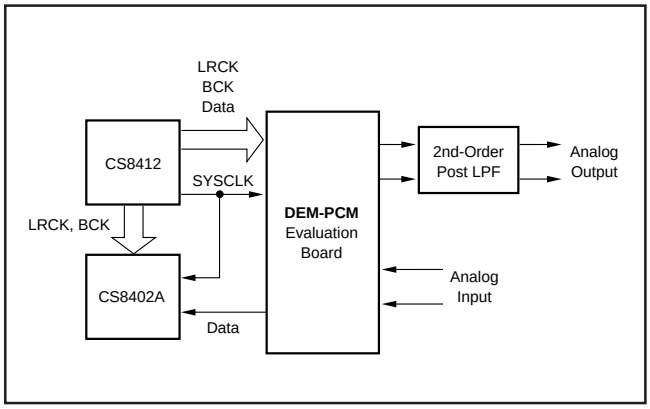


FIGURE 15. CODEC Configuration.

Table IX shows the DEM-DAI board switch and jumper configurations for CODEC configuration.

SWITCH/JUMPER	CONFIGURATION
SW1, SW2, SW3	Setup to match the corresponding CODEC input data format.
SW4, SW5, SW6	Setup to match the corresponding CODEC output data format.
SW7	Set to Slave mode.
SW9	PRO = H; FC0 and FC1 = sample rate in use; all others = L.
JP1	Set to NML.
JP2	Set to DIR.
JP3	Set DIR.
JP4	Not used, but set to 256/512 • f_S.
JP5	Set to DIR1.
JP6	Set NML.

TABLE IX. Switch and Jumper Settings for ADC Master Configuration.

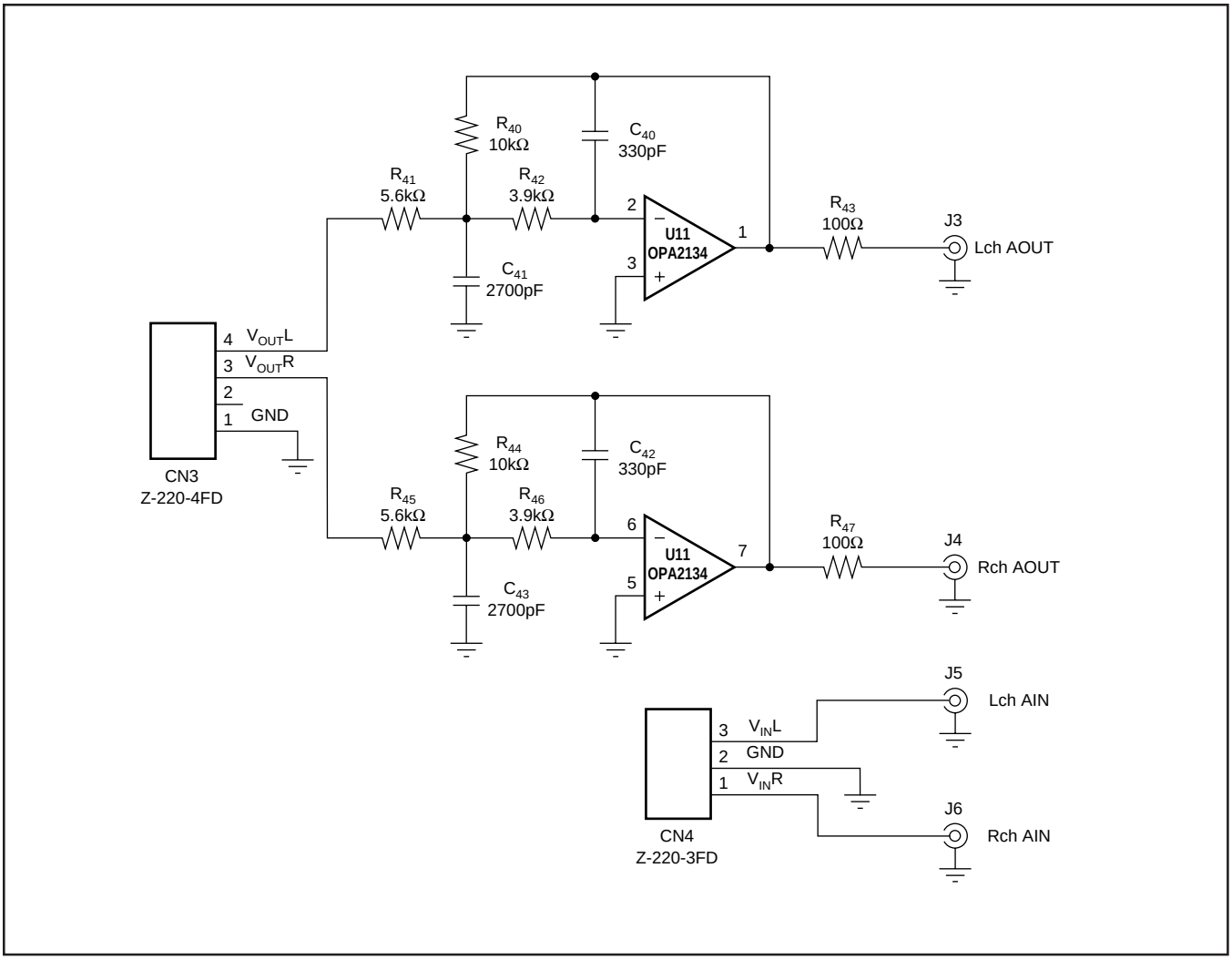


FIGURE 16. DAC Post Filter.

SCHEMATICS

Schematics for the DEM-DAI board are shown in Figures 16 through 18. Figure 16 shows the analog inputs, DAC post filter, and analog outputs. Figure 17 shows the power supply connections. Figures 18a and 18b detail the digital audio receiver, transmitter, and crystal oscillator/divider circuit. Also shown is the various switches and jumpers used to set the board configuration.

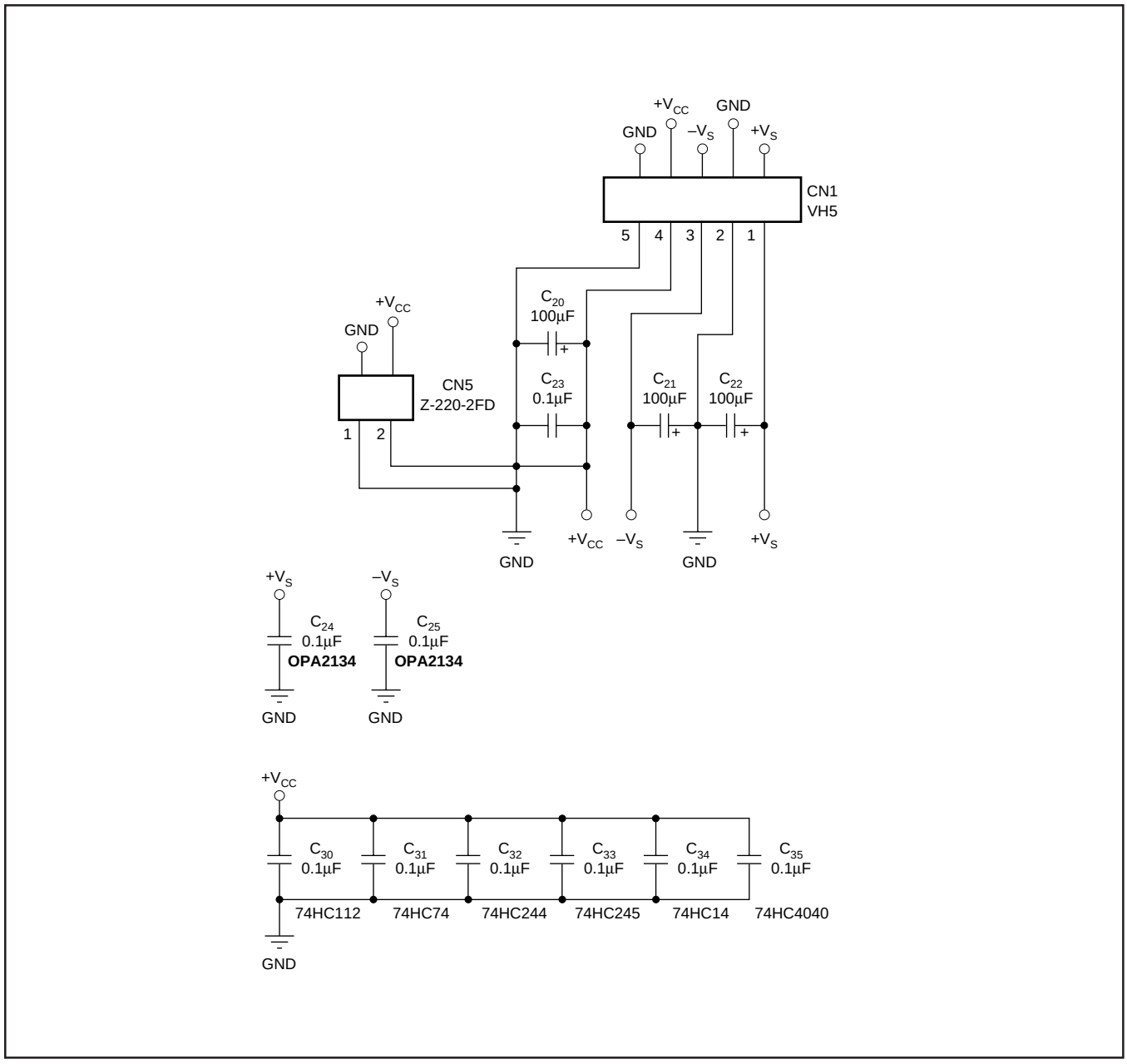


FIGURE 17. Power Supply Connections.

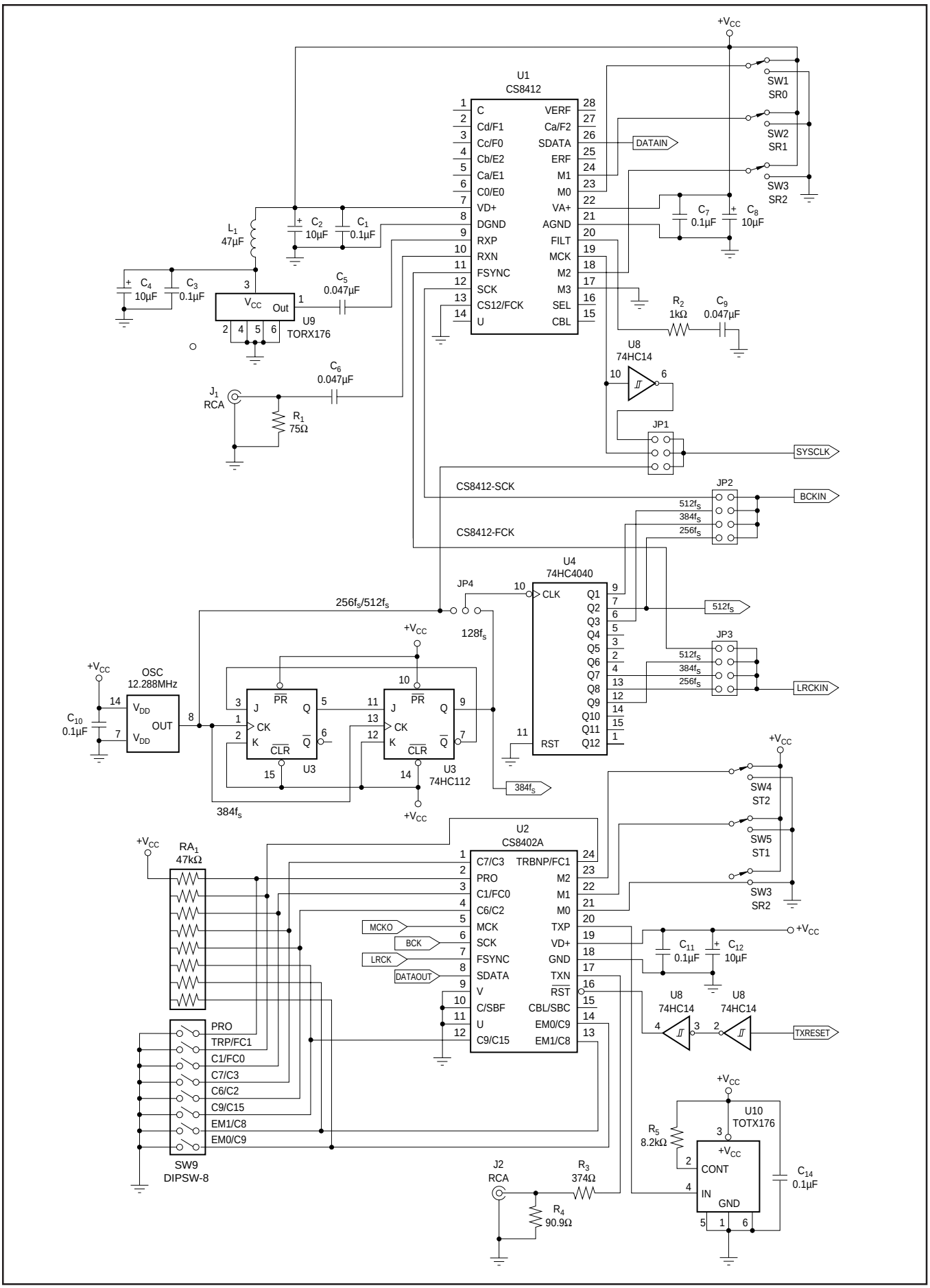


FIGURE 18a. Digital Audio Interface.

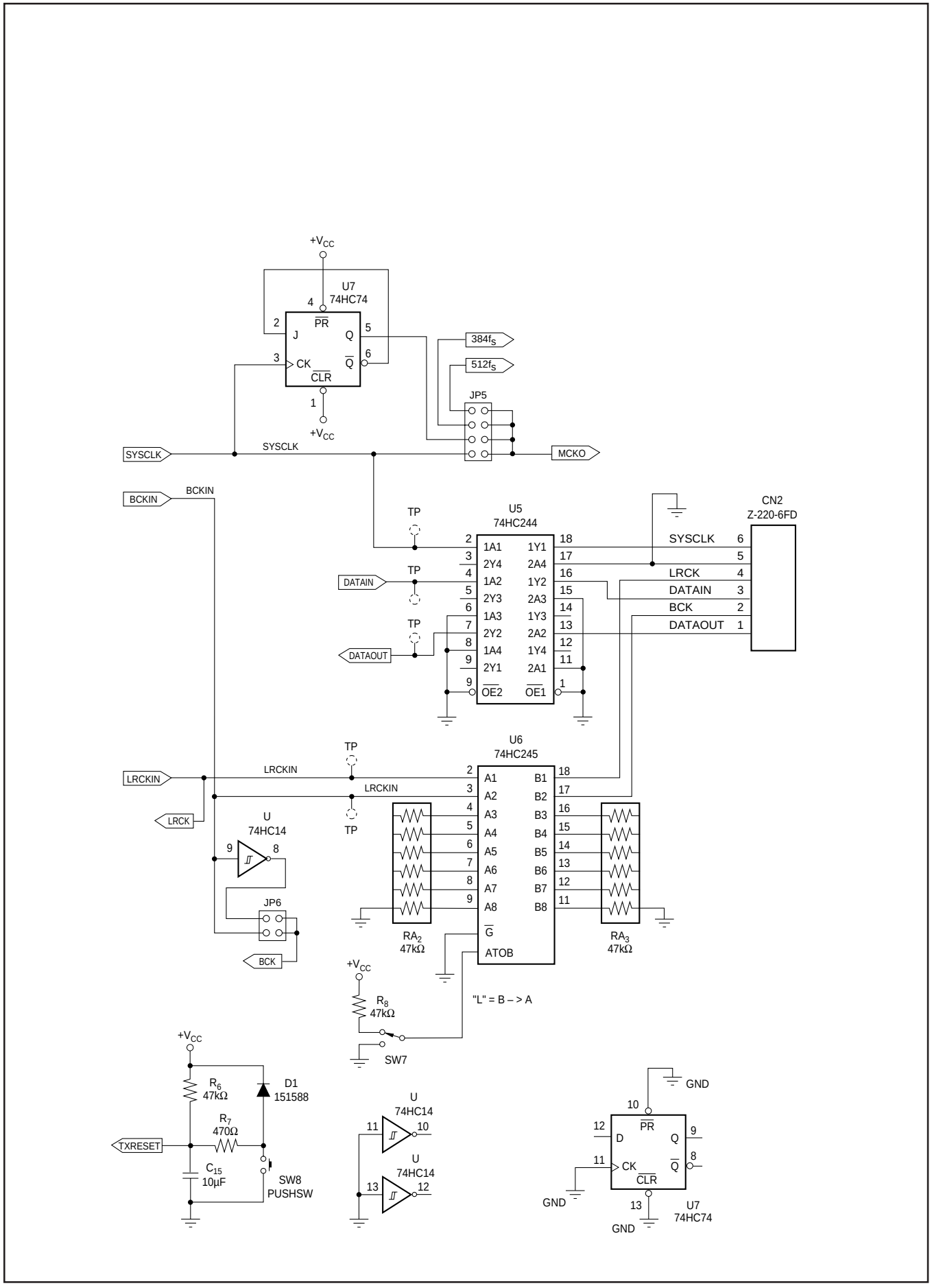


FIGURE 18b. Buffers and Miscellaneous Circuitry.