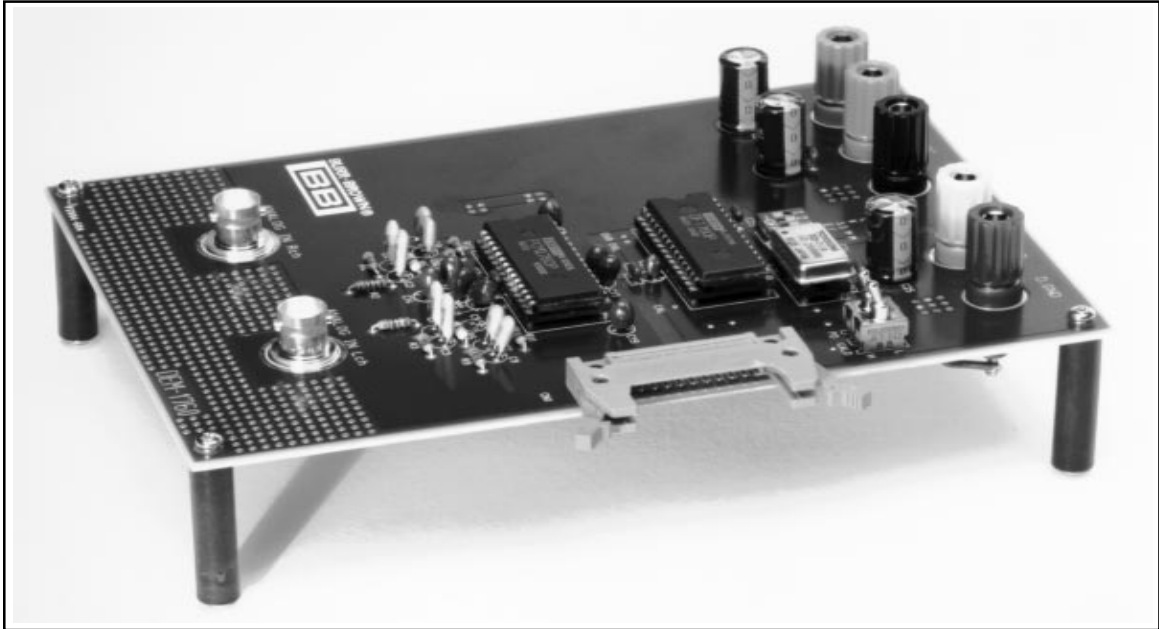




## DEM-PCM1760 EVALUATION FIXTURE



### FEATURES

- COMPLETE 20-BIT STEREO A/D CONVERSION SYSTEM
- 20-BIT A/D CONVERTER: PCM1760
- HIGH PERFORMANCE DIGITAL FILTER: DF1760
- SERIAL DIGITAL INTERFACE
- HIGH PERFORMANCE  
THD+N (F/S): 0.0015%  
Dynamic Range: 108dB (EIAJ)  
S/N Ratio: 108dB (EIAJ)
- ANALOG INPUT:  $\pm 2.5V$
- POWER SUPPLY:  $\pm 5V$ , +5V
- DIRECT INTERFACE TO DEM-PCM1702
- BOARD SIZE: 182mm x 128mm

### DESCRIPTION

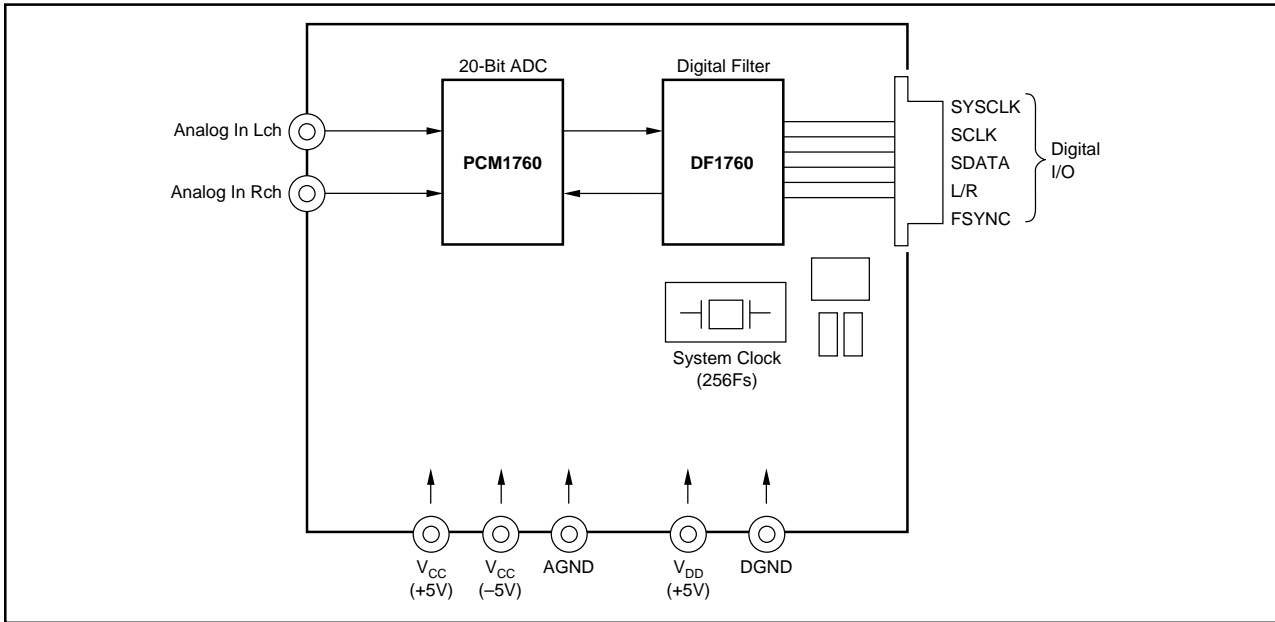
The DEM-PCM1760 is an evaluation fixture for the PCM1760/DF1760 (20-bit stereo analog-to-digital conversion system) primarily intended for quick evaluation of the PCM1760/DF1760's spectral purity and sound fidelity.

The PCM1760 is provided for evaluation with  $\pm 5V$  analog power supply and the DF1760 is provided for evaluation with +5V digital power supply.

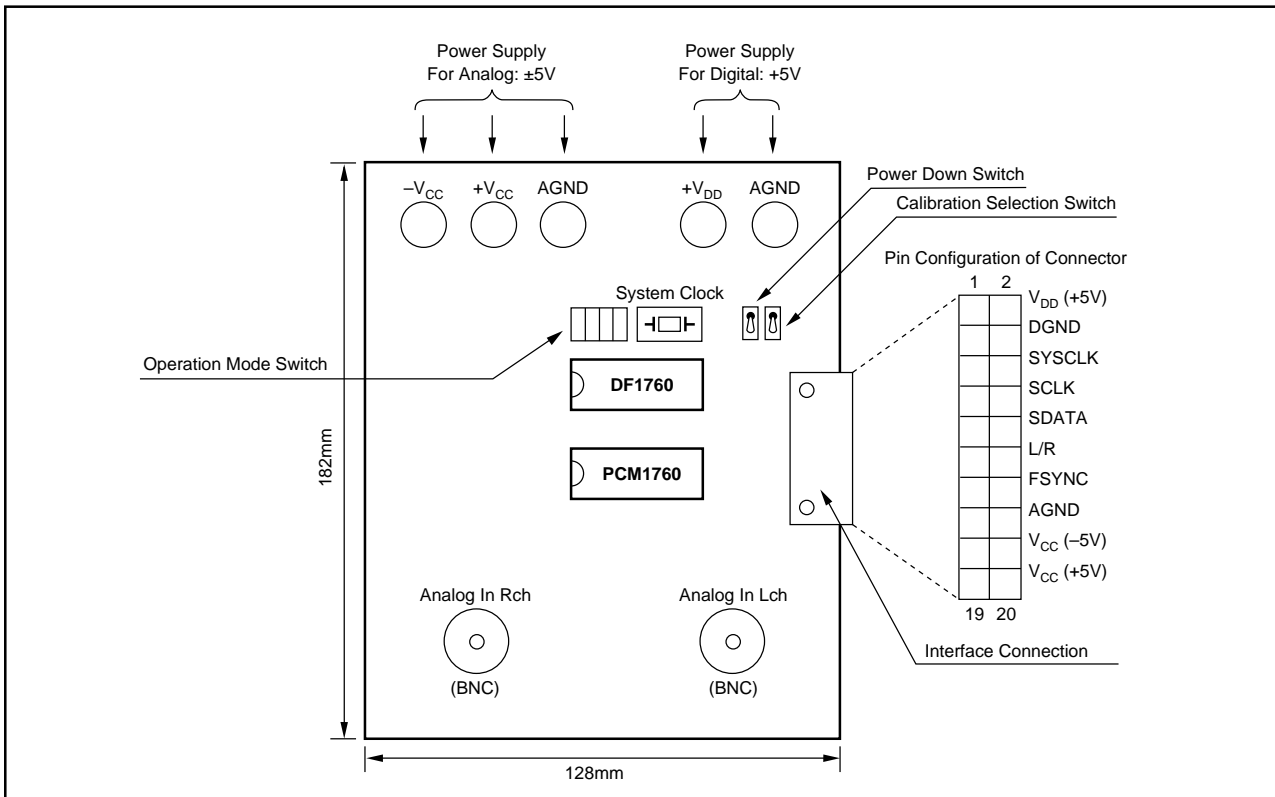
The input to the DEM-PCM1760 is  $\pm 2.5V$  full scale analog signal and output from the DEM-PCM1760 is a serial digital interface signal consisting of SYSCLK, SCLK, SDATA, and L/R.

The output digital data format is selectable and the operation mode is also selectable by function switches on the board.

## BLOCK DIAGRAM



## COMPONENT LOCATION AND FUNCTION



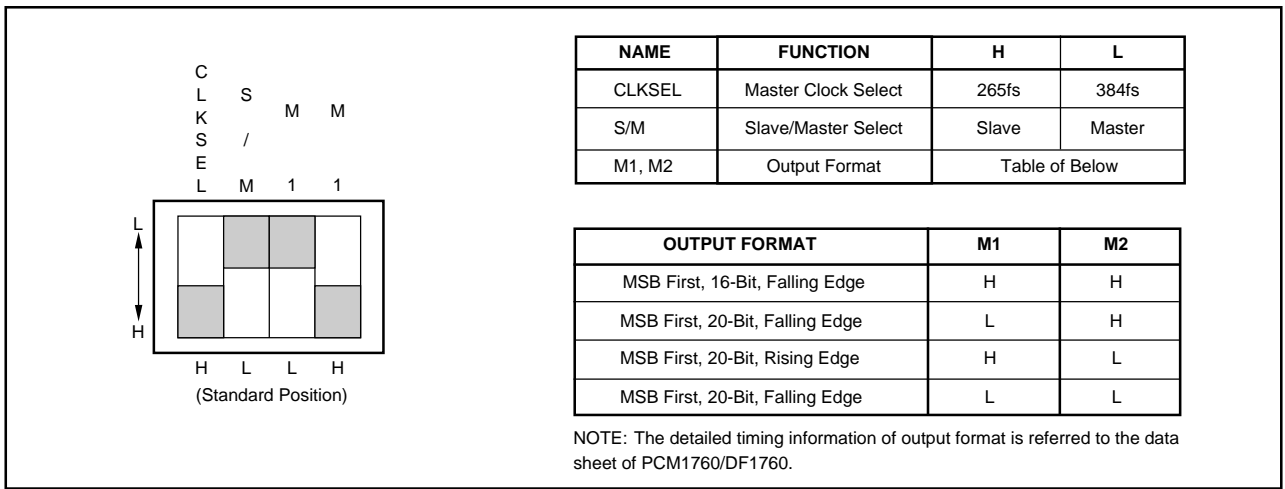
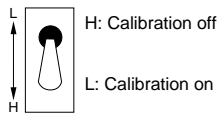
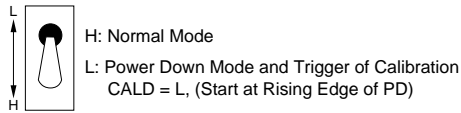


FIGURE 1. Operation Mode Select Switch.

**CALIBRATION SELECT SWITCH (CALD)**



**POWER DOWN SWITCH (PD)**



**COMBINATION WITH DEM-PCM1702**

The DEM-PCM1760 can be directly combined with the DEM-PCM1702 (20-bit stereo D/A conversion system) through the interface connector on the board.

In this case, the power supply should be connected to the DEM-PCM1702 and jumper line should be connected between the connector pin of the DEM-PCM1760 and the connector pin of the DEM-PCM1702.

The power supply for the DEM-PCM1760 is supplied from the DEM-PCM1702 through the jumper line and the DEM-PCM1760 outputs serial data for the DEM-PCM1702.

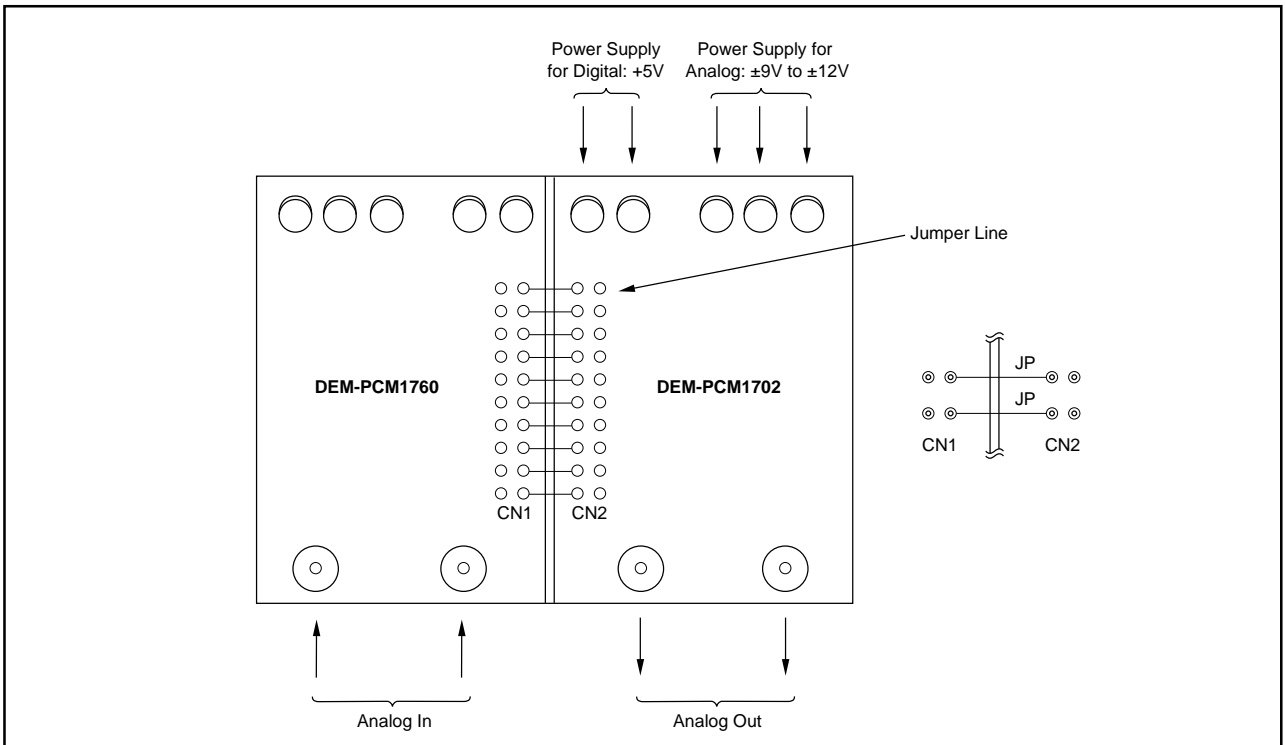


FIGURE 2.

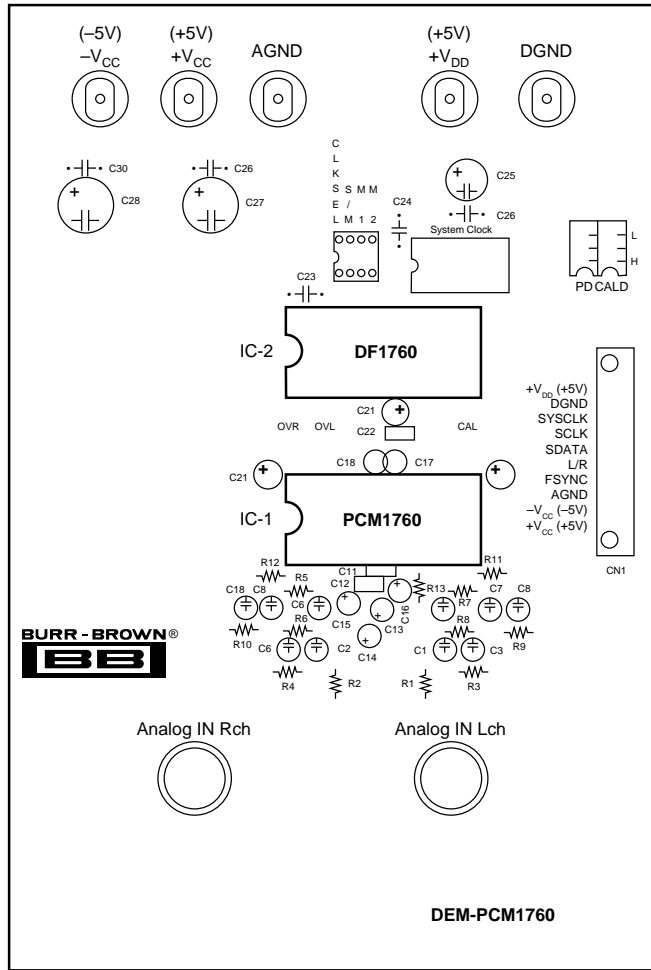
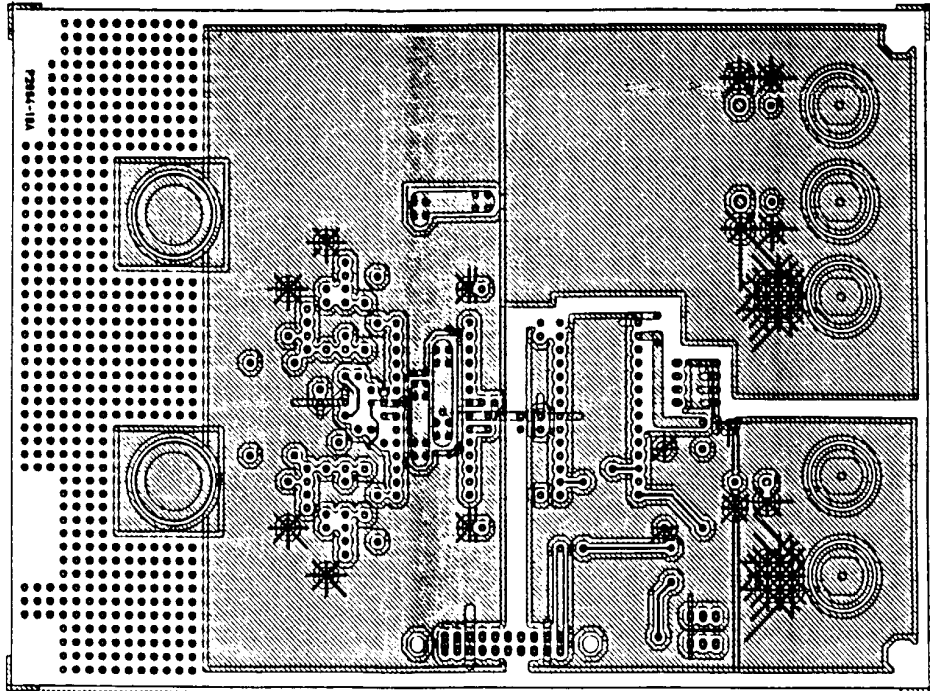
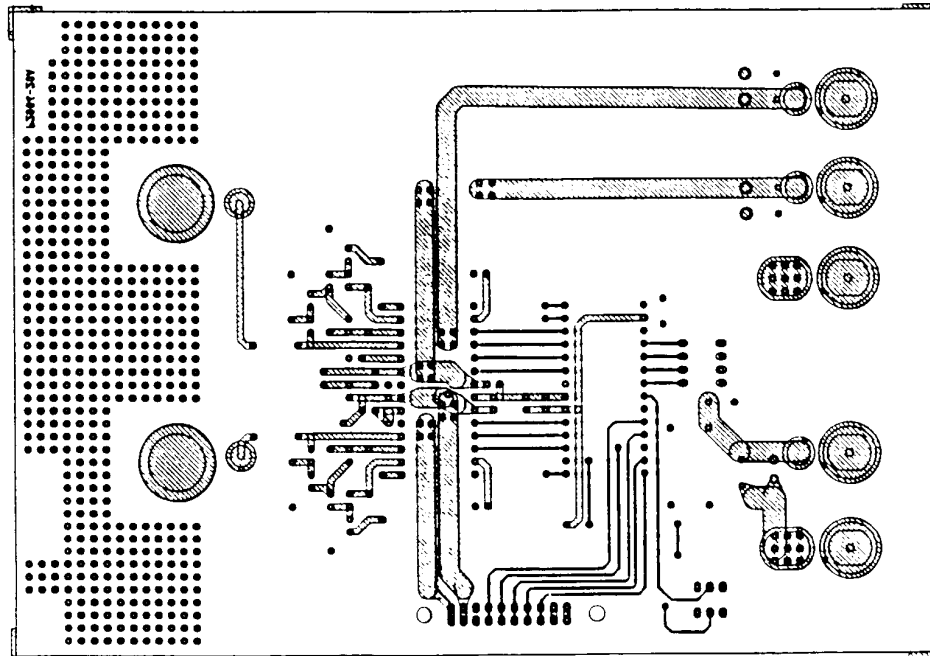


FIGURE 3. DEM-PCM1760 Board Layout—Component Layout.



LAYER 1 (TOP)



LAYER 2 (BOTTOM)

FIGURE 4.

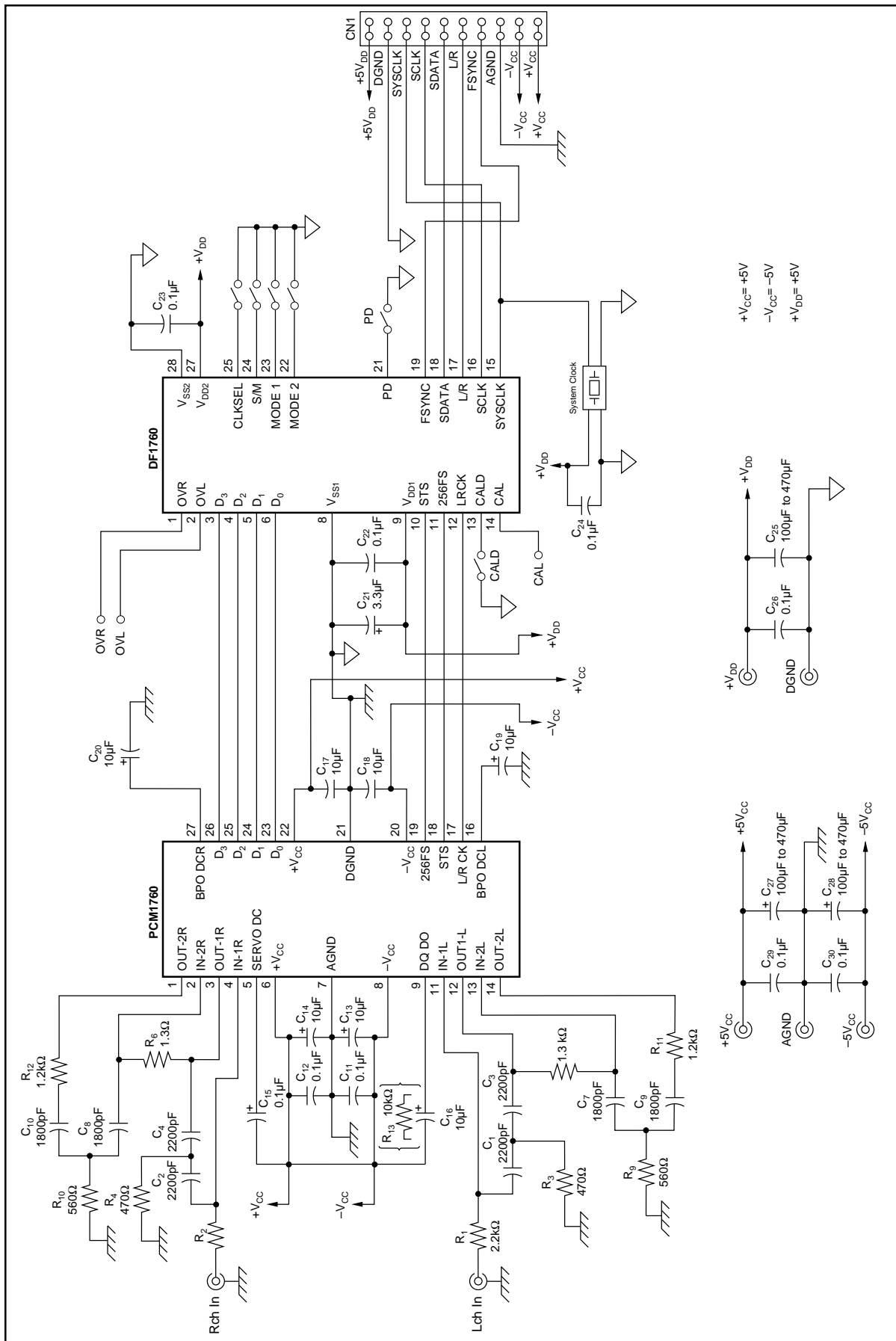


FIGURE 5. Circuit Diagram.