

DM74ALS564A Octal D-Type Edge-Triggered Flip-Flop with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS564A are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the \bar{Q} outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic

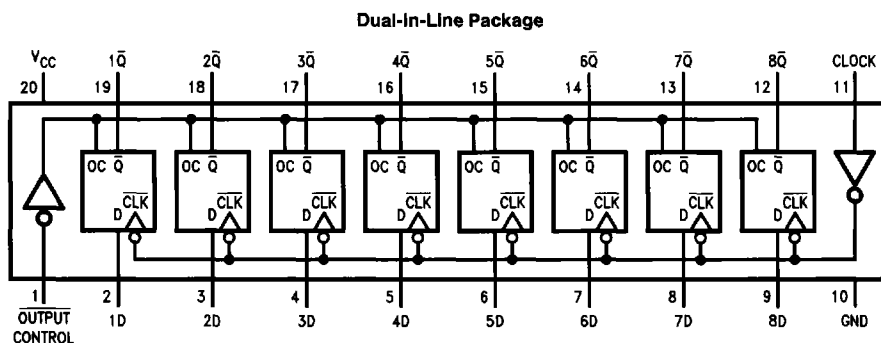
levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram



TL/F/6225-1

Order Number DM74ALS564AWM or DM74ALS564AN
See NS Package Number M20B or N20A

Function Table

| Output Control | Clock | D | Output \bar{Q} |
|----------------|-------|---|------------------|
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | \bar{Q}_0 |
| H | X | X | Z |

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

\bar{Q}_0 = Previous Condition of \bar{Q}

Absolute Maximum Ratings

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Voltage Applied to Disabled Output | 5.5V |
| Operating Free Air Temperature Range | |
| DM74ALS | 0°C to +70°C |
| Storage Temperature Range | –65°C to +150°C |
| Typical θ_{JA} | |
| N Package | 56.0°C/W |
| M Package | 75.0°C/W |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|-------------|--------------------------------|------|---------------|-----|------|-------|
| V_{CC} | Supply Voltage | | 4.5 | 5 | 5.5 | V |
| V_{IH} | High Level Input Voltage | | 2 | | | V |
| V_{IL} | Low Level Input Voltage | | | | 0.8 | V |
| I_{OH} | High Level Output Current | | | | –2.6 | mA |
| I_{OL} | Low Level Output Current | | | | 24 | mA |
| f_{CLOCK} | Clock Frequency | | 0 | | 30 | MHz |
| t_W | Width of Clock Pulse | High | 14 | | | ns |
| | | Low | 14 | | | ns |
| t_{SU} | Data Setup Time | | 15 \uparrow | | | ns |
| t_H | Data Hold Time | | 0 \uparrow | | | ns |
| T_A | Free Air Operating Temperature | | 0 | | 70 | °C |

The (\uparrow) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|-----------|---|---|------------------------------|--------------|------|------|---------|
| V_{IK} | Input Clamp Voltage | $V_{CC} = 4.5V$, $I_I = -18\text{ mA}$ | | | | –1.2 | V |
| V_{OH} | High Level Output Voltage | $V_{CC} = 4.5V$ $V_{IL} = V_{IL\text{ Max}}$ | $I_{OH} = \text{Max}$ | 2.4 | 3.2 | | V |
| | | $V_{CC} = 4.5V\text{ to }5.5V$ | $I_{OH} = -400\text{ }\mu A$ | $V_{CC} - 2$ | | | V |
| V_{OL} | Low Level Output Voltage | $V_{CC} = 4.5V$ $V_{IH} = 2V$ | $I_{OL} = 12\text{ mA}$ | | 0.25 | 0.4 | V |
| | | | $I_{OL} = 24\text{ mA}$ | | 0.35 | 0.5 | V |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = 5.5V$, $V_{IH} = 7V$ | | | | 0.1 | mA |
| I_{IH} | High Level Input Current | $V_{CC} = 5.5V$, $V_{IH} = 2.7V$ | | | | 20 | μA |
| I_{IL} | Low Level Input Current | $V_{CC} = 5.5V$, $V_{IL} = 0.4V$ | | | | –0.2 | mA |
| I_O | Output Drive Current | $V_{CC} = 5.5V$, $V_O = 2.25V$ | | –30 | | –112 | mA |
| I_{OZH} | Off-State Output Current High Level Voltage Applied | $V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 2.7V$ | | | | 20 | μA |
| I_{OZL} | Off-State Output Current Low Level Voltage Applied | $V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 0.4V$ | | | | –20 | μA |
| I_{CC} | Supply Current | $V_{CC} = 5.5V$ Outputs Open | Outputs High | | 10 | 18 | mA |
| | | | Outputs Low | | 15 | 24 | mA |
| | | | Outputs Disabled | | 16 | 30 | mA |

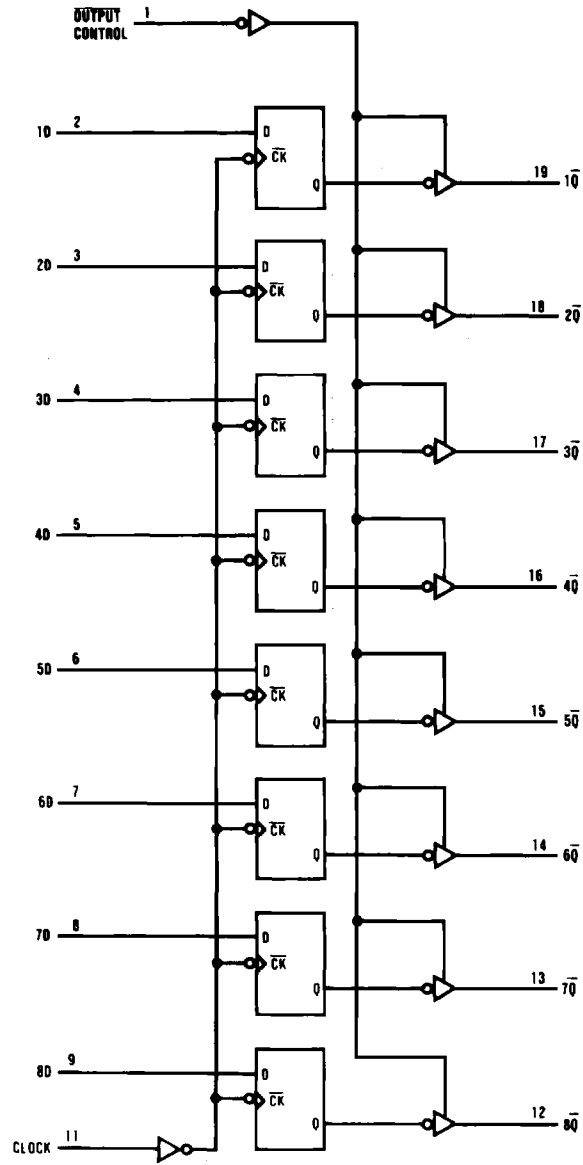
Switching Characteristics

over recommended operating free air temperature range (Note 1)

| Symbol | Parameter | Conditions | From | To | Min | Max | Units |
|-----------|--|---|-------------------|---------------|-----|-----|-------|
| f_{MAX} | Maximum Clock Frequency | $V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\Omega$ $C_L = 50$ pF | | | 30 | | MHz |
| t_{PLH} | Propagation Delay Time Low to High Level Output | | Clock | Any \bar{Q} | 4 | 14 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | | Clock | Any \bar{Q} | 4 | 14 | ns |
| t_{PZH} | Output Enable Time to High Level Output | | Output Control | Any \bar{Q} | 4 | 18 | ns |
| t_{PZL} | Output Enable Time to Low Level Output | | Output Control | Any \bar{Q} | 4 | 18 | ns |
| t_{PHZ} | Output Disable Time from High Level Output | | Output Control | Any \bar{Q} | 2 | 10 | ns |
| t_{PLZ} | Output Disable Time from Low Level Output | | Output Control | Any \bar{Q} | 3 | 15 | ns |

Note 1: See Section 5 for test waveforms and output load.

Logic Diagram



TL/F/6225-2