National Semiconductor

DM74AS286 9-Bit Parity Generator/Checker with Bus-Driver Parity I/O Port

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

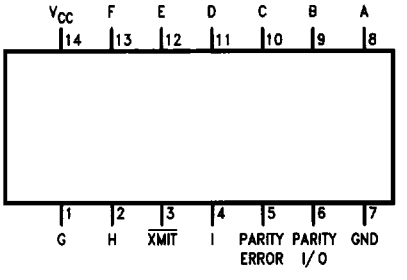
The 'AS286 can be used to upgrade the performance of most systems utilizing the 'AS180, 'AS280 parity generator/checker. Although the 'AS286 is implemented without expander inputs, the corresponding function is provided by the availability of an input pin $\overline{XMIT}$. $\overline{XMIT}$ is a control line which makes parity error output active and parity an input port when "high"; when "low", parity error output is inactive and parity becomes an output port. In addition, parity I/O control circuitry contains a feature to keep the I/O port in the TRI-STATE® during power up or down to prevent bus glitches.

Features

- PNP inputs to reduce bus loading
- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for n-bits
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- A parity I/O portable to drive bus

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74AS286M or DM74AS286N
See NS Package Number M14A or N14A

Function Table

Number of Inputs (A thru I) that are High	Parity I/O		$\overline{XMIT}$	Parity Error	Mode of Operation
	Input	Output			
0, 2, 4, 6, 8	N/A	H	L	H	Parity Generator
1, 3, 5, 7, 9	N/A	L	L	H	
0, 2, 4, 6, 8	H	N/A	H	H	Parity Checker
0, 2, 4, 6, 8	L	N/A	H	L	
1, 3, 5, 7, 9	H	N/A	H	L	Parity Checker
1, 3, 5, 7, 9	L	N/A	H	H	

L = Low Logic Level
H = High Logic Level
N/A = Not Applicable

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	77.0°C/W
M Package	108.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current	Parity I/O			−15	mA
		Parity Error			−2	mA
I_{OL}	Low Level Output Current	Parity I/O			48	mA
		Parity Error			20	mA
T_A	Operating Free-Air Temperature		0		70	°C

Electrical Characteristics

over recommended free-air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V		2.4	3.2		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V (V_I = 5.5V for Parity I/O)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V (Note 1)	Others			20	µA
			Parity I/O			50	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V (Note 1)				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, Transmit Mode $\overline{XMIT}$ = Low				43	mA
		Receive Mode $\overline{XMIT}$ = High				50	mA

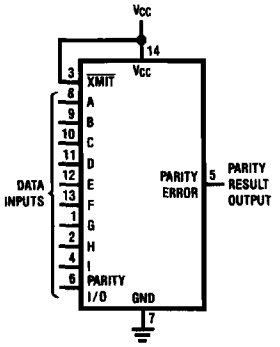
Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current, I_{OZH} and I_{OZL}.

Switching Characteristics over recommended supply and temperature range (Note 1)

Symbol	Parameter	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time from Low to High Level Output	Any Data Input	Parity I/O	3	15	ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Any Data Input	Parity I/O	3	14	ns
t_{PLH}	Propagation Delay Time from Low to High Level Output	Any Data Input	Parity Error	3	16.5	ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Any Data Input	Parity Error	3	16.5	ns
t_{PLH}	Propagation Delay Time from Low to High Level Output	Parity I/O	Parity Error	3	9	ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Parity I/O	Parity Error	3	9	ns
t_{PZL}	Output Enable Time to Low Level	$\overline{XMIT}$	Parity I/O	3	16	ns
t_{PLZ}	Output Disable Time from Low Level	$\overline{XMIT}$	Parity I/O	3	10	ns
t_{PZH}	Output Disable Time from High Level	$\overline{XMIT}$	Parity I/O	3	13	ns
t_{PHZ}	Output Enable Time to High Level	$\overline{XMIT}$	Parity I/O	3	11.5	ns

Note 1: See Section 5 for test waveforms and output load.

Typical Applications



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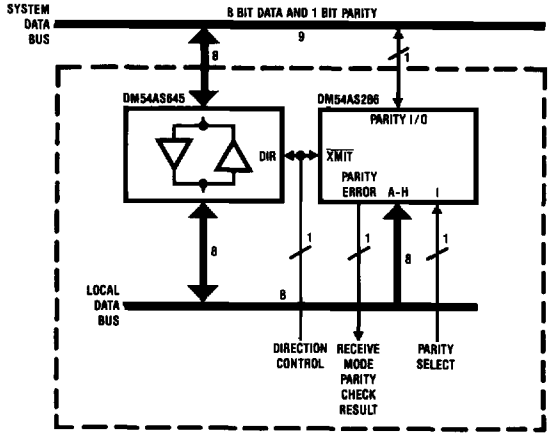
Number of Inputs that are Logic "1"		Parity Result Output
0, 2, 4, 6, 8, 10	Even	L
1, 3, 5, 7, 9	Odd	H

FIGURE 1. Dedicated 10-Bit Parity Sensing Configuration



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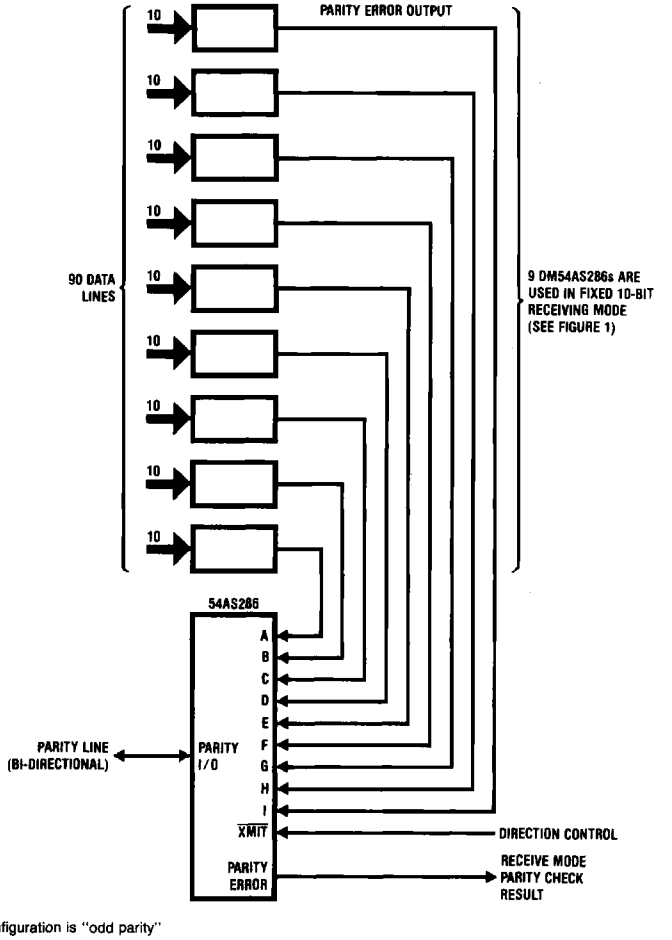
Typical Applications (Continued)

Direction Control (XMIT)	I/O Direction (Parity I/O)	Parity Check Result (Parity Error)	
		Level	Σ Result
H	Input (Receive)	H	True
		L	False
L	Output (Transmit)	H	N/A

L = Low Logic Level H = High Logic Level N/A = Not Applicable

Parity Select (Input I)	
Level	Format
H	Even
L	Odd

FIGURE 2. Bus I/O Parity Implementation



Note: Parity format in this configuration is "odd parity"

FIGURE 3. 90-Bit Parity Generator/Checker Implementation Using Device Expansion Techniques