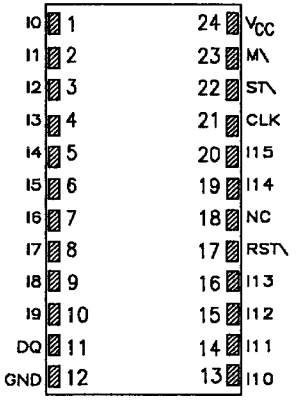
DALLAS SEMICONDUCTOR

DS1223
Electronic Configurator

FEATURES

- 16 remote programmable switches
- 9 bytes of nonvolatile read/write memory
- 16-bit programmable comparator
- 3-pin serial port sets switches and accesses memory
- Greater than 10 years of data retention
- Data and switch settings are automatically protected during power loss
- Full ± 10% operating range
- Applications include DIP switch replacement, remote PC board configuration, mapping, and decoding
- Connects directly to DS1206 Phantom Serial Interface Chip

PIN DESCRIPTION



24-PIN ENCAPSULATED PACKAGE
(720 MIL)

PIN NAMES (\ Denotes Condition Low)

I0-I15	- Switch, Comparator Input/Output
DQ	- Data Input/Data Output
GND	- Ground
RST\	- RESET
CLK	- CLOCK
ST\	- STROBE
V_{CC}	- +5 Volts
NC	- No Connection
M\	- Comparator Match

DESCRIPTION

The DS1223 Electronic Configurator is a CMOS nonvolatile switch, comparator, and read/write memory circuit designed for personalizing and configuring electronic equipment remotely. The Configurator has 16 switches that can be remotely programmed to either logic 1, logic 0, or high impedance. Switch pairs can also be connected to simulate 8 SPST switches. In addition, the logic state of 16 inputs can be compared to data contained in nonvolatile memory. There are 16 bytes of nonvolatile read/write memory. Bytes 0, 1, 2, 3, and 4 define switch settings; bytes 5 and 6 relate to the comparator; bytes 7 through 15 are free for any desired use.

A lithium energy source retains information stored in all 16 bytes of memory when power is lost. The Electronic Configurator monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is

switched on, and write protection is enabled to prevent loss of data. While in the data retention mode, the switch/comparator outputs are all in a high impedance mode and all inputs are ignored.

Information is sent to the Configurator via a serial input one byte at a time or in a burst where all 16 bytes are either written or read. Interface to a microprocessor is minimized by on-chip circuitry that permits data transfers with only three signals: CLOCK, RESET\, and Data Input/ Output.

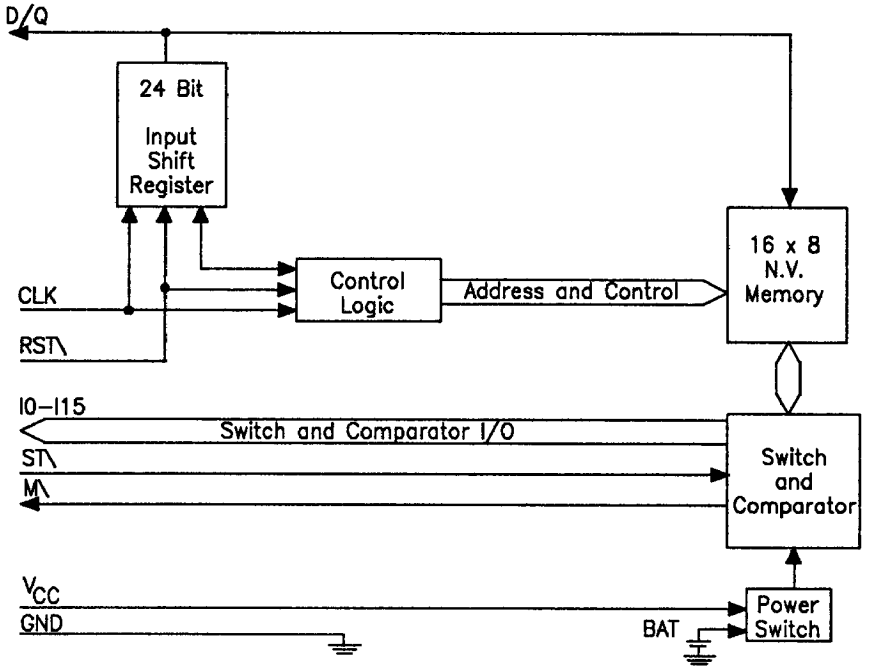
OPERATION

The block diagram (Figure 1) of the Electronic Configurator illustrates the main elements of the device: input shift register, control logic, nonvolatile memory, switch and comparator circuits, and power switch. To initiate communications with the Configurator, RESET\ is taken high and 24 bits are loaded into the input shift register providing both address and command information. Each bit is input serially on the rising edge of the clock. Four address bits specify one of 16 nonvolatile memory locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 clocks which load the input shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals 24 plus 8 for byte mode or 24 plus 128 for burst mode.

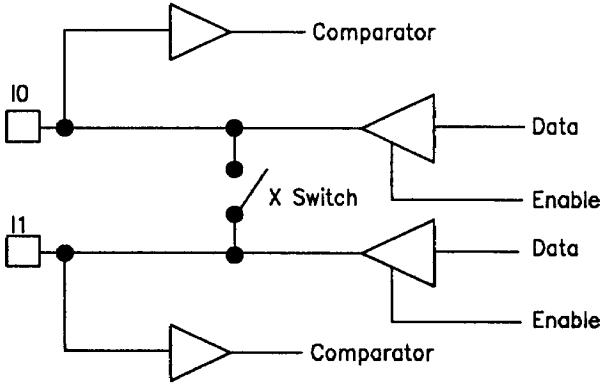
The information stored in the first five bytes of the nonvolatile memory defines the status of input/output pins I0-I15. The switch configuration is illustrated in Figure 2. Data stored in nonvolatile memory bytes 6 and 7 contain 16 bits that are compared to the input/output pins I0-I15. When all inputs match the value stored in bytes 6 and 7, the MATCH\ pin will be latched and driven low when the STROBE\ input transitions from low to high.

The nine remaining bytes serve as user read/ write nonvolatile memory. Figure 3 illustrates the Configurator register address and the definition of each bit.

ELECTRONIC CONFIGURATOR BLOCK DIAGRAM-Figure 1



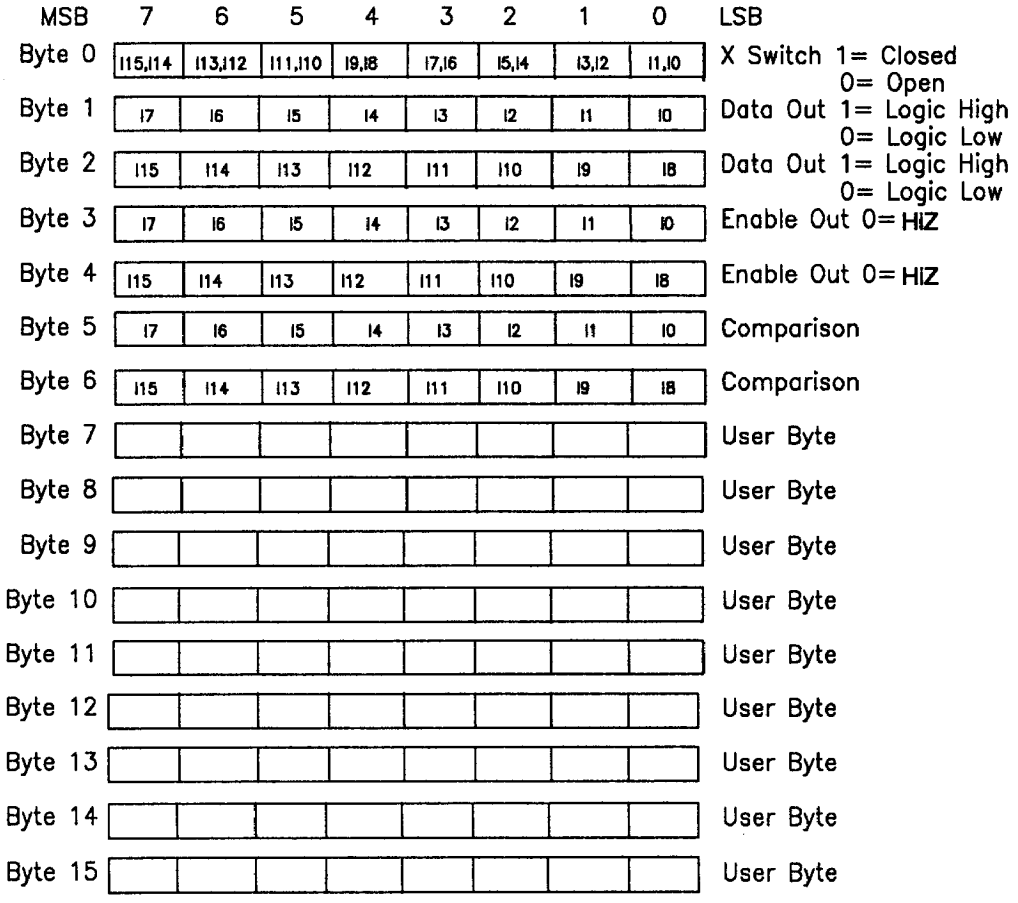
CONFIGURATOR SWITCHES Figure 2



X Switch Resistance ≤ 500Ω

Switch Pairs		
	I0–I1	I8–I9
	I2–I3	I10–I11
	I4–I5	I12–I13
	I6–I7	I14–I15

CONFIGURATOR MEMORY ADDRESSES-Figure 3



ADDRESS/COMMAND

Each data transfer consists of a three-byte address/command input called the address/command. The address/command is shown in Figure 4. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the Configurator are ignored until RESET\ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address A0 in bit 0, A1 in bit 1, A2 in bit 2, and A3 in bit 3. Bits 4 through 7 of the second byte of the address/command must be set at logic 0. If bits 4 through 7 do not equal logic 0, the cycle is aborted and all future inputs to the Configurator are ignored until RESET\ is brought low and then high again to begin a new cycle. The third byte of the address/command must have a logic 0 in bit 0 through bit 5 and a logic 1 written in bit 6. Bit 7 of byte three of the address/command is used along with bits A0 through A3 in byte 2 to define the burst mode. When A0 through A3 of byte two equals logic 0 and bit 7 of byte three equals logic 1, the Configurator will enter the burst mode after the 24-bit address/command sequence is complete.

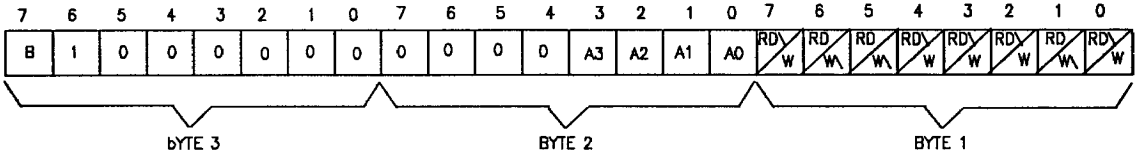
BURST MODE

Burst mode is specified for the Electronic Configurator when all address bits (A0-A3) of the address/command are set to logic 0 and bit 7 of byte three is set to logic 1. The burst mode causes 16 consecutive bytes to be read or written. Burst mode terminates when the RESET\ input is driven low.

RESET AND CLOCK CONTROL

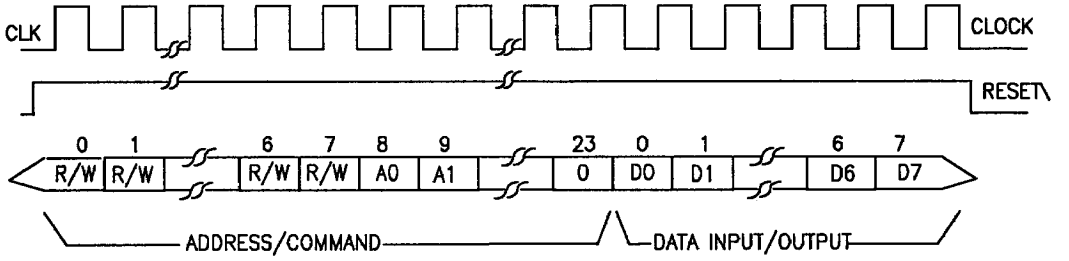
All data transfers are initiated by driving the RESET\ input high. The input also provides a method of terminating either single-byte or multiple-byte transfers. A clock cycle is a sequence of a falling edge followed by a rising edge. For data input, the data must be valid during the rising edge of clock cycles. Address/command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminate and the D/Q pin goes to a high impedance state if the RESET\ input is low. The RST\ input is used only to control communications with the Configurator and has no effect on the nonvolatile memory data. Data transfer is illustrated in Figure 5.

CONFIGURATOR-ADDRESS/COMMAND WORD Figure 4

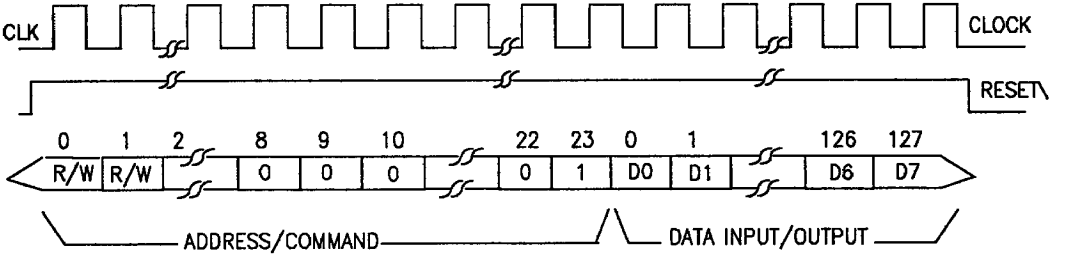


B-Burst
RD-Read
W-Write
A0-A3-Address

DATA TRANSFER Figure 5
SINGLE BYTE TRANSFER



BURST MODE TRANSFER



NOTES:
1. Data input sampled on rising edge of clock.
2. Data output changes on falling edge of clock.

DATA INPUT
Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set. (For data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1.)

DATA OUTPUT
Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles. (For data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0.)

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			1	uA	5
Output Leakage	I_{LO}			1	uA	5
Output Current @2.4V	I_{OH}	-1			mA	11
Output Current @ .4V	I_{OL}			+4	mA	11
Output Current @2.4V	I_{OH}	-400			uA	12
Output Current @ .4V	I_{OL}			1.6	mA	12
X Switch Impedance	X			500	ohms	7
Active Current	I_{CC1}			10	mA	8
Standby Current	I_{CC2}			2	mA	8, 2

CAPACITANCE (t_A = 25°C)

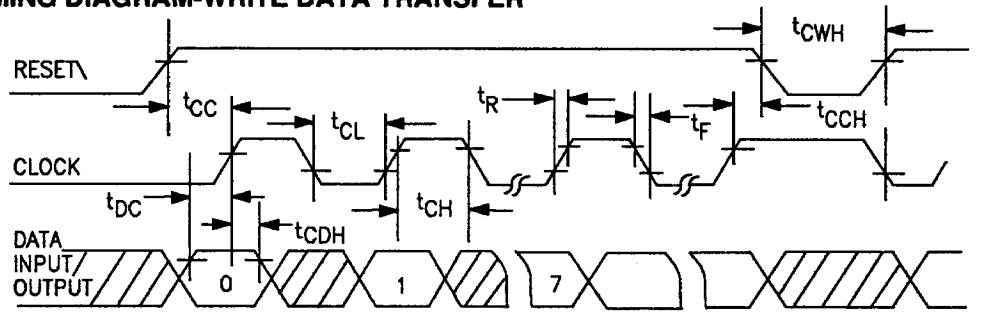
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5			pF	
Output Capacitance	C_{OUT}	7			pF	

AC ELECTRICAL CHARACTERISTICS

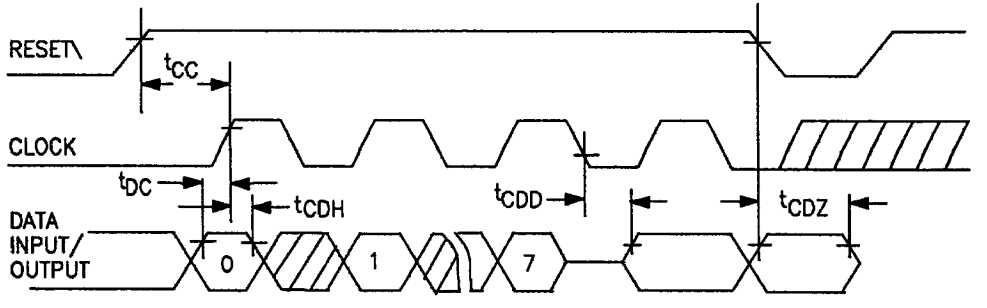
(0°C to 70°C, V_{CC} = 5v ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	3
Data to CLK Hold	t_{CDH}	50			ns	3
CLK to Data Delay	t_{CDD}			200	ns	3,4,6
CLK Low Time	t_{CL}	250			ns	3
CLK High Time	t_{CH}	250			ns	3
CLK Frequency	f_{CLK}	DC		2.0	MHz	3
CLK Rise & Fall	t_R,t_F			10	ns	3
RST\ to CLK Setup	t_{CC}	1			us	3,9
CLK to RST\ Hold	t_{CCH}	50			ns	3
RST\ Inactive Time	t_{CWH}	1			us	3
RST\ to //O High Z	t_{CDZ}			75	ns	3
Strobe to MATCH\ Valid	t_{SM}			35	ns	3
Input Setup	t_{SU}	40			ns	3,4
Input Hold	t_{HD}	10			ns	3,4

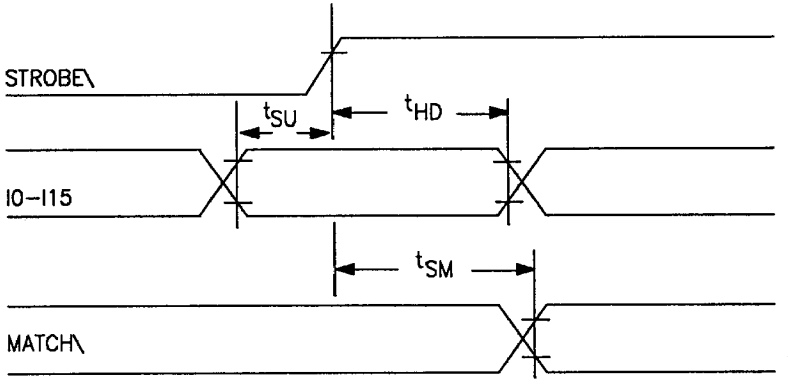
TIMING DIAGRAM-WRITE DATA TRANSFER[10]



TIMING DIAGRAM-WRITE DATA TRANSFER[10]



TIMING DIAGRAM-COMPARATOR[10]



NOTES:

1. All voltages are referenced to GND.
2. RESET\ = V_{IH}.
3. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
4. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
5. V_{CC} = +5 volts with outputs open.
6. Load capacitance = 100 pF.
7. X Switch Impedance is the terminal resistance of switch pairs when the X switch is closed; see Figure 2.
8. Measured with outputs open.
9. Measured at V_{IN} of RST\ = 3.8V.
10. A period of 100 ns must elapse after data transfer before switches and comparator outputs are valid.
11. Applies to DQ and MATCH\.
12. Applies to switches.