National Semiconductor

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DS32EL0124, DS32ELX0124

125 MHz — 312.5 MHz FPGA-Link Deserializer with DDR LVDS Parallel Interface

General Description

The DS32EL0124/DS32ELX0124 integrates clock and data recovery modules for high-speed serial communication over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. This easy-to-use chipset integrates advanced signal and clock conditioning functions, with an FPGA friendly interface.

The DS32EL0124/DS32ELX0124 deserializes up to 3.125 Gbps of high speed serial data to 5 LVDS outputs without the need for an external reference clock. With DC-balance decoding enabled, the application payload of 2.5 Gbps is deserialized to 4 LVDS outputs.

The DS32EL0124/DS32ELX01214 deserializers feature a remote sense capability to automatically signal link status conditions to its companion DS32EL0421/ELX0421 serializers without requiring an additional feedback path.

The parallel LVDS interface of these devices reduce FPGA I/O pins, board trace count and alleviates EMI issues, when compared to traditional single-ended wide bus interfaces.

The DS32EL0124/ELX0124 is programmable through a SMBus interface as well as through control pins.

Applications

- Imaging: Industrial, Medical Security, Printers
- Displays: LED walls, Commercial
- Video Transport
- Communication Systems
- Test and Measurement
- Industrial Bus

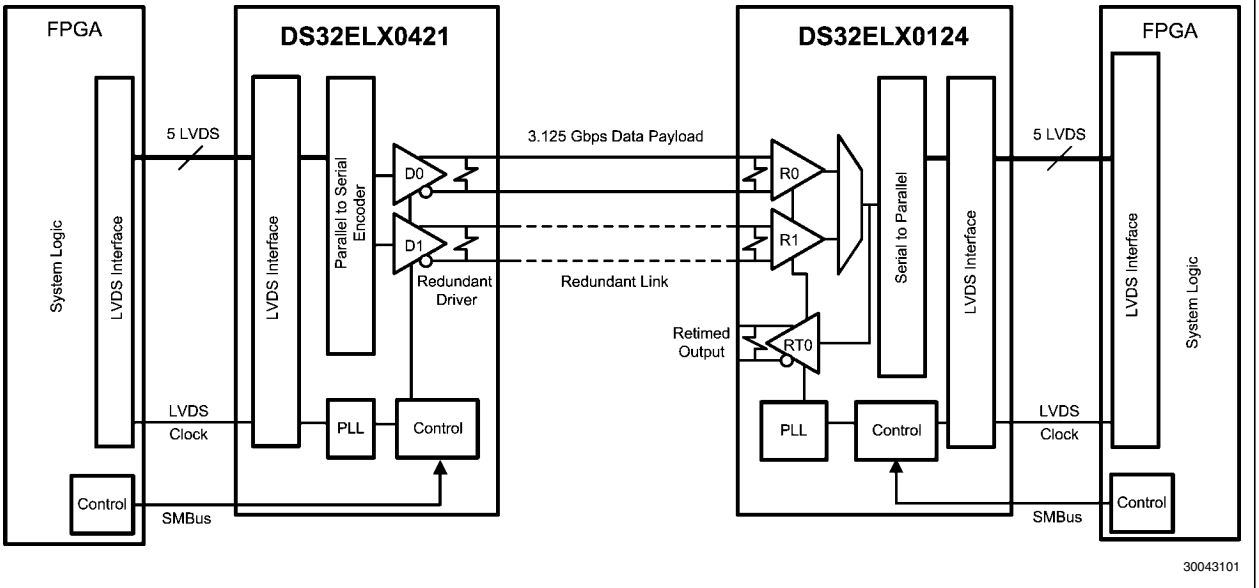
Features

- 5-bit DDR LVDS parallel data interface
- Programmable Receive Equalization
- Selectable DC-balance decoder
- Selectable De-scrambler
- Remote Sense for automatic detection and negotiation of link status
- No external receiver reference clock required
- LVDS parallel interface
- Programmable LVDS output clock delay
- Supports output data-valid signaling
- Supports keep-alive clock output
- On chip LC VCOs
- Redundant serial input (ELX device only)
- Retimed serial output (ELX device only)
- Configurable PLL loop bandwidth
- Configurable via SMBus
- Loss of lock and error reporting
- 48-pin LLP package with exposed DAP

Key Specifications

- 1.25 to 3.125 Gbps serial data rate
- 125 to 312.5 MHz DDR parallel clock
- -40° to +85°C temperature range
- > 8 kV ESD (HBM) protection
- 0.5 UI Minimum Input Jitter Tolerance (1.25 Gbps)

Typical Application



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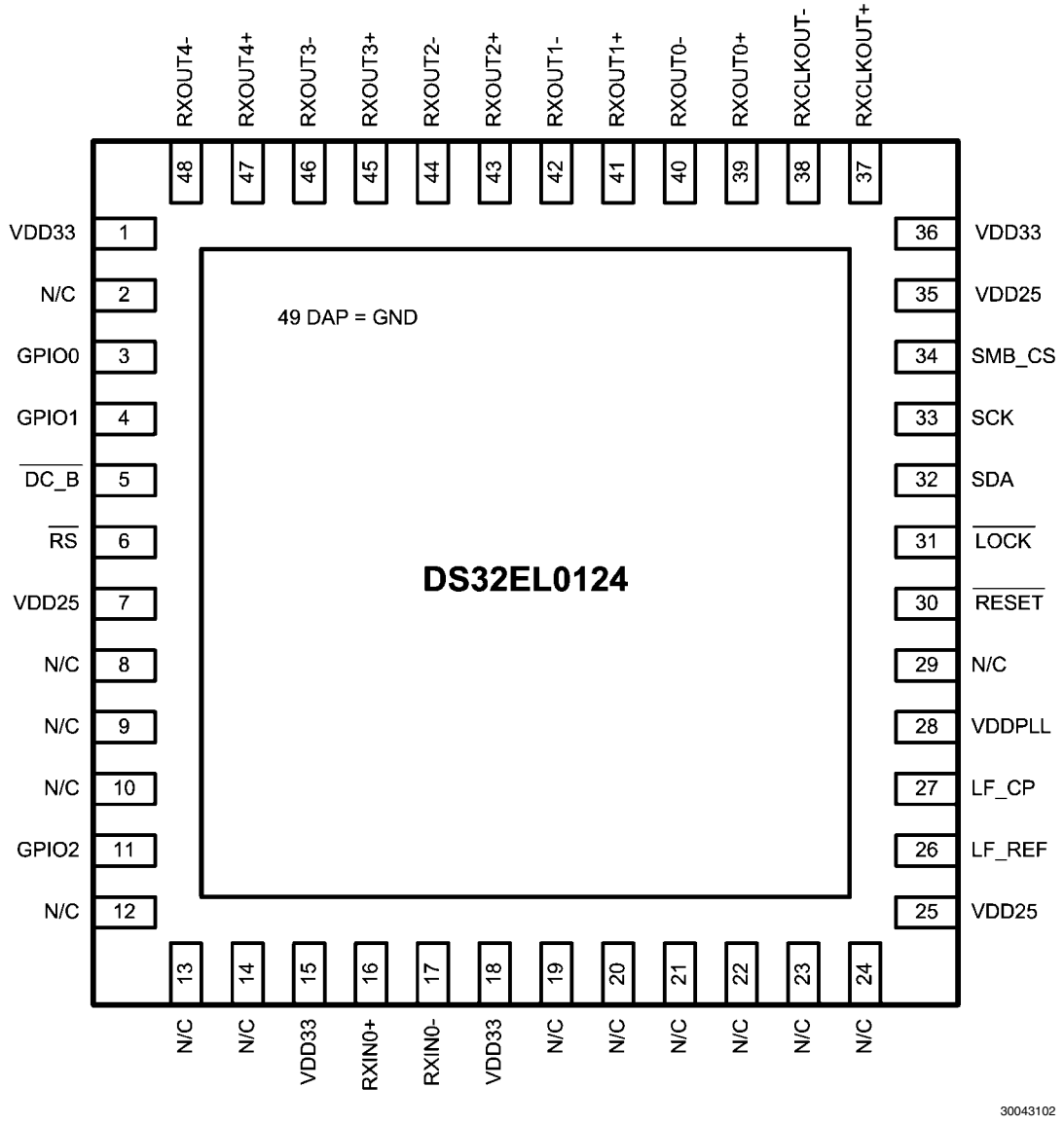
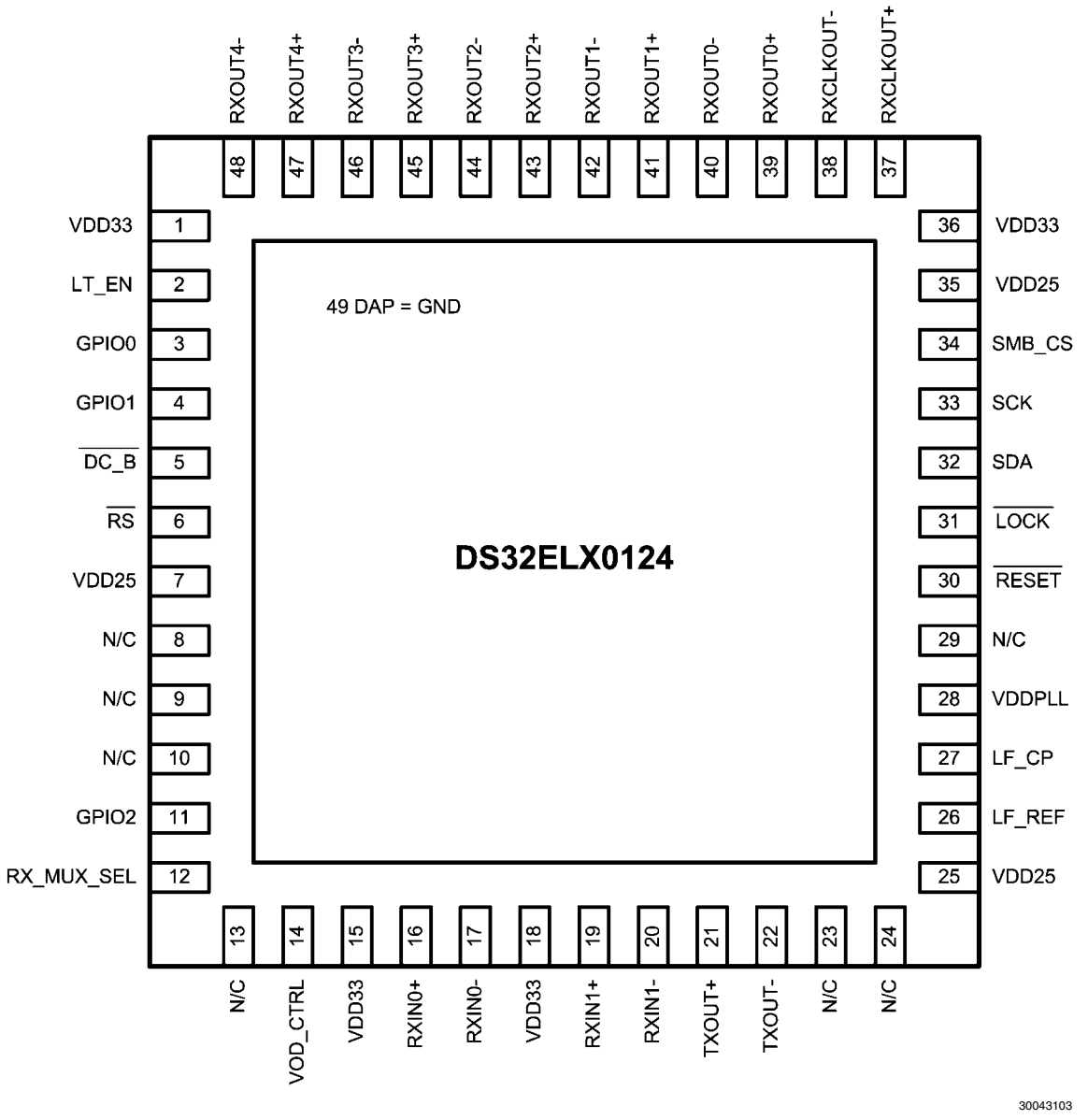
Connection Diagrams



Ordering Information

NSID	Description	Package	T&R Quantity
DS32EL0124SQ	DES	48 - LLP, SQA48A	1000
DS32EL0124SQE		48 - LLP, SQA48A	250
DS32EL0124SQX		48 - LLP, SQA48A	2500
DS32ELX0124SQ	DES with Redundant Input and Retimed Output	48 - LLP, SQA48A	1000
DS32ELX0124SQE		48 - LLP, SQA48A	250
DS32ELX0124SQX		48 - LLP, SQA48A	2500



Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
VDD33	1, 15, 18, 36	I, VDD	3.3V supply
VDD25	7, 25, 35	I, VDD	2.5V supply
VDD_PLL	28	I, VDD	3.3V supply
LF_CP	27	Analog	Loop filter capacitor connection
LF_REF	26	Analog	Loop filter ground reference
Exposed Pad	49	GND	Exposed Pad must be connected to GND by 9 vias.

Pin Name	Pin Number	I/O, Type	Description
CML I/O			
RxIN0+ RxIN0-	16 17	I, CML	Non-inverting and inverting high speed CML differential inputs of the deserializer. These inputs are internally terminated.
RxIN1+ RxIN1-	19 20	I, CML	**DS32ELX0124 only.** Non-inverting and inverting high speed CML differential inputs of the deserializer. These inputs are internally terminated.
TxOUT+ TxOUT-	21 22	O, CML	**DS32ELX0124 only.** Retimed serialized high speed output. Non-inverting and inverting speed CML differential outputs of the deserializer. These outputs are internally terminated.
LVDS Parallel Data Bus			
RxCLKOUT+ RxCLKOUT-	37 38	O, LVDS	Deserializer output clock. RxCLKOUT+/- are the non-inverting and inverting LVDS recovered clock output pins.
RxOUT[0:4]+/-	39, 40, 41, 42, 43, 44, 45, 46, 47, 48	O, LVDS	Deserializer output data. RxOUT[0:4]+/- are the non-inverting and inverting LVDS deserialized output data pins.
Control Pins			
LT_EN	2	I, LVCMOS	**DS32ELX0124 only.** When held high, retimed serialized high speed output is enabled.
RX_MUX_SEL	12	I, LVCMOS	**DS32ELX0124 only.** RX_MUX_SEL selects the input of the deserializer. 0 = RxIN0+/- selected 1 = RxIN1+/- selected
VOD_CTRL	14	I, LVCMOS	**DS32ELX0124 only.** VOD control. The deserializer loop through output amplitude can be adjusted by connecting this pin to a pull-down resistor. The value of the pull-down resistor determines the VOD. See *LOOP THROUGH DRIVER LAUNCH AMPLITUDE* for more details.
$\overline{\text{DC\_B}}$ $\overline{\text{RS}}$	5 6	I, LVCMOS	DC-balance and Remote Sense pins. See Application section for device behavior.
$\overline{\text{RESET}}$	30	I, LVCMOS	Reset pin. When held low, reset the device. 0 = Device Reset 1 = Normal operation
$\overline{\text{LOCK}}$	31	O, LVCMOS	Lock indication output. pin goes low when the deserializer is locked to the incoming data stream and begins to output data and clock on RxOUT and RxCLKOUT respectively. 0 = Deserializer locked 1 = Deserializer not locked
SMBus			
SCK	I, SMBus	33	SMBus compatible clock.
SDA	I/O, SMBus	32	SMBus compatible data line.
SMB_CS	I, SMBus	34	SMBus chip select. When held high, SMBus management control is enabled.
Other			
GPIO0	3	I/O, LVCMOS	Software configurable IO pins.
GPIO1	4	I/O, LVCMOS	Software configurable IO pins.
GPIO2	11	I/O, LVCMOS	Software configurable IO pins.
NC	2 ,8, 9, 10, 12, 13, 14, 19, 20, 21, 22, 23, 24, 29	Misc.	No Connect, for DS32EL0124
	8, 9, 10, 13, 23, 24, 29	Misc	No Connect, for DS32ELX0124

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD33})	−0.3V to +4V
Supply Voltage (V_{DD25})	-0.3V to +3.0V
LVCMOS Input Voltage	−0.3V to (V_{DD33} + 0.3V)
LVCMOS Output Voltage	-0.3V to (V_{DD33} + 0.3V)
CML Input/Output Voltage	-0.3V to 3.6V
LVDS Output Voltage	-0.3V to +3.6V
Junction Temperature	+125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Package Thermal Resistance	
θ_{JA}	+25.0°C/W
ESD Susceptibility	
HBM	≥8 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD33})	3.135	3.3	3.465	V
Supply Voltage (V_{DD25})	2.375	2.5	2.625	V
Supply Noise Amplitude from 10 Hz to 50 MHz			100	mV_{P-P}
Ambient Temperature (T_A)	−40	+25	+85	°C
SMBus Pull–Up Resistor to V_{SDD} Value		1000		Ω

Power Supply Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD25}	2.5V supply current Loop Through Driver Disabled	1.25 Gbps		50	59	mA
		2.5 Gbps		62	73	
		3.125 Gbps		69	79	
	2.5V supply current Loop Through Driver Enabled	1.25 Gbps		88	99	
		2.5 Gbps		100	112	
		3.125 Gbps		107	120	
I_{DD33}	3.3V supply current Loop Through Driver Disabled	1.25 Gbps		105	121	mA
		2.5 Gbps		105	121	
		3.125 Gbps		105	121	
	3.3V supply current Loop Through Driver Enabled	1.25 Gbps		111	127	
		2.5 Gbps		111	127	
		3.125 Gbps		111	127	
P_D	Power Consumption Loop Through Driver Disabled	1.25 Gbps		475	560	mW
		2.5 Gbps		500	600	
		3.125 Gbps		520	620	
	Power Consumption Loop Through Driver Enabled	1.25 Gbps		590	690	
		2.5 Gbps		620	730	
		3.125 Gbps		640	750	

LVCMOS Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. Applies to LT_EN, GPIO0, GPIO1, GPIO2, RX_MUX_SEL, $\overline{DC\_B}$, $\overline{RESET}$, $\overline{RS}$, $\overline{LOCK}$. (*Note 2*, *Note 4*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA	2.7	3.2		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA			0.3V	V
V_{CL}	Input Clamp Voltage	I_{CL} = –18 mA		-0.9	–1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V, or V_{DD33}	-40		40	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (*Note 6*)		-45		mA

SMBus Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SIL}	Data, Clock Input Low Voltage				0.8	V
V_{SIH}	Data, Clock Input High Voltage		2.1		V_{SDD}	V
V_{SDD}	Nominal Bus Voltage		2.375		3.465	V
I_{SLEAKB}	Input Leakage Per Bus Segment	SCK and SDA pins		±200		µA
I_{SLEAKP}	Input Leakage Per Pin			±10		µA
C_{SI}	Capacitance for SDA and SCK			10		pF

SMBus Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SMB}	Bus Operating Frequency		10		100	kHz
t_{BUF}	Bus free time between top and start condition		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated		4.0			µs
$t_{SU:STA}$	Repeated Start Condition Setup Time	(*Note 3*)	4.7			µs
$t_{HD:DAT}$	Data Hold Time		300			ns
$t_{SU:DAT}$	Data Setup Time	(*Note 3*)	250			ns
t_{LOW}	Clock Low Time		4.7			µs
t_{HIGH}	Clock High Time		4.0		50	µs
$t_{SU:CS}$	SMB_CS Setup Time	(*Note 3*)	30			ns
$t_{HS:CS}$	SMB_CS Hold Time	(*Note 3*)	100			ns
t_{POR}	Time in which the device must be operational after power on	(*Note 3*)			500	ms

LVDS Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	R_L = 100Ω	230		310	mV
ΔV_{OD}	Changes in V_{OD} between complimentary output states				35	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary states				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω (*Note 6*)	-50			mA

LVDS Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ROTR}	LVDS low-to-high transition time			300		ps
t_{ROTF}	LVDS high-to-low transition time			300		ps
t_{ROCP}	LVDS output clock period			2T		ns
t_{RODC}	RxCLKOUT Duty Cycle		45	50	55	%
t_{RBIT}	LVDS output bit width			T		ns
t_{ROSC}	RxOUT Setup to RxCLKOUT OUT		650	800		ps
t_{ROHC}	RxOUT Hold to RxCLKOUT OUT		650	800		ps
t_{RODJ}	LVDS Output Deterministic Jitter	RxCLKOUT (*Note 3*)		18		ps
		RxOUT0–4 (*Note 3*)		43		
t_{RORJ}	LVDS Output Random Jitter	RxCLKOUT (*Note 3*)		2.5		ps
		RxOUT0–4 (*Note 3*)		2.5		
t_{ROTJ}	Peak-to-Peak LVDS Output Jitter	RxCLKOUT (*Note 3*)		51		ps
		RxOUT0–4 (*Note 3*)		70		
t_{RLA}	Deserializer Lock Time	(*Note 3*) 1.25 Gbps		22		ms
		2.5 Gbps		90		
		3.125 Gbps		115		
t_{LVSK}	LVDS Output Skew	LVDS Differential Output Skew between + and - pins		20		ps

CML Input Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TOL_{JIT}	Serial Input Jitter Tolerance	RJ = 0.18 UI DJ = 0.37 UI SJ increased until failure 1.25 Gbps f < 10 kHz f > 1 MHz		 30 0.5		UI
		2.5 Gbps f < 10 kHz f > 1 MHz		 50 0.3		
		3.125 Gbps f < 10 kHz f > 1 MHz		 70 0.3		

CML Input Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential input voltage	(*Note 3*)	230		2200	mV
V_{IN}	Single ended input voltage	(*Note 3*)	115		1100	mV
I_{IN}	Input Current		-300		50	µA
R_{IT}	Input Termination		84	100	116	Ω

CML Retimed Loop Through Output Electrical Specifications, DS32ELX0124 Only

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LTOD}	Output differential voltage	VOD_CTRL resistor = 9.09 kΩ (*Note 3*)	1.15		1.45	V
R_{LTOT}	Output termination	50Ω	40	50	60	Ω
		75Ω	60	75	90	
ΔR_{LTOT}	Mismatch in output termination resistors			5		%

CML Retimed Loop Through Output Timing Specifications, DS32ELX0124 Only

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 5*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{JIT}	Additive Output Jitter	(*Note 3*)		24	35	ps
t_{OS}	Output Overshoot	(*Note 3*)		1.5	8	%
t_{LTR}	Retimed output driver differential low to high transition time	(*Note 3*)		74	105	ps
t_{LTF}	Retimed output driver differential high to low transition time	(*Note 3*)		74	105	ps
t_{LTRFMM}	Mismatch in Rise/Fall Time	(*Note 3*)		5	15	%
t_{LTDE}	Retimed driver de-emphasis width			1		UI

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical and Timing Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Parameter is guaranteed by characterization and is not tested at production.

Note 4: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 5: Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 6: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Timing Diagrams

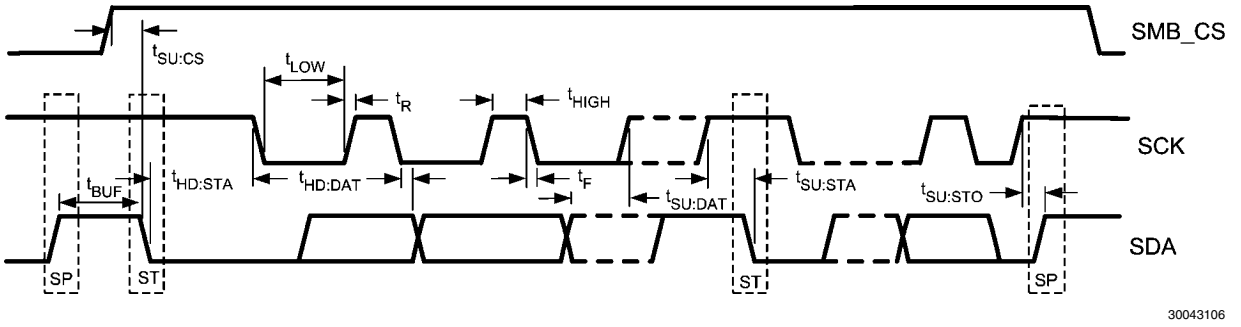


FIGURE 1. SMBus Timing Parameters

FIGURE 2. LVDS Output Transition Time

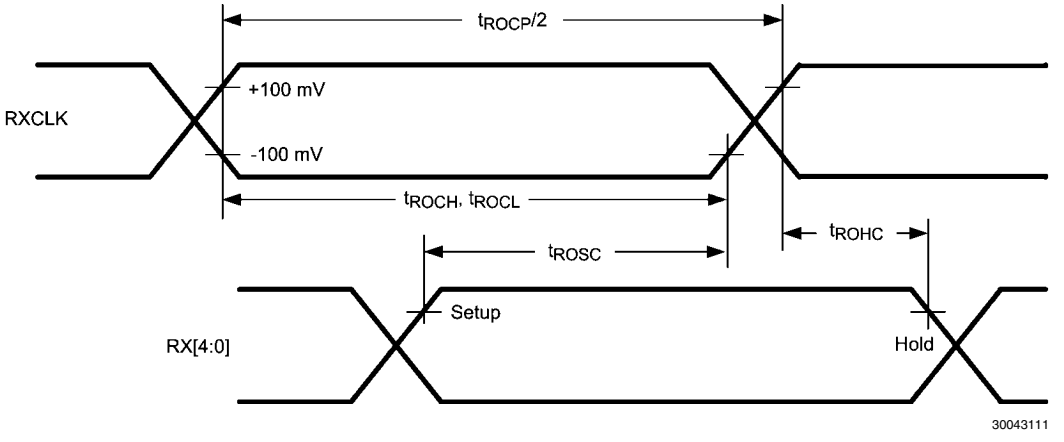


FIGURE 3. Deserializer (LVDS Interface) Setup/Hold and High/Low Times

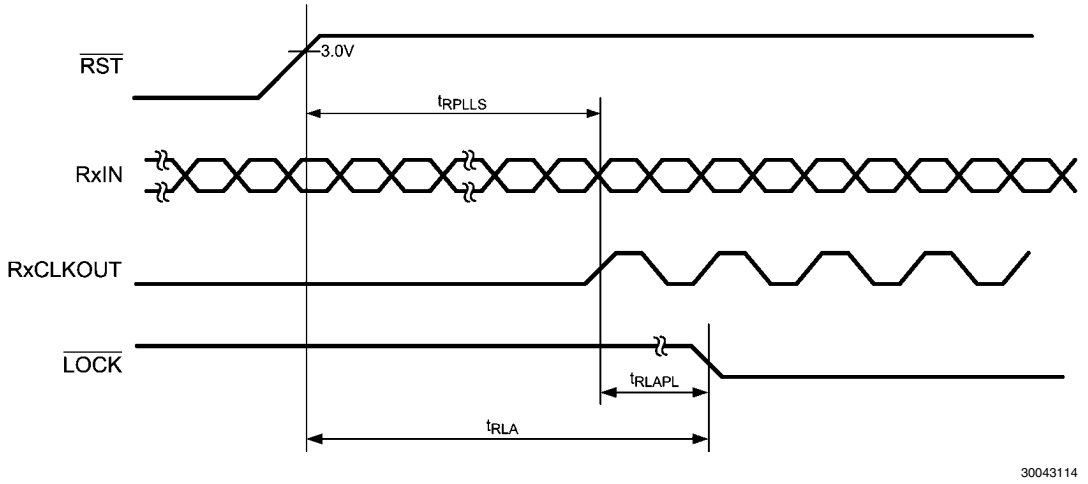


FIGURE 4. Reset to Lock Time

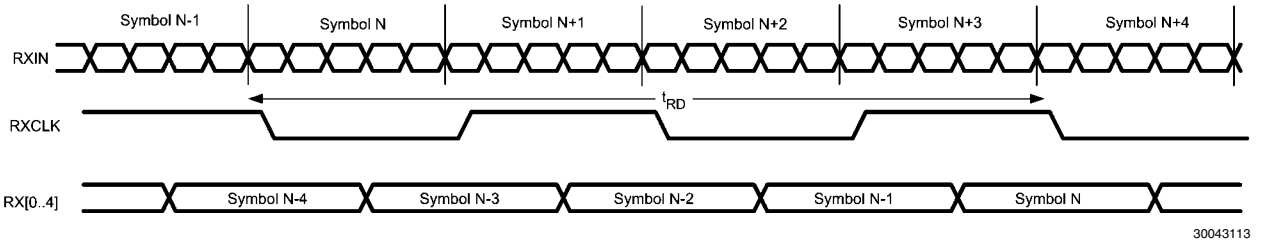


FIGURE 5. Deserializer Propagation Delay

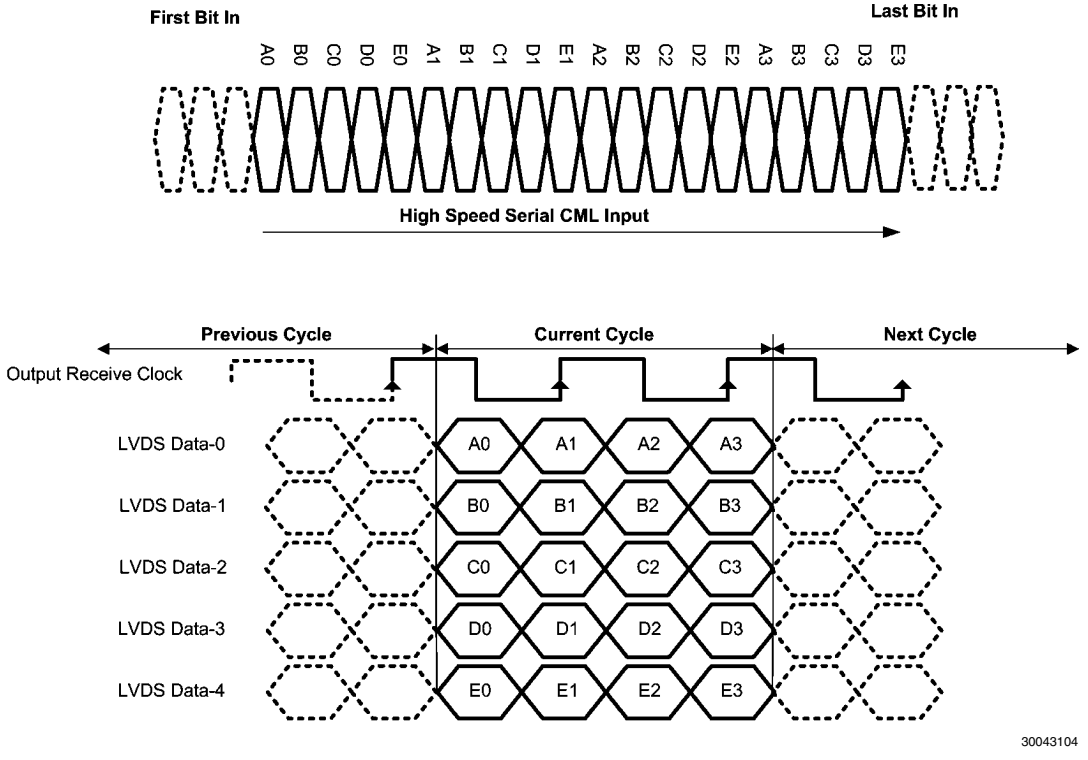


FIGURE 6. CML to LVDS Bit Map

Functional Description

POWER SUPPLIES

The DS32EL0124 and DS32ELX0124 have several power supply pins, at 2.5V as well as 3.3V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of parallel 4.7µF and 0.1µF capacitors as a minimum, with a 0.1µF capacitor on each power pin. A 22 µF capacitor is required on the VDDPLL pin which is connected to the 3.3V rail.

These devices have a large contact in the center on the bottom of the package. This contact must be connected to the system GND as it is the major ground connection for the device.

POWER UP

It is recommended, although not necessary, to bring up the 3.3V power supply before the 2.5V supply. If the 2.5V supply is powered up first, an initial current draw of approximately 600mA from the 2.5V rail may occur before settling to its final value. Regardless of the sequence, both power rails should monotonically ramp up to their final values.

POWER MANAGEMENT

These devices have two methods to reduce power consumption. To enter the first power save mode, the on board host FPGA or controlling device can cease to output the DDR transmit clock. To further reduce power, a write to the power down register will put the device in its lowest power mode.

RESET

There are three ways to reset these devices. A reset occurs automatically during power-up. The device can also be reset by pulling the $\overline{\text{RESET}}$ pin low, with normal operation resuming when the pin is driven high again. The device can also be reset by writing to the reset register. This reset will put all of the register values back to their default values, except it will not affect the address register value if the SMBus default address has been changed.

LVDS OUTPUTS

The DS32EL0124 and DS32ELX0124 has standard LVDS outputs, compatible with ANSI/TIA/EIA-644. It is recommended that the PCB trace between the FPGA and the deserializer output be no more than 40-inches. Longer PCB traces may introduce signal degradation as well as channel skew which could cause serialization errors. The connection between the host and the DS32EL0124 or DS32ELX0124 should be over a controlled impedance transmission line with impedance that matches the termination resistor – usually 100Ω. Setup and hold times are specified in the LVDS Switching Characteristics table, however the clock delay can be adjusted by writing to register 30'h.

LOOP FILTER

The DS32EL0124 and DSELX0124 have an internal clock data recovery module (CDR), which is used to recover the input serial data. The loop filter for this CDR is external, and for optimum results, a 30nF capacitor should be connected between pins 26 and 27. See the Typical Interface Circuit (*Figure 12*).

LOOP THROUGH DRIVER LAUNCH AMPLITUDE

The launch amplitude of the retimed CML loop through driver is controlled by placing a single resistor from the VOD_CTRL pin to ground. Use the following equation to obtain the desired V_{LTOD} by selecting the corresponding resistor value.

$$R = (1400\ mV / V_{LTOD}) \times 9.1\ k\Omega$$

The retimed CML loop through driver launch amplitude can also be adjusted by writing to SMBus register 49'h, bits 3:1. This register is meant to assist system designers during the initial prototype design phase. For final production, it is recommended that the appropriate resistor value be selected for the desired V_{LTOD} and that register 49'h be left to its default value.

REMOTE SENSE

The remote sense feature can be used when a DS32EL0421 or DS32ELX0421 serializer is directly connected to a DS32EL0124 or DS32ELX0124 deserializer. Active components in the signal path between the serializer and the deserializer may interfere with the back channel signaling of the devices.

When remote sense is enabled, the deserializer will cycle through five states to successfully establish a link and align the data. The state diagram for the deserialiezr is shown in *Figure 7*. The deserialzer will remain in the low power IDLE state until it receives an input signal. Once the CDR of the deserializer has locked to the input clock, the device will enter the LINK DETECT state. While in this state, the deserializer will monitor the line to see if the serializer is sending the training pattern. While in this state, the deserializer will periodically send a link detect signal upstream to notify the serializer that it can now send the training pattern. When the deserializer detects that data coming in on the serial line, it will proceed to the CLOCK ACQUISITION state. While in this state the deserializer will monitor the incoming data for set periods of time in an attempt to extract the clock from the data. Once, the deserializer has successfully extracted the clock the device will proceed to the LINK ACQUISITION STATE. In this state the deserializer will perform lane alignment based on the expected training pattern and then enter the NORMAL state. If the deserializer is unable to successfully lock or maintain lock, it will break the link sending the serializer back to the IDLE or LINK DETECT states.

DC-BALANCE DECODER

The DS32EL0124 and DS32ELX0124 have a built-in DC-balance decoder to support AC-coupled applications. When enabled, the output signal RxOUT4+/-, is treated as a data valid bit. If RxOUT4+/- is low, then the data output from RxOUT0 - RxOUT3 has been successfully decoded using the 8b/10b coding scheme. If RxOUT4+/- is high and the outputs RxOUT0 - RxOUT3 are high then an invalid 8b/10b code was received, signifying a bit error. If RxOUT4+/- is high and the outputs RxOUT0 - RxOUT3 are low then an idle character has been received. The default idle character is a K28.5 code. In order to properly receive other K codes, they must first be programmed into the deserializer via the SMBus. The SMBus registers allow for only a single programmable character.

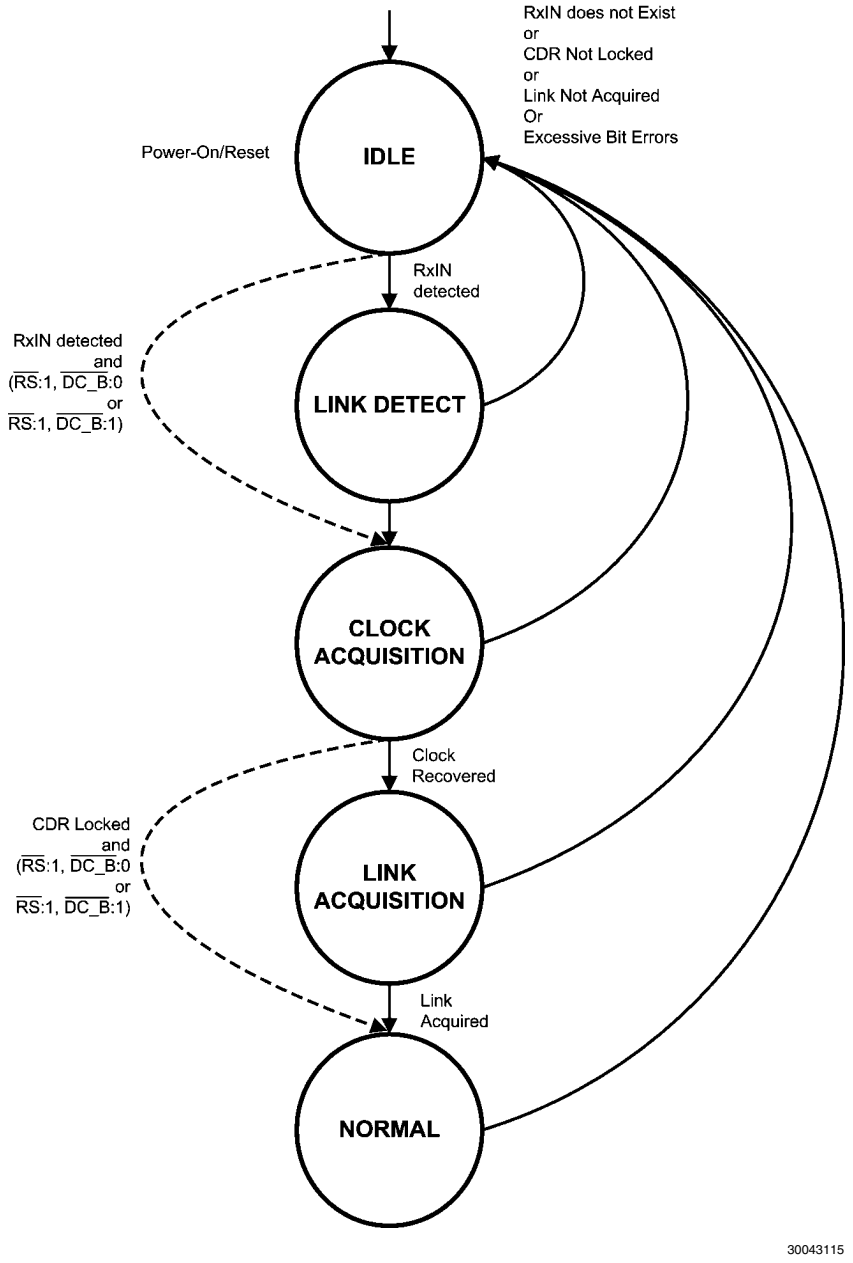


FIGURE 7. Deserializer State Diagram

DESCRAMBLER AND NRZI DECODER

The CDR of the deserializer expects a transition density of 20% for a period of 200 µs. To improve the transition density of the data, the scrambler and NRZI encoder, which are integrated features in the DS32EL0421 and DS32ELX0421, serializers can be enabled. If the descrambler is enabled, the serialized data is descrambled after being recovered by the CDR to according to the polynomial specified in the DS32EL0421 datasheet. Using the scrambler/descrambler helps to lower EMI emissions by spreading the spectrum of the data. Scrambling also creates transitions for a deserializer's CDR to properly lock onto.

The scrambler is enabled or disabled by default depending on how the $\overline{DC\_B}$ and $\overline{RS}$ pins are configured. To override the default scrambler setting two register writes must be performed. First, write to register 22'h and set bit 5 to unlock the descrambler register. Next write to register 21'h and change bit 5 to the desired value. Please note that NRZI decoder has its own control bits in registers 22'h and 21'h.

CML INPUT INTERFACING

The DS32ELX0124 has two inputs to support redundancy and failover applications. Either input can be selected by using the RX_MUX_SEL pin or internal control registers. Whichever input is selected will be routed to the CDR of the deserializer. Only one input may be selected at a time.

The input stage is self-biased and does not need any external bias circuitry. The DS32EL0124 and DS32ELX0124 include integrated input termination resistors. These deserializers also support a wide common mode input from 50mV to Vcc -

50mV and can be DC-coupled where there is no significant Ground potential difference between the interfacing systems. The serial inputs also provides input equalization control in order to compensate for loss from the media. The level of equalization is controlled by the SMBus interface. For the DS32ELX0124, each input can have its own independent equalizer settings.

It is recommended to use RxIN0+/- as the primary input. Due to its close proximity to the loop through driver, RxIN1 has a typical performance less than RxIN0, with regards to cable length performance. When interfacing to RxIN1+/- and transmitting with the loop through driver on TxOUT+/-, it is important to follow good layout practices as described in the layout guidelines section and in the LVDS Owner's Manual. Poor layout techniques can result in excessive cross talk coupled into RxIN1.

CML OUTPUT INTERFACING (DS32ELX0124 ONLY)

The retimed loop through serial outputs of the DS32ELX0124 provide low-skew differential signals. Internal resistors connected from TxOUT+ and TxOUT- to VDD25 terminate the outputs. The output level can be set by adjusting the pull-down resistor to the VOD_CTRL pin. The output terminations can also be programmed to be either 50 or 75 ohms.

The output buffer consists of a current mode logic(CML) driver with user configurable de-emphasis control, which can be used to optimize performance over a wide range of transmission line lengths and attenuation distortions resulting from low cost CAT(-5, -6, -7) cable or FR4 backplane. Output de-emphasis is user programmable through SMBus interface. Users can control the strength of the de-emphasis to optimize for a specific system environment. Please see the Register Map, register 67'h bits 6:5, for details.

DEVICE CONFIGURATION

There are four ways to configure the DS32EL0124 and DS32ELX0124 devices, these combinations are shown in *Table 1*. Refer to *Figure 7* to see how the combinations of the $\overline{RS}$ and $\overline{DC\_B}$ pins change the link startup behavior of the deserializers. When connecting to a serializer other than the DS32EL0421 or DS32ELX0421, Remote Sense should be disabled. The descrambler and NRZI decoder shown in *Table 1* can be enabled or disabled through register programming.

When Remote Sense is enabled, with $\overline{RS}$ pin tied low, the deserializer must be connected directly to a DS32EL0421/DS32ELX0421 serializer without any active components between them. The Remote Sense module features both an upstream and downstream communication method for the serializer to detect a deserializer and vice versa. This feature is used to pass link status information between the 2 devices.

If DC-Balance is enabled, the maximum number of parallel LVDS lanes is four. The fifth lane becomes a Data Valid signal (TXIN4±). If the Data Valid input to the serializer is logic high, then SYNC characters are transmitted. If the deserializer receives a SYNC character, then the LVDS data outputs will all be logic low and the Data Valid outputs will be logic high. If the deserializer detects a DC-Balance code error, the output data pins will be set to logic high with the Data Valid output also set to logic high.

In the case where DC-Balance is enabled and Remote Sense is disabled, with $\overline{RS}$ set to high and $\overline{DC\_B}$ set to low, an external device should toggle the Data Valid input to the serializer periodically to ensure constant lock. With these pin settings the devices can interface with other active component in the high speed signal path, such as fiber modules. Every time a DS32EL0421/DS32ELX0421 serializer establishes a link to a DS32EL0124/DS32ELX0124 deserializer with DC-Balance enabled and Remote Sense disabled, the Data Valid input to the serializer must be held high for 110 LVDS clock periods. This allows the deserializer to extract the clock and perform lane alignment while skipping the LINK ACQUISITION state.

When both Remote Sense and DC-Balance are disabled, $\overline{RS}$ and $\overline{DC\_B}$ pins set to high, the LVDS lane alignment is not maintained. In this configuration, data formatting is handled by an FPGA or external source. In this mode the deserializer locks to incoming random data. To achieve lock during the clock acquisition phase, the incoming data should have a transition density of approximately 20% for a period of 200 µs. Scrambling and NRZI encoding can be implemented to help improve the transition density of the data. This pin setting also allows for the devices to interface with other active components in the high speed signal path.

TABLE 1. Device Configuration Table

Remote Sense Pin ($\overline{RS}$)	DC-Balance Pin($\overline{DC\_B}$)	Configuration
0	0	Remote Sense enabled DC-Balance enabled Data Alignment De-Scrambler and NRZI decoder disabled by default
0	1	Remote Sense enabled DC-Balance disabled Data Alignment De-Scrambler and NRZI decoder enabled by default
1	0	Remote Sense disabled DC-Balance enabled Data Alignment De-Scrambler and NRZI decoder enabled by default
1	1	Remote Sense disabled DC-Balance disabled No Data Alignment De-Scrambler and NRZI decoder disabled by default

SMBus INTERFACE

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the SMB_CS pin HIGH enables the SMBus port, allowing access to the configuration registers. Holding the SMB_CS pin LOW disables the device's SMBus, allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the SMB_CS signal for the deserializer must be driven LOW.

The address byte for all DS32EL0124 and DS32ELX0124 devices is B0'h. Based on the SMBus 2.0 specification, these devices have a 7-bit slave address of 1011000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1011 0000'b or B0'h.

The SCK and SDA pins are 3.3V LVCMOS signaling and include high-Z internal pull up resistors. External low impedance pull up resistors maybe required depending upon SMBus loading and speed. Note, these pins are not 5V tolerant.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SCK is HIGH.

There are three unique states for the SMBus:

START A HIGH to LOW transition on SDA while SCK is HIGH indicates a message START condition.

STOP A LOW to HIGH transition on SDA while SCK is HIGH indicates a message STOP condition.

IDLE If SCK and SDA are both HIGH for a time exceeding t_{BUF} from the last detected STOP condition or if they are HIGH for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus Transactions

The devices support WRITE and READ transactions. See Register Description Table for register address, type (Read/Write, Read Only), default value and function information.

Writing to a Register

The devices support WRITE and READ transactions. See Register Description Table for register address, type (Read/Write, Read Only), default value and function information.

1. The Host (Master) selects the device by driving its SMBus Chip Select (SMB_CS) signal HIGH.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit (“0”).
8. The Host drives a STOP condition.
9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (SMB_CS) signal HIGH.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
8. The Device drives an ACK bit “0”.
9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit “1”indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

SMBus Configurations

Many different configurations of the SMBus are possible and depend upon the specific requirements of the applications. Several possible applications are described.

Configuration 1

The deserializer SMB_CS may be tied High (always enabled) since it is the only device on the SMBus. See Figure 8.

Configuration2

Since the multiple SER devices have the same address, the use of the individual SMB_CS signals is required. To communicate with a specific device, its SMB_CS is driven High to select the device. After the transaction is complete, its SMB_CS is driven Low to disable its SMB interface. Other devices on the bus may now be selected with their respective chip select signals and communicated with. See Figure 9.

Configuration 3

The addressing field is limited to 7-bits by the SMBus protocol. Thus it is possible that multiple devices may share the same 7-bit address. An optional feature in the SMBus 2.0 specification supports an Address Resolution Protocol (ARP). This optional feature is not supported by the DS32EL0124/DS32ELX0124 devices. Solutions for this include: the use of the independent SMB_CS signals, independent SMBus segments, or other means.

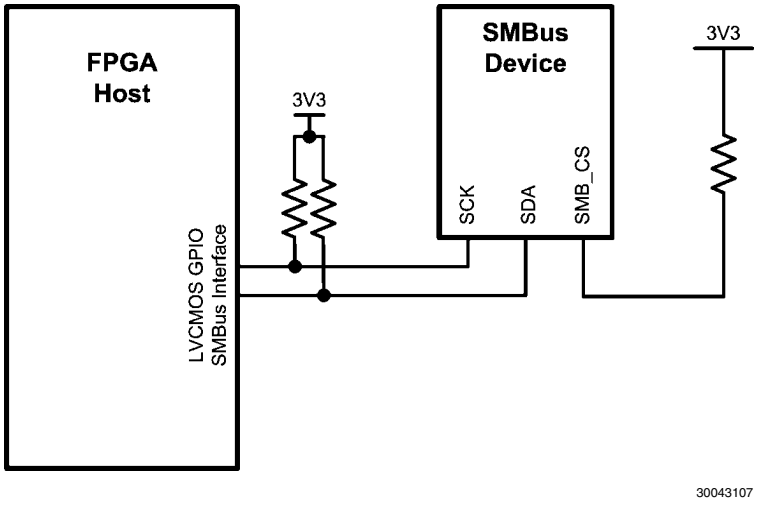


FIGURE 8. SMBus Configuration 1

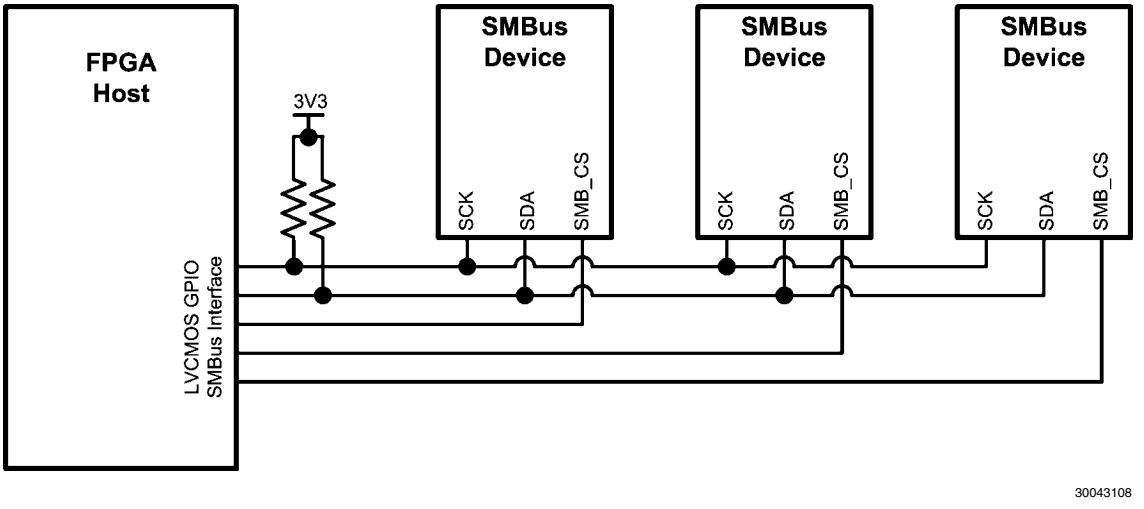


FIGURE 9. SMBus Configuration 2

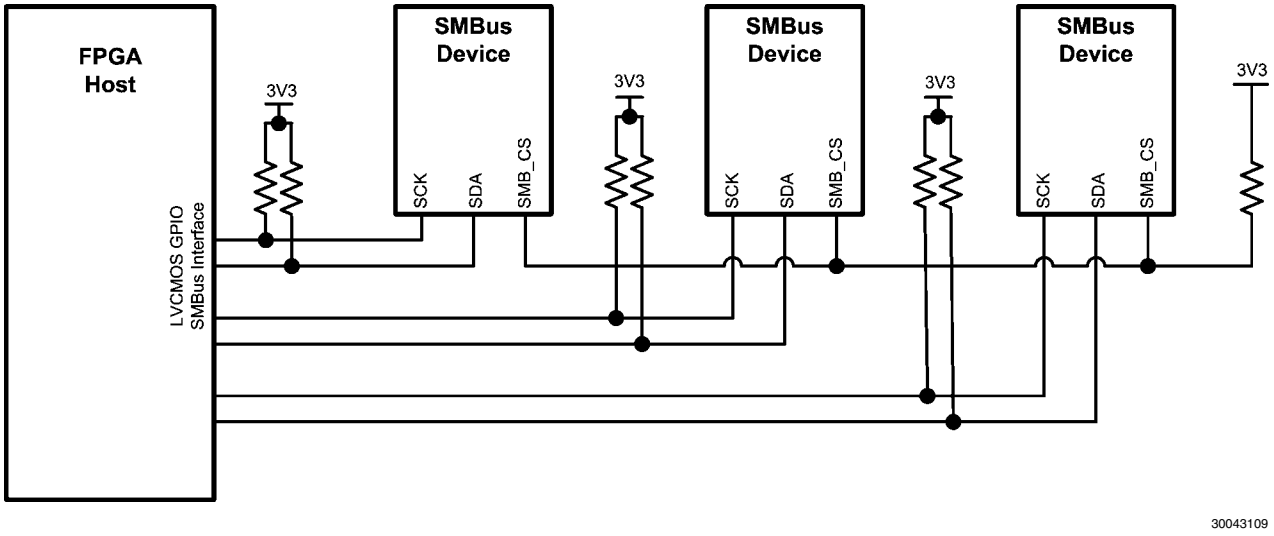


FIGURE 10. SMBus Configuration 3

PROPAGATION DELAY

Once the deserializer is locked, the amount of time it takes for a signal to travel from the high speed CML serial input through the device and out via the DDR LVDS interface is defined to be the propagation delay. The propagation delay through the DS32EL0124/DS32ELX0124 due to the analog circuitry is considered negligible compared to the time delay caused by the digital components. The information presented in this section allows system designers to predict the propagation delay through the device in terms of clock cycles which are proportional to the high speed serial line rate.

Each clock cycle shown in *Figure 11* is defined to be 1/20th of the high speed serial bit rate. For example, at a serial line rate of 3.125 Gbps the clock frequency of each delay cycle would be 156.25 MHz. Note, this is not the same frequency as the LVDS outputs, which would be 312.5 MHz for a serial line rate of 3.125 Gbps. Dashed lines in *Figure 11* indicate that the feature is disabled by default in that mode and therefore add no more time to the total propagation delay. In the last row, bypassed indicates that the data is sampled even though the feature is disabled by default. The sampling of the data results in an added amount of propagation delay as specified in the box.

Config Pins ($\overline{RS}$, $\overline{DC\_B}$)	CML Interface	NRZ Decoder	Descrambler	Lane Alignment Logic	DC Balance Decoder	LVDS Interface	Total Propagation Delay
	Data Flow →						
0, 0	2 clocks	— —	— —	3 clocks	1 clock	3-4 clocks	9-10 clocks
0, 1	2 clocks	1 clock	1 clock	3 clocks	1 clock	3-4 clocks	11-12 clocks
1, 0	2 clocks	1 clock	1 clock	3 clocks	— —	3-4 clocks	10-11 clocks
1, 1	2 clocks	1 clock (bypassed)	1 clock (bypassed)	3 clocks	— —	3-4 clocks	10-11 clocks

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FIGURE 11. Deserializer Propagation Delay

PROPAGATION DELAY FOR RETIMED LOOP THROUGH DRIVER — DS32ELX0124 ONLY

If the loop through driver is enabled in the DS32ELX0124, the propagation delay can also be defined as the amount of time it takes a signal to pass from the high speed CML serial input to the retimed loop through driver output. This time delay is measured in CDR clock cycles. The CDR clock frequency is equal to high speed serial line rate or one high speed serial bit width. For example, if the high speed serial line rate is 3.125 Gbps, then the CDR clock frequency is 3.125 GHz. The propagation delay from the high speed input to the loop through driver output is 1 CDR clock.

Applications Information

GPIO PINS

The GPIO pins can be useful tools when debugging or evaluating the system. For specific GPIO configurations and functions refer to registers 2, 3, 4, 5 and 6 in the device register map.

GPIO pins are commonly used when there are multiple deserializers on the same SMBus. In order to program individual settings into each serializer, they will each need to have a unique SMBus address. To reprogram multiple deserializers on a single SMBus, configure the first deserializer such that the SMBus lines are connected to the FPGA or host controller. The CS pin of the second serializer should be tied to GPIO0 of the first deserializer, with the CS pin of the next deseriazlier tied to GPIO0 of its preceding deserializer. By holding all of the GPIO0 pins low, the first deserializer's address may now be reprogrammed by writing to register 0. The first deserializer's GPIO pin can now be asserted and the second deserializer's address may now be reprogrammed.

HIGH SPEED COMMUNICATION MEDIA

Using the deserializer's integrated equalizer blocks in combination with the DS32EL0421 or DS32ELX0421's integrated de-emphasis block allows data to be transmitted across a variety of media at high speeds. Factors that can limit device performance include excessive input clock jitter, noisy power rails, EMI from nearby noisy components and poor layout techniques. Although many cables contain wires of similar gauge and shielding, performance can vary greatly depending on the quality of the connector.

The DS32ELX0124 also has a programmable de-emphasis block on its retimed loop through output TxOUT+/-. The de-emphasis setting for the loop through driver is programmed through the SMBus.

REDUNDANCY APPLICATIONS

The DS32ELX0124 has two high speed CML serial inputs. SMBus register control allows the host device to monitor for errors or link loss on the active input channel. This enables the host device, usually an FPGA, to switch to the secondary input if problems occur with the primary input.

LINK AGGREGATION

Multiple DS32EL0421/DS32ELX0421 serializers and D32EL0124/DS32ELX0124 deserializers can be aggregated together if an application requires a data throughput of more than 3.125 Gbps. By utilizing the data valid signal of each device, the system can be properly deskewed to allow for a single cable, such as CAT-6, DVI-D, or HDMI, to carry data payloads beyond 3.125 Gbps.

Link aggregation configurations can also be implemented in applications which require longer cable lengths. In these type of applications the data rate of each serializer and deserializer chipset can be reduced, such that the applications' net data throughput is still the same. Since each high speed channel is now operating at a fraction of the original data rate, the loss over the cable is reduced, allowing for greater lengths of cable to be used in the system.

For more information regarding link aggregation please see Application Note 1887, Expanding the Payload with National's FPGA-Link DS32ELX0421 and DS32ELX0124 Serializer and Deserializer.

REACH EXTENSION

The DS32ELX0124 deserializer contains a retimed loop through CML serial output. The loop through driver also has programmable de-emphasis making this device capable of reach extension applications.

DAISY CHAINING

The loop through driver of the DS32ELX0124 deserializer can be used to string together deserializers in a daisy chain configuration. This allows a single data source such as a DS32EL0421 serializer to communicate to multiple receiving systems.

LAYOUT GUIDELINES

It is important to follow good layout practices for high speed devices. The length of LVDS input traces should not exceed 40 inches. In noisy environments the LVDS traces may need to be shorter to prevent data corruption due to EMI. Noisy components should not be placed next to the LVDS or CML traces. The LVDS and CML traces must have a controlled differential impedance of 100Ω. Do not place termination resistors at the CML inputs or output, the DS32EL0124 and DS32ELX0124 have internal termination resistors. It is recommended to avoid using vias. Each pair of vias creates an impedance mismatch in the transmission line and result in reflections, which can greatly lower the maximum distance of the high speed data link. If vias are required, they should be placed symmetrically on each side of the differential pair. For more tips and detailed suggestions regarding high speed board layout principles, please consult the LVDS Owner's Manual.

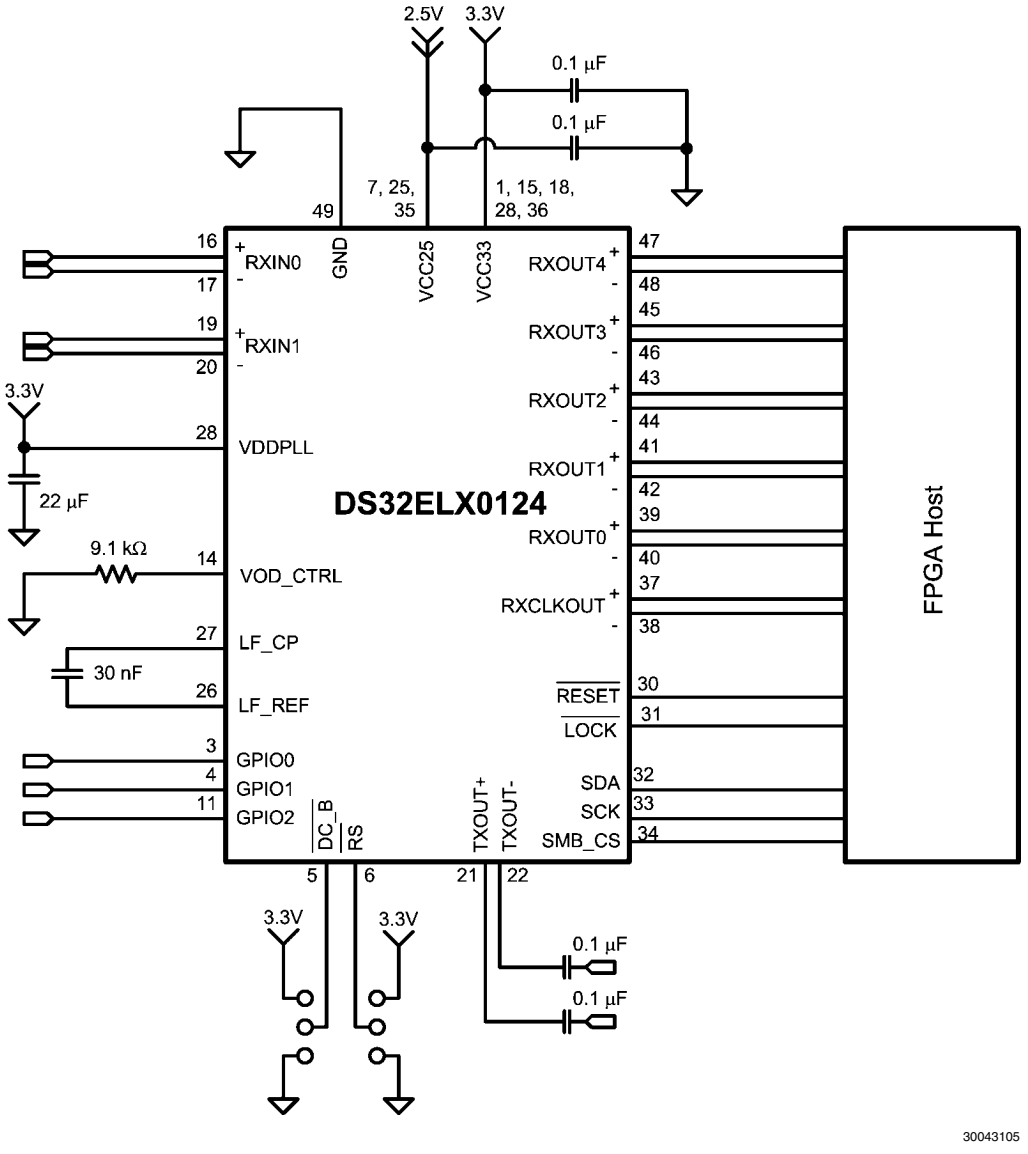
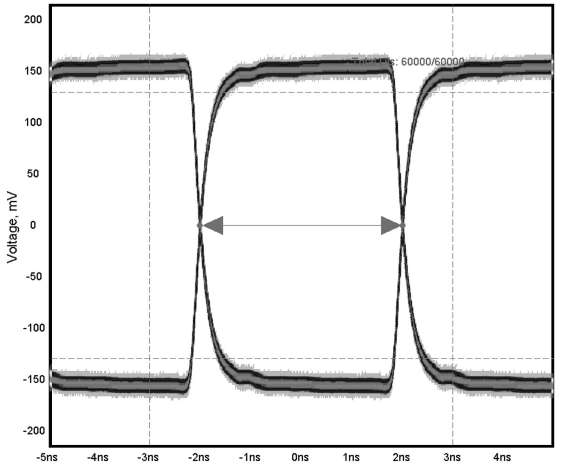


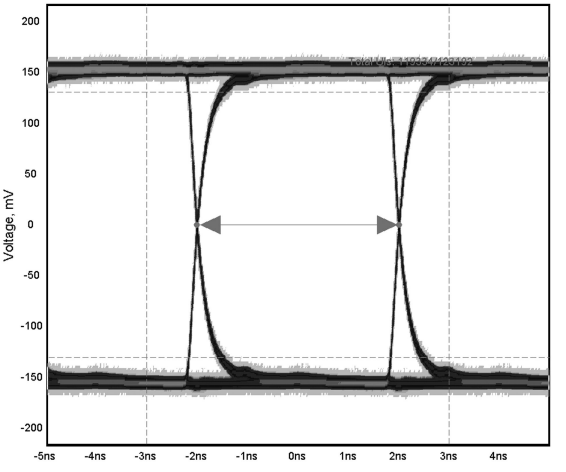
FIGURE 12. Typical Interface Circuit

Typical Performance Characteristics

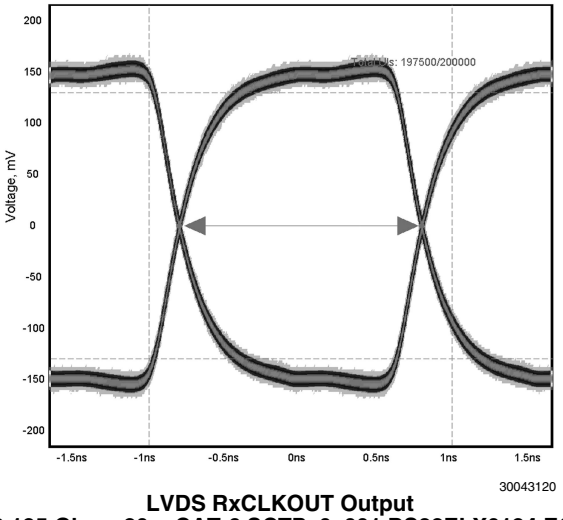
The eye diagrams shown below illustrate the typical performace of the DS32ELX0124/DS32EL0124 configured with $\overline{RS}$ = 0, $\overline{DC\_B}$ = 0, for the conditions listed below each figure. The PRBS-15 data was generated by a low cost FPGA, which used an LMK03000C to generate the various clock frequencies. The data was then sent to a DS32ELX0421 configured with $\overline{RS}$ = 0, $\overline{DC\_B}$ = 0, which transmitted the data across the specified cable type and length at the specified data rate. The signal conditioning settings used for each measurement are also listed below the figures.



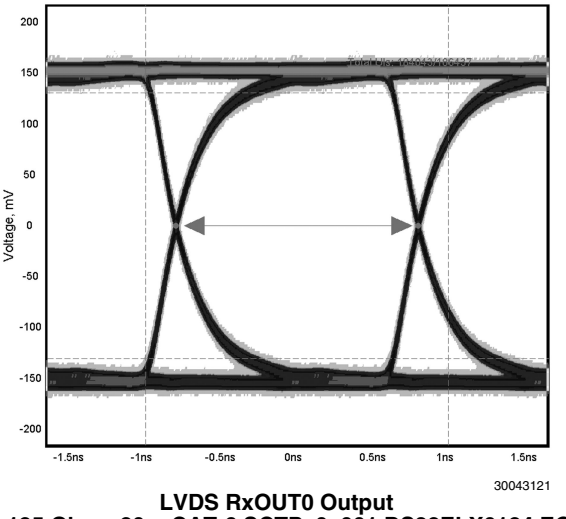
LVDS RxCLKOUT Output
(1.25 Gbps, 40m CAT-5e, 0x000 DS32ELX0124 EQ setting, 0x10 DS32EL0421 De-Emphasis setting)



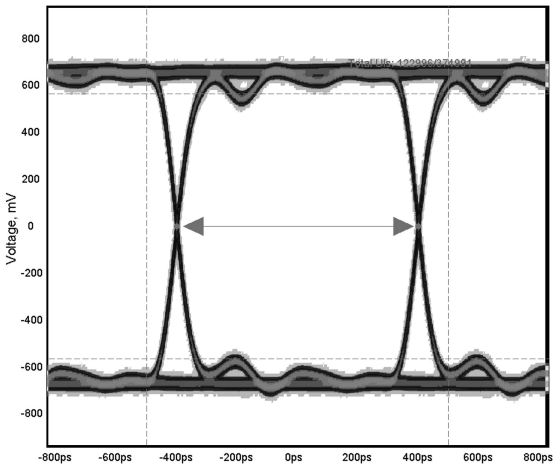
LVDS RxOUT0 Output
(1.25 Gbps, 40m CAT-5e, 0x000 DS32ELX0124 EQ setting, 0x10 DS32EL0421 De-Emphasis setting)



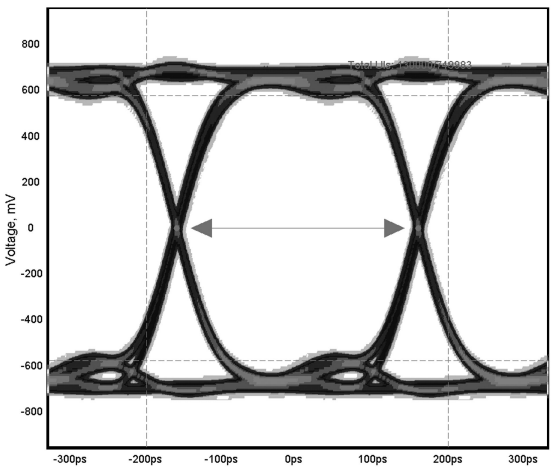
LVDS RxCLKOUT Output
(3.125 Gbps, 20m CAT-6 SCTP, 0x001 DS32ELX0124 EQ setting, 0x10 DS32EL0421 De-Emphasis setting)



LVDS RxOUT0 Output
(3.125 Gbps, 20m CAT-6 SCTP, 0x001 DS32ELX0124 EQ setting, 0x10 DS32EL0421 De-Emphasis setting)



Retimed Loop Through Output
(1.25 Gbps, 40m CAT-5e, 0x000 DS32ELX0124 EQ setting, 0x10 DS32EL0421 De-Emphasis setting)



Retimed Loop Through Output
(3.125 Gbps, 20m CAT-6 SCTP, 0x001 DS32ELX0124 EQ setting, 0x10 DS32EL0421 De-Emphasis setting)

Register Map

The register information for the deserializer is shown in the table below. Some registers have been omitted or marked as reserved; these are for internal testing and should not be written to. Some register bits require an override bit to be set before they can be written to.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
00	Device ID	7:1	SMBus Address	R/W	58'h	Some systems will use all 8 bits as the device ID. This will shift the value from 58'h to B0'h
		0	Reserved		0	
01	Reset	7:1	Reserved		0	
		0	Software Reset	R/W	0	Reset the device. Does not affect device ID.
02	GPIO0 Config	7:4	GPIO0 Mode	R/W	0	0000: GP Out 0001: Signal Detect RxIN0 0010: BIST Status **All Others: Reserved**
		3:2	GPIO0 R Enable	R/W	01'b	00: Pullup/Pulldown disabled 01: Pulldown Enabled 10: Pullup Enabled 11: Reserved
		1	Input Enable	R/W	0	0: Input buffer disabled 1: Input buffer enabled
		0	Output Enable	R/W	1'b	0: Output Tri-State™ 1: Output enabled
03	GPIO1 Config	7:4	GPIO1 Mode	R/W	0	0000: Power On Reset 0001: GP Out 0010: Signal Detect RxIN1 0011:CDR Lock **All Others: Reserved**
		3:2	GPIO1 R Enable	R/W	01'b	00: Pullup/Pulldown disabled 01: Pulldown Enabled 10: Pullup Enabled 11: Reserved
		1	Input Enable	R/W	0	0: Input buffer disabled 1: Input buffer enabled
		0	Output Enable	R/W	1	0: Output Tri-State™ 1: Output enabled
04	GPIO2 Config	7:4	GPIO2 Mode	R/W	0	0000: GP Out 0001: Always on Clock Out 0010: LVDS Tx CLK 0011: CDR CLK **All Others: Reserved**
		3:2	GPIO2 R Enable	R/W	01'b	00: Pullup/Pulldown disabled 01: Pulldown Enabled 10: Pullup Enabled 11: Reserved
		1	Input Enable	R/W	0	0: Input buffer disabled 1: Input buffer enabled
		0	Output Enable	R/W	1'b	0: Output Tri-State™ 1: Output enabled
05	GP In	7:3	Reserved			
		2	GP In 2	R	0	Input value on GPIO2
		1	GP In 1	R	0	Input value on GPIO1
		0	GP In 0	R	0	Input value on GPIO0

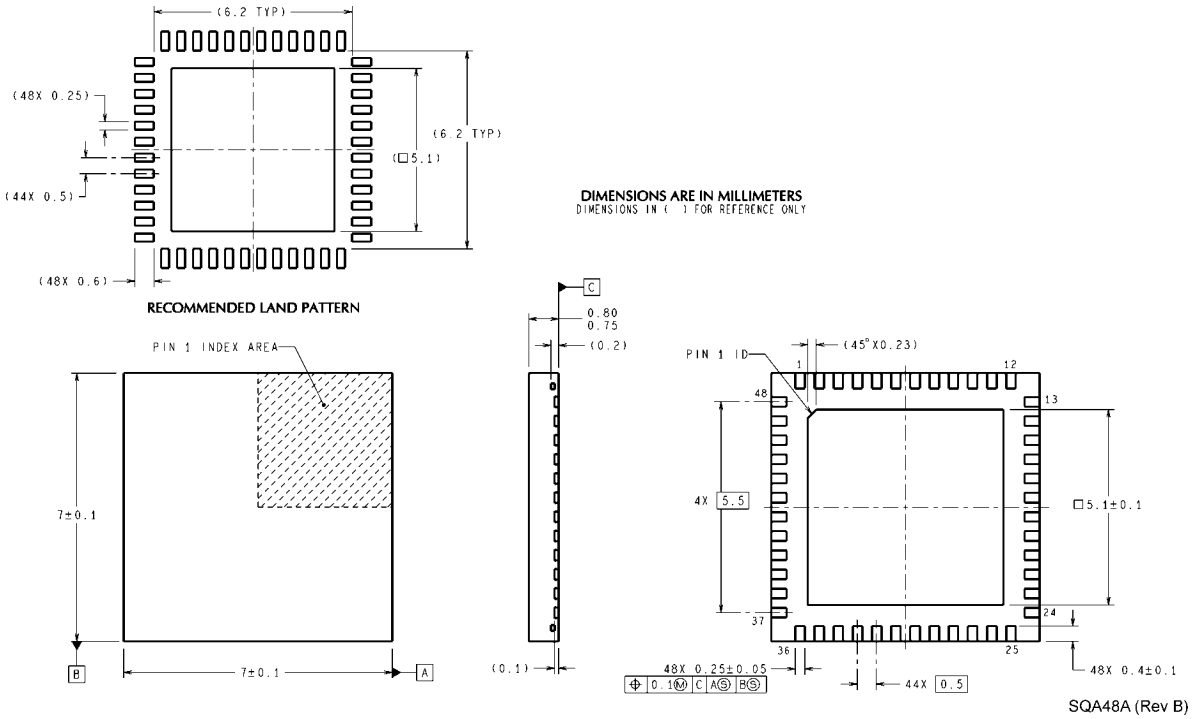
Addr (Hex)	Name	Bits	Field	R/W	Default	Description
06	GP Out	7:3	Reserved		0	
		2	GP Out 2	R/W	0	Output value on GPIO2
		1	GP Out 1	R/W	0	Output value on GPIO1
		0	GP Out 0	R/W	0	Output value on GPIO0
07 — 1F Reserved						
20	Device Config 0	7	LVDS Always On Clock	R/W	0	1: Disable 0: When not locked switch to Always On Clock
		6:3	Reserved		0	
		2	Reverse Data Order	R/W	0	0: Normal 1: Reverse output data order
		1	Reset Channel	R/W	0	Reset input high speed channel
		0	Digital Power Down	R/W	0	Power down parallel, seria-to-parallell, and always on clock
21	Device Config 1	7	Reserved		0	
		6	NRZI Decode Enable	R/W	0	Enable NRZI decoding of incoming data; requires an override bit
		5	Descramble Enable	R/W	0	Enabled the descrambler, requires an override bit
		4	Rx Mux	R/W	0	RX_MUX_SEL control register. requires an override bit
		3	Decode Bypass	R/W	0	Bypass DC Balance decoder. requires an override bit
		2	Training Sequence Enable	R/W	0	Enable training sequence. requires an override bit
		1:0	Device Configuartion	R/W	0	MSB: Remote Sense enable, active low LSB: DC balance encoder enable, active low requires an override bit
22	Device Config Override	7	Reserved		0	
		6	NRZ Override	R/W	0	Unlock bit 6 of register 21'h
		5	Descramble Override	R/W	0	Unlock bit 5 of register 21'h
		4	Rx Mux Override	R/W	0	Unlock bit 4 of register 21'h
		3	Reserved		0	
		2	Decode Bypass Override	R/W	0	Unlock bit 3 of register 21'h
		1	Traning Override	R/W	0	Unlock bit 2 of register 21'h
		0	Device Config Override	R/W	0	Unlock bits 1 and 0 of register 21'h
23 — 26 Reserved						

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
27	LVDS Per Channel Enable	7	LVDS V_{OD} High	R/W	0	0: LVDS V_{OD} normal operation. Setting used in Electrical Characteristics Table 1: Increases V_{OD}. Allows for longer traces to be driven, but consume more power
		6	LVDS Control	R/W	0	1: Allow SMBus to control LVDS per channel enable
		5	RxCLKOUT Enable	R/W	0	Enables RxCLKOUT output driver
		4	RxOUT4 Enable	R/W	0	Enables RxOUT4 output driver
		3	RxOUT3 Enable	R/W	0	Enables RxOUT3 output driver
		2	RxOUT2 Enable	R/W	0	Enables RxOUT2 output driver
		1	RxOUT1 Enable	R/W	0	Enables RxOUT1 output driver
		0	RxOUT0 Enable	R/W	0	Enables RxOUT0 output driver
28	LVDS Config	7	Reserved		0	
		6	LVDS Reset	R/W	0	Resets LVDS block
		5	LVDS Clock Rate	R/W	1	0:RxCLKOUT is DDR/2 1: RxCLKOUT is DDR
		4	LVDS Clock Invert	R/W	0	Inverts the polarity of the RxCLKOUT signal
		3:2	LVDS Clock Delay	R/W	10'b	00: 160 ps 11: -80 ps 80 ps step size
		1:0	Reserved		0	
29 — 2A Reserved						
2B	Event Config	7:4	Reserved		0	
		3	Event Count Select	R/W	0	0: Select CDR Event Counter for reading. Events include loss of signal detect or loss of CDR lock. 1: Select Data Event Counter for reading
		2	Reset CDR Error Count	R/W	0	Resets CDR event count
		1	Reset Link Error Count	R/W	0	Reset data event count
		0	Enable Count	R/W	0	Enable event coutners
2C	Reserved					
2D	Error Monitor	7:5	Reserved		0	
		4	Accumulate Error Enable	R/W	0	1: Enable counting accumulation of errors
		3	8b/10b Error disable	R/W	0	1: Disables 8b/10b decode errors from being counted or flagged on $\overline{\text{LOCK}}$ pin
		2	Clear Event Counter	R/W	0	1: clears errors in both the current and previous state of teh errors count
		1	Select Error Count	R/W	0	0: Number of errors in current run 1: Number of errors within the selected timing window
		0	Normal Error Disable	R/W	0	1: Disable exiting NORMAL state when the number of errors exceeds the error threshold
2E	Error Threshold LSBs	7:0	Error Threshold	R/W	10'h	Error threshold above which part stops transmittion of data — LSB
2F	Error Threshold MSBs	7:0	Error Threshold	R/W	0	Error threshold above which part stops transmittion of data — MSB

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
30 — 3A Reserved						
3B	Data Rate	7	Reserved		0	
		6:4	Frequency Range	R	111'b	001: Reserved 010: 1 — 1.3 Gbps 011: 1.2 — 1.8 Gbps 100: 1.5 — 2.1 Gbps 101: 1.9 — 2.7 Gbps 110: 2.4 — 3.2 Gbps 111: No Lock
		3:2	BIST Status	R	0	00: BIST passed 01: BIST failed to capture PREAMBLE 10: BIST pattern mode failed 11: BIST data sequence failed
		1	BIST Done	R	0	BIST pattern done. Set when not using repeat.
		0	BIST Allign Done	R	0	Alignment of incoming data done
3C	Reserved					
3D	Event Status	7:0	Event Count	R	0	Count of errors that caused a loss of link
3E	Error Status LSBs	7:0	Data Error Count	R	0	Number of errors in data — LSB
3F	Errors Status MSBs	7:0	Data Error Count	R	0	Number of errors in data — MSB
40 — 49 Reserved						
49	Loop Through Driver Config	7:5	Reserved		0	
		4	Termination Select	R/W	1	0: 75Ω 1: 50 Ω
		3:1	Output Amplitude Adjust	R/W	011'b	000: Level 7 001: Level 8 (Highest output) 010: Level 5 011: Level 6 (Normal output) 100: Level 4 101: Level 3 110: Level 2 111: Level 1 (Lowest output)
		0	Reserved		0	
60	EQ Attenuator	7:4	Reserved		0	
		3	Attenuator 0 Override	R/W	0	Overrides attenuation control in EQ 0
		2	Attenuator 1 Override	R/W	0	Overrides attenuation control in EQ 1
		1	Attenuator 0 Enable	R/W	0	1: enables attenuatorfor for EQ 0. Requires bit 3 to be set
		0	Attenuator 1 Enable	R/W	0	Enables attenuato for EQ 1. Requires bit 2 to be set.r

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
61	EQ Boost Control	7:5	EQ 0 Boost Control		0	Sets EQ level for RxIN0. Requires override bit 000: Off x10: Low (or 110) x01: Mid (or 101) x11: High (or 111)
		4:2	EQ 1 Boost Control		0	Sets EQ level for RxIN1. Requires override bit 000: Off x10: Low (or 110) x01: Mid (or 101) x11: High (or 111)
		1:0	Reserved		0	
62	Reserved					
63	EQ Override Control	7	Reserved		1	
		6	Reserved		1	
		5	EQ 0 Enable	R/W	1	1: Enables EQ for RxIN0
		4	EQ 1 Enable	R/W	0	1: Enables EQ for RxIN1
		3:0	Reserved		0	
64 — 66 Reserved						
67	LT De-Emphasis Control	7	Reserved		0	
		6:5	De-Emphasis Setting		0	00: Off 01: Low 10: Med 11: Max
		4:0	Reserved		0	

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number SQA48A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

Notes

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Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
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