DV2880T, DV2880U

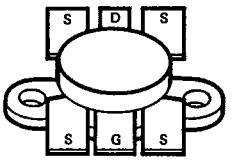
N-Channel Enhancement-Mode RF Power FETs

175 MHz
28-35 V
80 W
10 dB

FEATURES

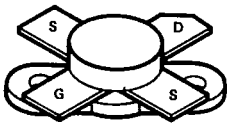
- 20:1 VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter

Package Type T



.500 J0 Flange

Package Type U



.500 SOE Flange

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Gate-Source Voltage	20V	Total Device Dissipation	160 W
Drain-Source Voltage	80V	Thermal Resistance, Junction to Case	1.1°C/W
Drain-Gate Voltage	80V	Junction Temperature	200°C
Drain Current (DC)	8 A	Storage Temperature	–65°C to 150°C

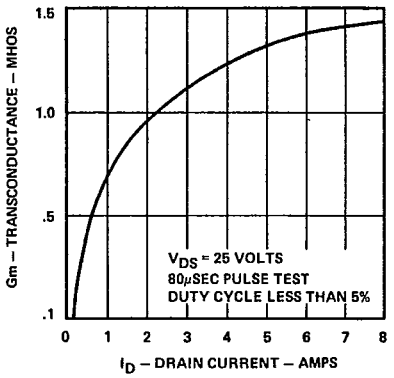
ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Symbol	Characteristics		Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage		80			V	V_{GS} = 0V, I_D = 20 mA
I_{DSS}	Drain-Source Leakage Current				4	mA	V_{GS} = 0V, V_{DS} = 30V
I_{GSS}	Gate-Source Leakage Current				400	nA	V_{GS} = 20V, V_{DS} = 0V
g_m[1]	D.C. Forward Transconductance		0.8	1.1		Mho	V_{DS} = 10V, I_D = 4A, ΔV_{GS} = 1.0V
$I_{D(on)}$[1]	On-State Drain Current			7		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage		2		6	V	V_{GS} = V_{DS}, I_D = 400 mA
C_{iss}	Common-Source Input Capacitance				210	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance				175	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance				25	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	DV2800T	10			dB	V_{DD} = 28V, Po = 80W, f = 175 MHz, I_{DQ} = 0.4A
		DV2880U	9				
η	Drain Efficiency		55	60		%	V_{DD} = 28V, Po = 80W, f = 175 MHz, I_{DQ} = 0.4A
V_{SWR}	Load Mismatch Tolerance		20:1				V_{DD} = 28V, Po = 80W, f = 175 MHz, I_{DQ} = 0.4A
N.F.	Noise Figure			4.0		dB	V_{DS} = 28V, I_D = 0.4A, f = 175 MHz

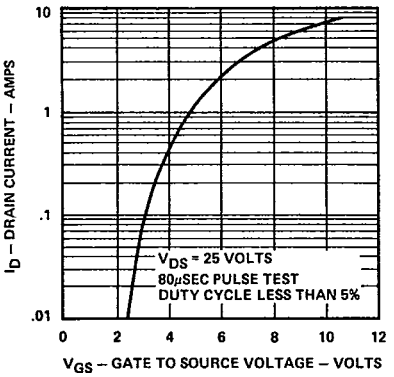
Note 1: Pulse Test—80 μs to 300 μs, 1% duty cycle

TYPICAL PERFORMANCE CURVES (25° C unless otherwise noted)

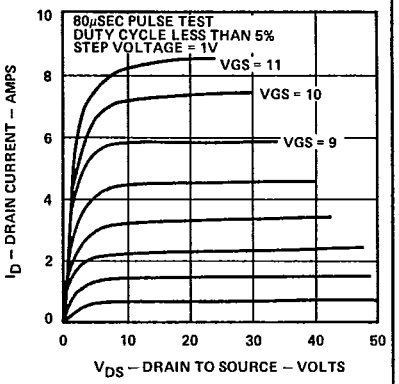
Transconductance vs Drain Current



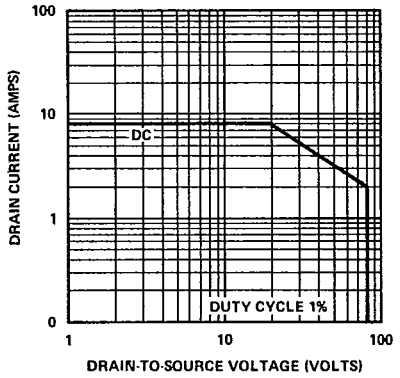
Transfer Characteristics



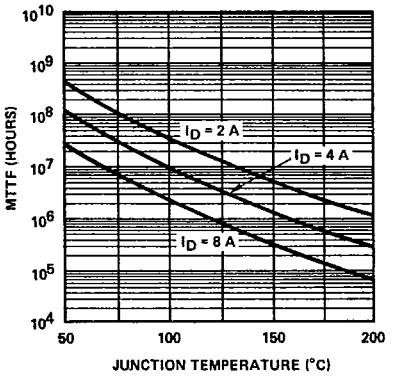
Output Characteristics



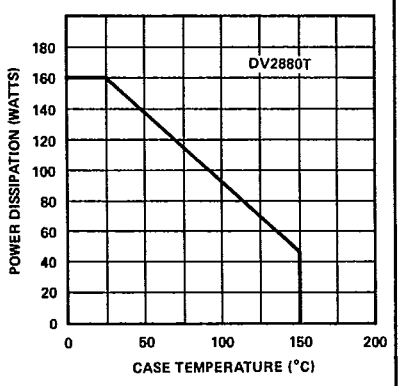
DC and Inductive Safe Operating Region $T_C = 25°C$



MTTF vs Temperature

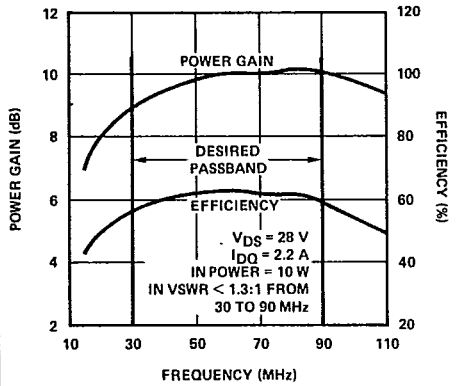


Power Dissipation vs Case Temperature

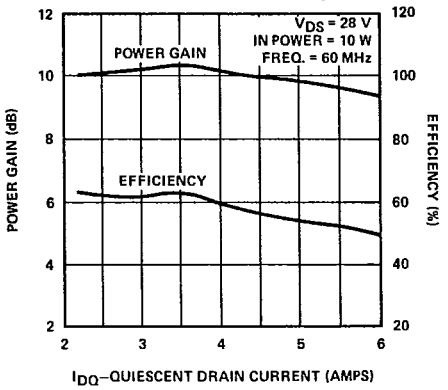


APPLICATIONS AND SYSTEMS DATA

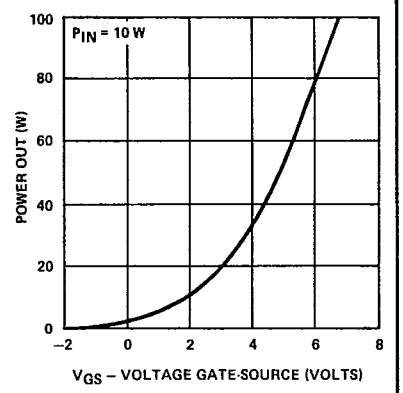
Power Gain and Efficiency vs Frequency



Efficiency vs I_{dq}



Output Power vs Gate-Source Bias



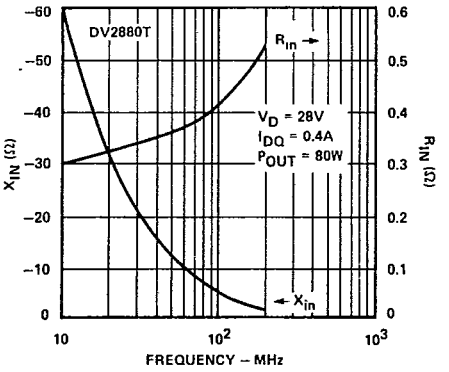
SMALL SIGNAL 2-PORT PARAMETERS

2-PORT Y-PARAMETER MATRIX IN MILLIMHOS

Freq	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
(MHz)	(Real	Imag)	(Real	Imag)	(Real	Imag)	(Real	Imag)
10	0	10.5	886	−47.6	0	−1.03	4.42	8.34
20	0.897	21.3	881	−37.5	0	−2.05	5.31	15.9
50	6.52	58.3	902	−106	.5	−5.65	7.61	42.5
100	20.1	128	1060	−294	2.13	−11.9	11.0	89.3
150	57.0	207	1220	−565	6.63	−19.8	21.4	134
200	125	322	1450	−964	12.8	−33.4	23.1	191
250	241	340	1230	−1.61	32.5	−48.7	14.9	226
300	520	219	215.5	−2.4	33.6	−96.9	−76.3	371
350	565	124	−243.2	−2.02	43.5	−123	−66.1	417
400	574	4.06	−695.7	−1.72	37.1	−166	−59.3	551
450	509	−35.6	−812.7	−1.35	30.2	−198	−17.0	644
500	477	−11.6	−800.4	−1.27	43.7	−258	−13.8	749

Condition: 28 V, 1.6 A

Equivalent Large Signal Series Input Impedance vs Frequency

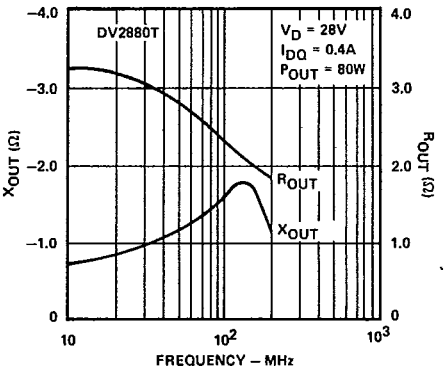


POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)
10	.798	−134°	25.1	106°	.00	18.4°	.691	−141°
20	.819	−154°	13.1	91.8°	.03	6.42°	.819	−157°
50	.839	−168°	4.51	71.8°	.03	−6.34°	.766	−166°
100	.884	−173°	1.95	51.1°	.02	−13.2°	.835	−169°
150	.921	−175°	1.04	40.4°	.016	−6.22°	.888	−172°
200	.943	−177°	.629	34.2°	.013	−1.27°	.917	−174°
250	.953	−179°	.436	28.3°	.013	24.5°	.939	−175°
300	.959	178°	.309	26.4°	.013	40.4°	.950	−176°
350	.962	178°	.234	24.4°	.015	50.7°	.954	−176°
400	.966	177°	.187	24.3°	.017	58.8°	.957	−177°
450	.963	176°	.157	25.9°	.020	65.5°	.958	−178°
500	.966	176°	.138	27.2°	.029	69.0°	.962	−178°

Condition: 28 V, 1.6 A

Equivalent Large Signal Series Output Impedance vs Frequency

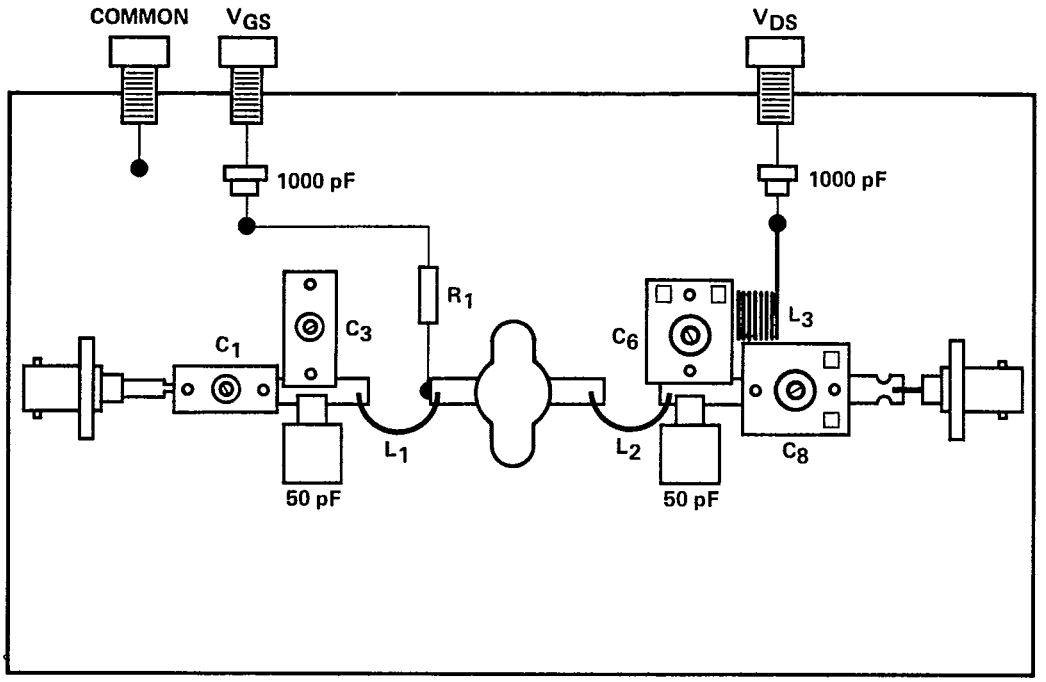


BROADBAND AMPLIFIER ABSTRACT

Besides identifying five distinct advantages of power VMOS FETs which makes them the "designer's choice" for wideband amplifier design, Application Note AN80-4 derives useful equations that allow for the establishment of power gain and low input VSWR. Described is a 100 W power amplifier extending across the 30 MHz to 90 MHz band with an input VSWR less than 1.2:1, and a power gain of typically 10 dB. See Application Note AN80-6 for ALC, AGC applications.

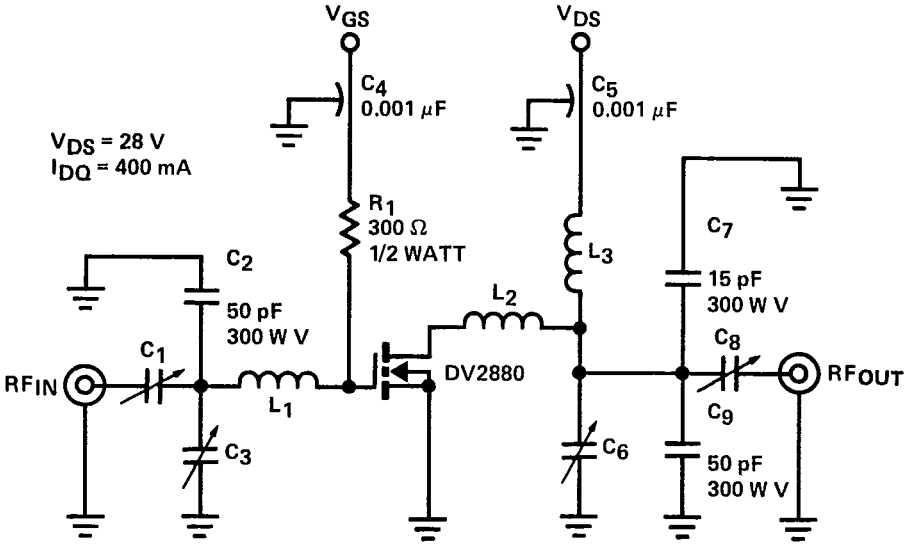
TEST FIXTURE

175 MHz Test Fixture

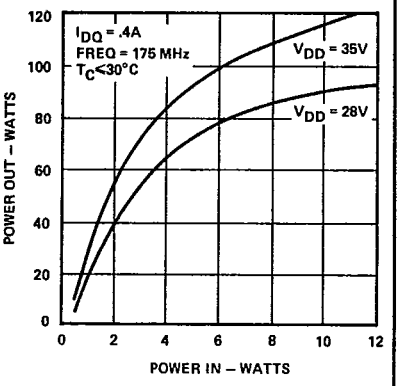


Scale: 3/4 of Original Size

175 MHz DV2880 Schematic Diagram



DV2880T Typical Output Power vs Input Power



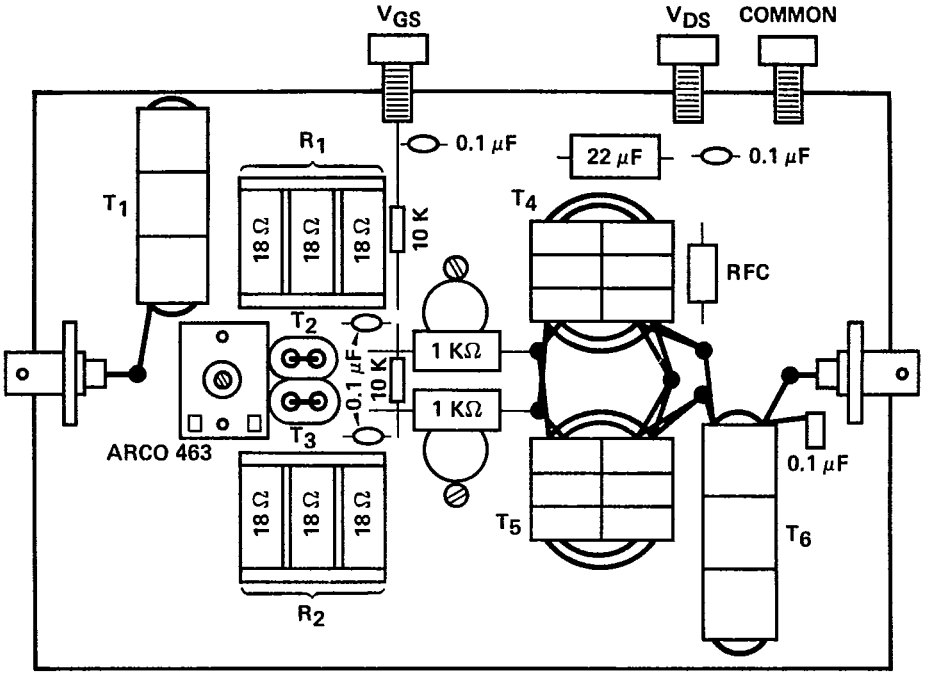
PARTS LIST

C_1, C_3, 4 to 40 pF ARCO #422 trimmer capacitors
C_6, C_8, 9 to 180 pF ARCO #463 trimmer capacitors
L_1, 1 3/16" length of #12 AWG (loop 1/2")
L_2, 1" length of #12 AWG (loop 0.4")
L_3, 8 turns #18 AWG enamel of 1/4" diameter, close wound
R_1, 300 Ω 1/2 watt

BROADBAND AMPLIFIER

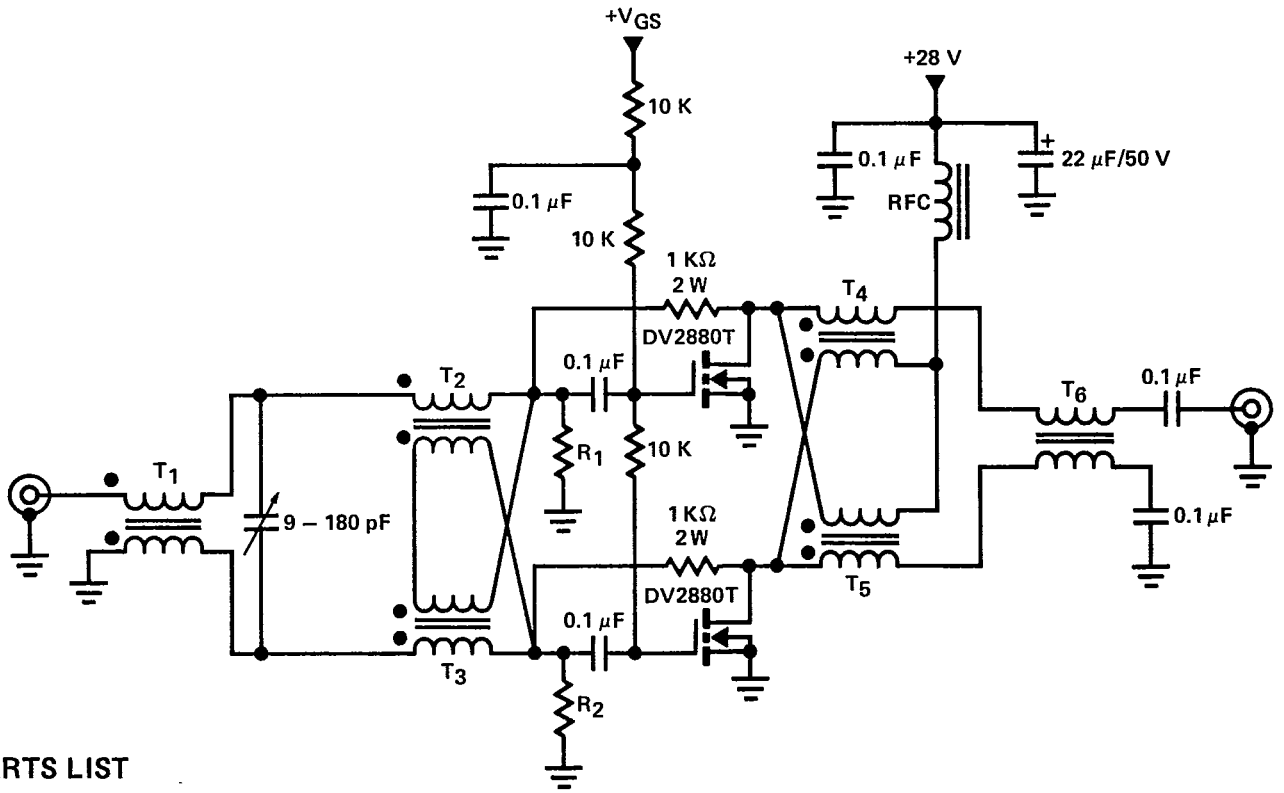
DV2880T

30 to 80 MHz Broadband Component Layout



Circuit Board Layout, Scale: 3/4 of Original Size Full–Scale PCB Shown on Last Page

100 Watt Broadband VMOS Power Amplifier



PARTS LIST

RFC ~ Ferroxcube P/N VK200 09/3B

T_1, T_6 ~ two turns of RG-196A/U 50 Ω coax wound on three balun cores placed end on end. Cores are Stackpole P/N 57-0973. $\mu_0 = 35$

T_2, T_3 ~ two turns #22 twisted pair, four turns per inch, wound on two balun core. Core is Stackpole P/N 57-0973. $\mu_0 = 35$

$T_4 = T_5$ ~ three turns of 25 Ω coax wound on 6 torroid cores. Cores are configured similar to balun style core, three cores per side. Two 50 Ω coax RG-196A/U were paralleled to simulate 25 Ω coax. Cores are Indiana General P/N F627-8-Q2

R1, R2 ~ three 18 Ω 2 watt carbon composition resistors in parallel