

SMC63A08

4-bit Single Chip Microcomputer

Preliminary



- 4-bit Low Cycle / Inst. Core CPU
- Built-in Dot-matrix Type LCD Driver
- Low Voltage Operation (0.9V Min.)
- Built-in Gate Array

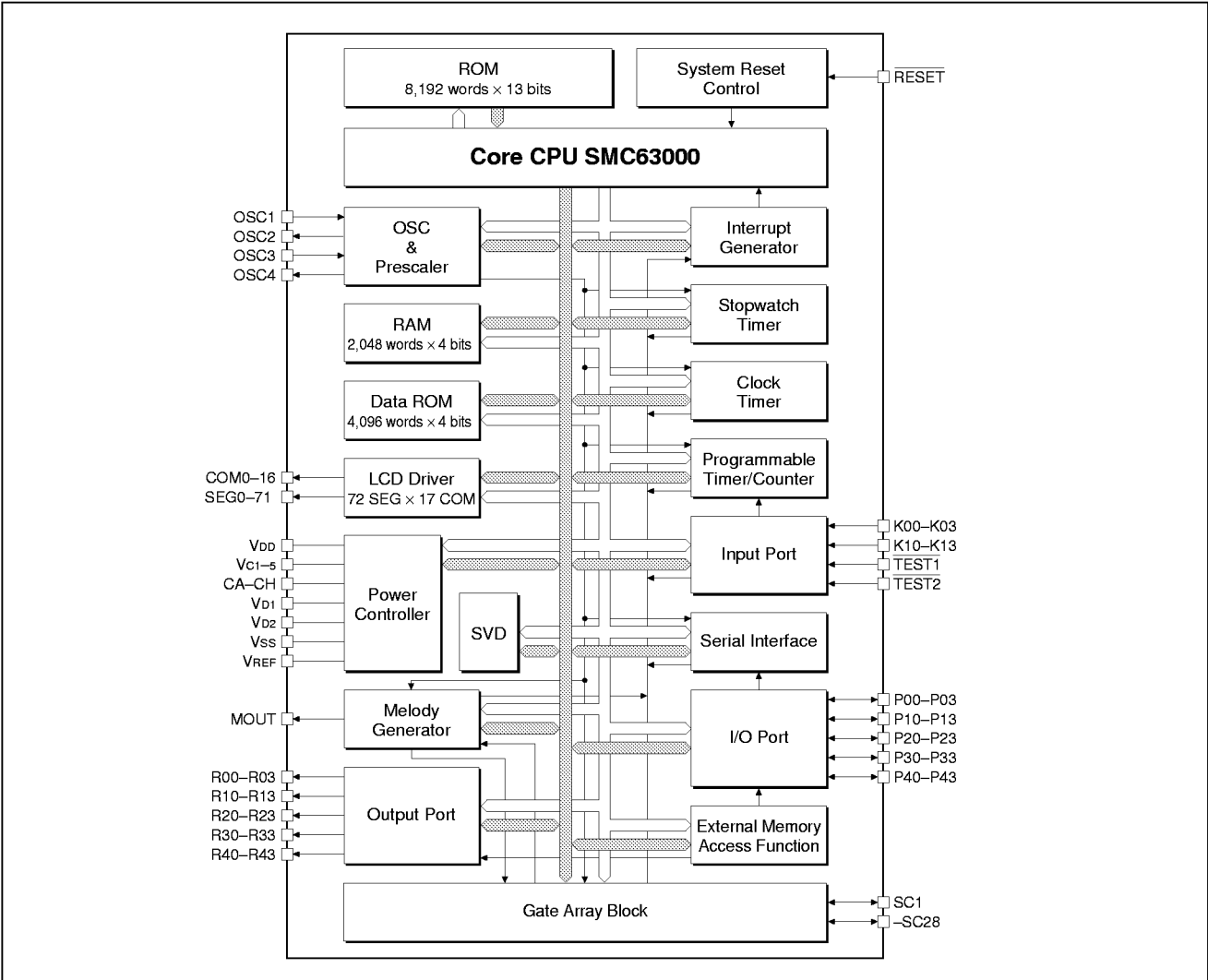
DESCRIPTION

The SMC63A08 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, dot-matrix type LCD driver, 5000 gates of gate array and counters. And the SMC63A08 can be operated by single Manganese battery with LCD display. So that the SMC63A08 is best suited for systems such as numeric pager.

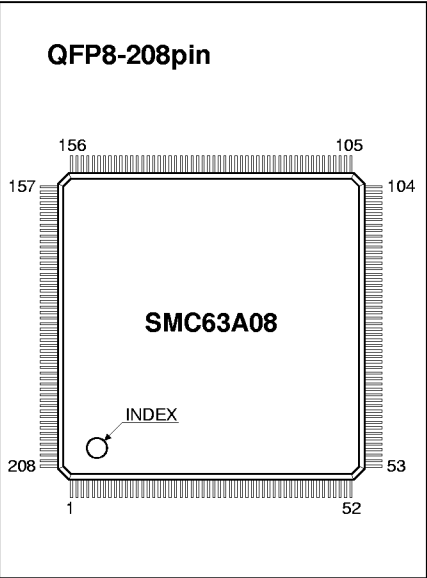
FEATURES

- CMOS LSI 4-bit parallel processing
- Main clock 32.768 / 76.8 / 153.8kHz (Mask option)
- Sub clock 1MHz (Typ.)
- Instruction set 46 kinds, 411 instructions
- Instruction execution time 32kHz 61μsec (Min.)
1MHz 2μsec (Min.)
- ROM capacity ROM : 8,192 × 13 bit
Data ROM : 4,096 × 4 bit
- RAM capacity Data RAM : 2,048 × 4 bit
Display RAM : 360 × 4 bit
- External memory capacity 512K × 2
- I/O port Input : 8 bit
Output : 20 bit
I/O : 20 bit
- LCD driver 72 segments × 8 / 16 / 17 commons
- Gate array 5,000 usable gates (Bus interface)
- Melody Equivalent SVM7100
- Supply voltage detect 16 levels by programmable (from 1.05 to 2.60V)
- Clock timer 1 ch.
- Watchdog timer Built-in
- Programmable timer 8 bit × 2 ch.
- Serial interface Synchronous 8-bit
- Interrupts External : Key interrupt 2 lines
Internal : Clock timer 4 lines
: Stopwatch timer 2 lines
: Programmable timer 2 lines
: Serial interface 1 line
: Gate array 4 lines
: Melody 1 line
- Package QFP8-208pin (plastic), Die form
- Supply voltage 0.9 to 3.6V
- Current consumption HALT mode (32.768kHz) : 1.5μA (Typ.)

BLOCK DIAGRAM



PIN CONFIGURATION



No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	SEG62	27	N.C.	53	TEST2	79	P40	105	SC1	131	SC27	157	N.C.	183	N.C.
2	SEG63	28	N.C.	54	TEST1	80	P33	106	SC2	132	SC28	158	N.C.	184	SEG39
3	SEG64	29	CA	55	MOUT	81	P32	107	SC3	133	COM7	159	SEG16	185	SEG40
4	SEG65	30	CB	56	R43	82	P31	108	SC4	134	COM6	160	SEG17	186	SEG41
5	SEG66	31	CC	57	R42	83	P30	109	SC5	135	COM5	161	SEG18	187	SEG42
6	SEG67	32	CD	58	R41	84	P23	110	SC6	136	COM4	162	SEG19	188	SEG43
7	SEG68	33	CE	59	R40	85	P22	111	SC7	137	COM3	163	SEG20	189	SEG44
8	SEG69	34	CF	60	R33	86	P21	112	SC8	138	COM2	164	SEG21	190	SEG45
9	SEG70	35	CG	61	R32	87	P20	113	SC9	139	COM1	165	SEG22	191	SEG46
10	SEG71	36	CH	62	R31	88	P13	114	SC10	140	COM0	166	SEG23	192	SEG47
11	COM8	37	Vc5	63	R30	89	P12	115	SC11	141	SEG0	167	SEG24	193	SEG48
12	COM9	38	Vc4	64	R23	90	P11	116	SC12	142	SEG1	168	SEG25	194	SEG49
13	COM10	39	Vc3	65	R22	91	P10	117	SC13	143	SEG2	169	SEG26	195	SEG50
14	COM11	40	Vc2	66	R21	92	P03	118	SC14	144	SEG3	170	SEG27	196	SEG51
15	COM12	41	Vc1	67	R20	93	P02	119	SC15	145	SEG4	171	SEG28	197	SEG52
16	COM13	42	Vd2	68	R13	94	P01	120	SC16	146	SEG5	172	SEG29	198	SEG53
17	COM14	43	VSS	69	R12	95	P00	121	SC17	147	SEG6	173	SEG30	199	SEG54
18	COM15	44	OSC1	70	R11	96	K13	122	SC18	148	SEG7	174	SEG31	200	SEG55
19	COM16	45	OSC2	71	R10	97	K12	123	SC19	149	SEG8	175	SEG32	201	SEG56
20	N.C.	46	Vd1	72	R03	98	K11	124	SC20	150	SEG9	176	SEG33	202	SEG57
21	N.C.	47	OSC3	73	R02	99	K10	125	SC21	151	SEG10	177	SEG34	203	SEG58
22	N.C.	48	OSC4	74	R01	100	K03	126	SC22	152	SEG11	178	SEG35	204	SEG59
23	N.C.	49	VDD	75	R00	101	K02	127	SC23	153	SEG12	179	SEG36	205	SEG60
24	N.C.	50	VREF	76	P43	102	K01	128	SC24	154	SEG13	180	SEG37	206	SEG61
25	N.C.	51	RESET	77	P42	103	K00	129	SC25	155	SEG14	181	SEG38	207	N.C.
26	N.C.	52	N.C.	78	P41	104	N.C.	130	SC26	156	SEG15	182	N.C.	208	N.C.

N.C. : No Connection

PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V _{DD}	49	–	Power (+) supply pin
V _{SS}	43	–	Power (–) supply pin
V _{D1}	46	–	Oscillation/internal logic system regulated voltage output pin
V _{D2}	42	–	Supply voltage doubler/halver output pin
V _{C1} –V _{C5}	41–37	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option)
V _{REF}	50	O	LCD system power supply testing pin
CA–CF	29–34	–	LCD system boosting/reducing capacitor connecting pin
CG, CH	35, 36	–	Supply voltage doubling/halving capacitor connecting pin
OSC1	44	I	Crystal oscillation input pin
OSC2	45	O	Crystal oscillation output pin
OSC3	47	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	48	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	103–100	I	Input port
K10–K13	99–96	I	Input port
P00–P03	95–92	I/O	I/O port
P10–P13	91–88	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	87	I/O	I/O port (switching to chip select CS0 output is possible by software)
P21	86	I/O	I/O port (switching to chip select CS1 output is possible by software)
P22	85	I/O	I/O port (switching to CL output is possible by software)
P23	84	I/O	I/O port (switching to FR output is possible by software)
P30–P33	83–80	I/O	I/O port (switching to external data bus D00–D03 is possible by software)
P40–P43	79–76	I/O	I/O port (switching to external data bus D04–D07 is possible by software)
R00	75	O	Output port (switching to WR output is possible by software)
R01	74	O	Output port (switching to RD output is possible by software)
R02	73	O	Output port (switching to TOUT output is possible by software)
R03	72	O	Output port (switching to FOUT output is possible by software)
R10–R13	71–68	O	Output port (switching to external address bus A00–A03 is possible by software)
R20–R23	67–64	O	Output port (switching to external address bus A04–A07 is possible by software)
R30–R33	63–60	O	Output port (switching to external address bus A08–A12 is possible by software)
R40–R43	59–56	O	Output port (switching to external address bus A13–A15 is possible by software)
COM0–COM16	140–133, 11–19	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG71	141–156, 159–181, 184–206, 1–10	O	LCD segment output pin
MOUT	55	O	Melody output pin
SC1–SC28	105–132	I, O, I/O	G/A input/output pin
RESET	51	I	Initial reset input pin
TEST1	54	I	Testing input pin
TEST2	53	I	Testing input pin

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{DD}	–0.5 to 7.0	V
Input voltage (1)	V _I	–0.5 to V _{DD} + 0.3	V
Input voltage (2)	V _{IOSC}	–0.5 to V _{D1} + 0.3	V
Permissible total output current *1	ΣI _{VDD}	10	mA
Operating temperature	T _{opr}	–20 to 70	°C
Storage temperature	T _{stg}	–65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	–
Permissible dissipation *2	P _D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP8-208pin).

Recommended Operating Conditions

(T_a=–20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	V _{SS} =0V				
		Doubler mode (OSC3 OFF)	0.9	1.1	1.30	V
		Normal mode (OSC3 OFF)	1.30	3.0	3.6	V
		Normal mode (OSC3 ON)	2.2	3.0	3.6	V
Oscillation frequency (1)	f _{OSC1}	Halver mode (OSC3 OFF)	2.6	3.0	3.6	V
		Any one is selected	–	32.768	–	kHz
			–	76.8	–	kHz
			–	153.6	–	kHz
Oscillation frequency (2)	f _{OSC3}	Duty 50±5%, V _{DC} =“1”, V _{DD} =2.2 to 3.6V	50	1,000	1,200	kHz

● DC Characteristics

(Unless otherwise specified: $V_{DD}=1.5V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $T_a=25^{\circ}C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$, $C_9-C_{10}=0.4\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43	$0.8 \cdot V_{DD}$		V_{DD}	V
High level input voltage (2)	V_{IH2}	RESET, TEST1, TEST2	$0.9 \cdot V_{DD}$		V_{DD}	V
Low level input voltage (1)	V_{IL1}	K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43	0		$0.2 \cdot V_D$	V
Low level input voltage (2)	V_{IL2}	RESET, TEST1, TEST2	0		$0.1 \cdot V_{DD}$	V
High level input current	I_{IH}	$V_{IH}=1.5V$ K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43 RESET, TEST1, TEST2	0		0.5	μA
Low level input current (1)	I_{IL1}	$V_{IL1}=V_{SS}$ No pull up K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43 RESET, TEST1, TEST2	-0.5		0	μA
Low level input current (2)	I_{IL2}	$V_{IL2}=V_{SS}$ With pull up K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43 RESET, TEST1, TEST2	-8	-5	-3	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.9 \cdot V_{DD}$ R00-03, R10-13, R20-23, R30-33 R40-43, P00-03, P10-13, P20-23 P30-33, P40-43			-0.3	mA
High level output current (2)	I_{OH2}	$V_{OH2}=0.9 \cdot V_{DD}$ MOUT			-0.3	mA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.1 \cdot V_{DD}$ R00-03, R10-13, R20-23, R30-33 R40-43, P00-03, P10-13, P20-23 P30-33, P40-43	0.7			mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.1 \cdot V_{DD}$ MOUT	0.7			mA
Common output current	I_{OH3}	$V_{OH3}=V_{C5}-0.05V$ COM0-COM16			-30	μA
	I_{OL3}	$V_{OL3}=V_{SS}+0.05V$	30			μA
Segment output current	I_{OH4}	$V_{OH4}=V_{C5}-0.05V$ SEG0-SEG71			-10	μA
	I_{OL4}	$V_{OL4}=V_{SS}+0.05V$	10			μA

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $T_a=25^{\circ}C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$, $C_9-C_{10}=0.4\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43	$0.8 \cdot V_{DD}$		V_{DD}	V
High level input voltage (2)	V_{IH2}	RESET, TEST1, TEST2	$0.9 \cdot V_{DD}$		V_{DD}	V
Low level input voltage (1)	V_{IL1}	K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43	0		$0.2 \cdot V_D$	V
Low level input voltage (2)	V_{IL2}	RESET, TEST1, TEST2	0		$0.1 \cdot V_{DD}$	V
High level input current	I_{IH}	$V_{IH}=3.0V$ K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43 RESET, TEST1, TEST2	0		0.5	μA
Low level input current (1)	I_{IL1}	$V_{IL1}=V_{SS}$ No pull up K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43 RESET, TEST1, TEST2	-0.5		0	μA
Low level input current (2)	I_{IL2}	$V_{IL2}=V_{SS}$ With pull up K00-03, K10-13, P00-03 P10-13, P20-23, P30-33, P40-43 RESET, TEST1, TEST2	-16	-10	-6	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.9 \cdot V_{DD}$ R00-03, R10-13, R20-23, R30-33 R40-43, P00-03, P10-13, P20-23 P30-33, P40-43			-1.5	mA
High level output current (2)	I_{OH2}	$V_{OH2}=0.9 \cdot V_{DD}$ MOUT			-1.5	mA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.1 \cdot V_{DD}$ R00-03, R10-13, R20-23, R30-33 R40-43, P00-03, P10-13, P20-23 P30-33, P40-43	6			mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.1 \cdot V_{DD}$ MOUT	6			mA
Common output current	I_{OH3}	$V_{OH3}=V_{C5}-0.05V$ COM0-COM16			-30	μA
	I_{OL3}	$V_{OL3}=V_{SS}+0.05V$	30			μA
Segment output current	I_{OH4}	$V_{OH4}=V_{C5}-0.05V$ SEG0-SEG71			-10	μA
	I_{OL4}	$V_{OL4}=V_{SS}+0.05V$	10			μA

● Analog Circuit Characteristics

(Unless otherwise specified: VDD=1.5V when VC1 standard is selected, VDD=3.0V when VC2 standard is selected, VSS=0V, fOSC1=32.768kHz, CG=25pF, Ta=25°C, VD1/VC1/VC2/VC4/VC5 are internal voltage, C1–C8=0.2μF, C9–C10=0.4μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage (when VC1 standard is selected)	VC1	VDD=1.5V Connect 1MΩ load resistor between VSS and VC1 (No panel load)	LC0–3="0"			
				Typ.×0.88	Typ.×1.12	V
	VC2	Connect 1MΩ load resistor between VSS and VC2 (No panel load)	2•VC1		2•VC1 ×0.9	V
	VC4	Connect 1MΩ load resistor between VSS and VC4 (No panel load)	3•VC1		3•VC1 ×0.9	V
	VC5	Connect 1MΩ load resistor between VSS and VC5 (No panel load)	4•VC1		4•VC1 ×0.9	V
LCD drive voltage (when VC2 standard is selected)	VC1	Connect 1MΩ load resistor between VSS and VC1 (No panel load)	1/2•VC2 -0.1		1/2•VC2 ×0.95	V
	VC2	VDD=3.0V Connect 1MΩ load resistor between VSS and VC2 (No panel load)	LC0–3="0"			
				Typ.×0.88	Typ.×1.12	V
	VC4	Connect 1MΩ load resistor between VSS and VC4 (No panel load)	3/2•VC2		3/2•VC2 ×0.95	V
	VC5	Connect 1MΩ load resistor between VSS and VC5 (No panel load)	2•VC2		2•VC2 ×0.95	V
SVD voltage	VSVD	SVDS0–3="0"	0.95	1.05	1.15	V
		SVDS0–3="1"	1.05	1.10	1.15	V
		SVDS0–3="2"	1.10	1.15	1.20	V
		SVDS0–3="3"	1.15	1.20	1.25	V
		SVDS0–3="4"	1.20	1.25	1.30	V
		SVDS0–3="5"	1.25	1.30	1.35	V
		SVDS0–3="6"	1.35	1.40	1.45	V
		SVDS0–3="7"	1.55	1.60	1.65	V
		SVDS0–3="8"	1.90	1.95	2.00	V
		SVDS0–3="9"	1.95	2.00	2.05	V
		SVDS0–3="10"	2.00	2.05	2.10	V
		SVDS0–3="11"	2.05	2.10	2.15	V
		SVDS0–3="12"	2.15	2.20	2.25	V
		SVDS0–3="13"	2.25	2.30	2.35	V
		SVDS0–3="14"	2.45	2.50	2.55	V
		SVDS0–3="15"	2.55	2.60	2.65	V
SVD circuit response time	tSVD				100	μS

● Current Consumption

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $C_G=25pF$, $T_a=25^{\circ}C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$, $C_9-C_{10}=0.4\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I _{OP}	During HALT	32.768kHz	1.5	3.0	μA
		Normal mode	76.8kHz	2.0	4.5	μA
		LCD power OFF	153.6kHz	4.5	10.0	μA
		During HALT	32.768kHz	6.5	12.0	μA
		Normal mode *1	76.8kHz	8.0	15.0	μA
		LCD power ON	153.6kHz	11.0	20.0	μA
		During HALT	32.768kHz	13.0	27.0	μA
		Doubler mode ($V_{DD}=1.2V$) *1	76.8kHz	15.0	29.0	μA
		LCD power ON	153.6kHz	22.0	40.0	μA
		During HALT	32.768kHz	3.5	8.0	μA
		Halver mode ($V_{DD}=3.0V$) *1	76.8kHz	4.0	9.0	μA
		LCD power ON	153.6kHz	6.0	12.0	μA
		During execution	32.768kHz	10	20	μA
		Normal mode *1	76.8kHz	18	30	μA
		LCD power ON	153.6kHz	35	55	μA
			1MHz (CR oscillation)	320	600	μA
			1MHz (Ceramic oscillation)	300	500	μA
		During execution	32.768kHz	22	40	μA
		Doubler mode ($V_{DD}=1.2V$) *1	76.8kHz	35	60	μA
		LCD power ON	153.6kHz	65	100	μA
		During execution	32.768kHz	6	10	μA
		Halver mode ($V_{DD}=3.0V$) *1	76.8kHz	10	18	μA
		LCD power ON	153.6kHz	20	35	μA

*1: No panel load. The SVD circuit is OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $C_G=25pF$, C_D =built-in, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	$t_{sta} \leq 3sec$ (V_{DD})	1.1			V
Oscillation stop voltage	V _{stp}	$t_{stp} \leq 10sec$ (Normal mode)	1.1			V
		(V_{DD}) (Doubler mode)	0.9			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC (in chip)		14		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{DD}=0.9$ to $3.6V$ with VDC switching			10	ppm
		without VDC switching			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$ 32.768kHz	30	40		ppm
		76.8kHz	20	25		ppm
		153.6kHz	8	10		ppm
Harmonic oscillation start voltage	V _{hho}	$C_G=5pF$ (V_{DD})	3.6			V
Permitted leak resistance	R _{leak}	Between OSC1 and V_{DD} , V_{SS}	200			M Ω

OSC3 CR oscillation circuit

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $R_{CR}=40.2k\Omega$, $T_a=25^{\circ}C$)

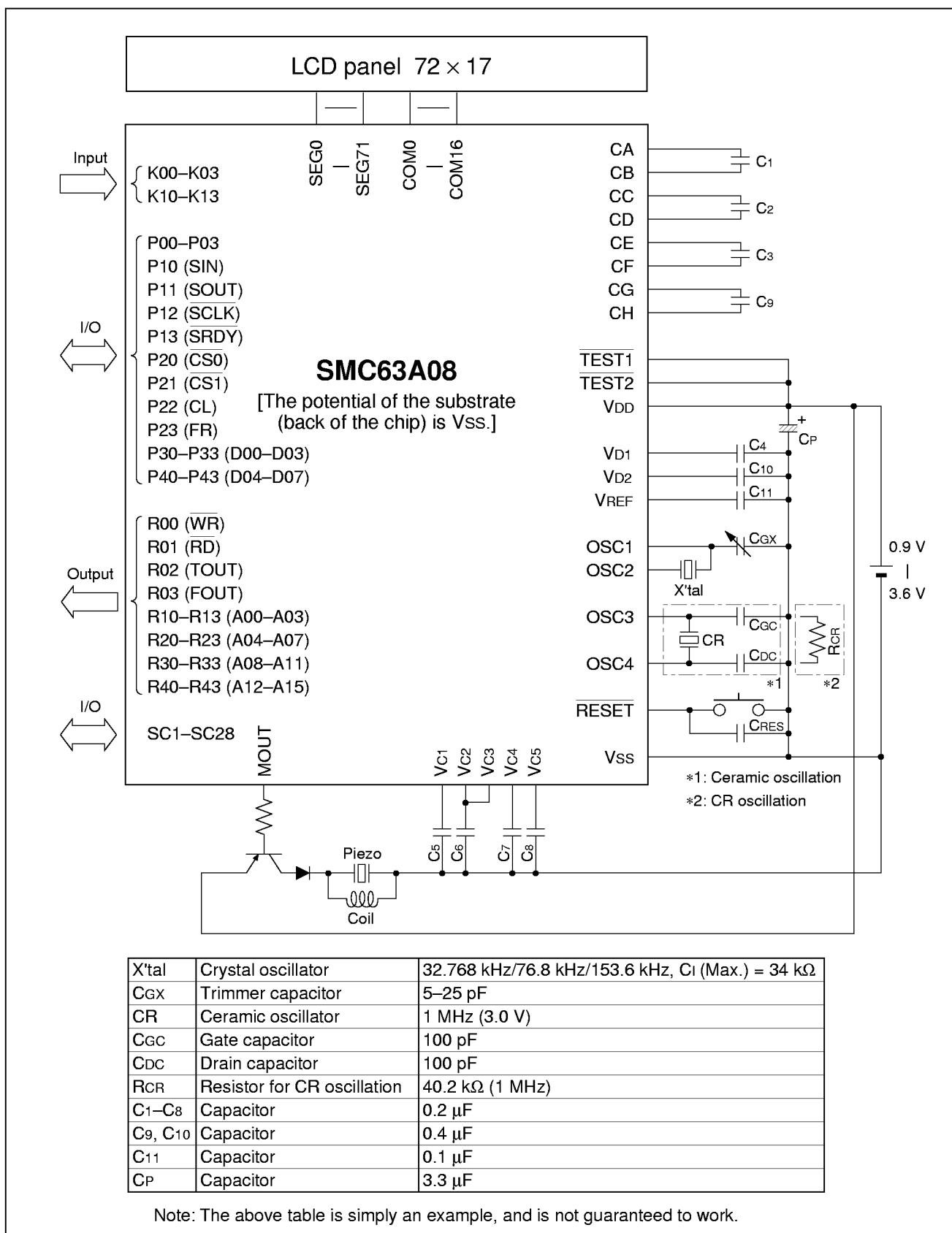
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f _{OSC3}		-30	900kHz	30	%
Oscillation start voltage	V _{sta}	Normal mode (V_{DD})	2.2			V
Oscillation start time	t _{sta}	$V_{DD}=2.2$ to $3.6V$			3	mS
Oscillation stop voltage	V _{stp}	Normal mode (V_{DD})	2.2			V

OSC3 ceramic oscillation circuit

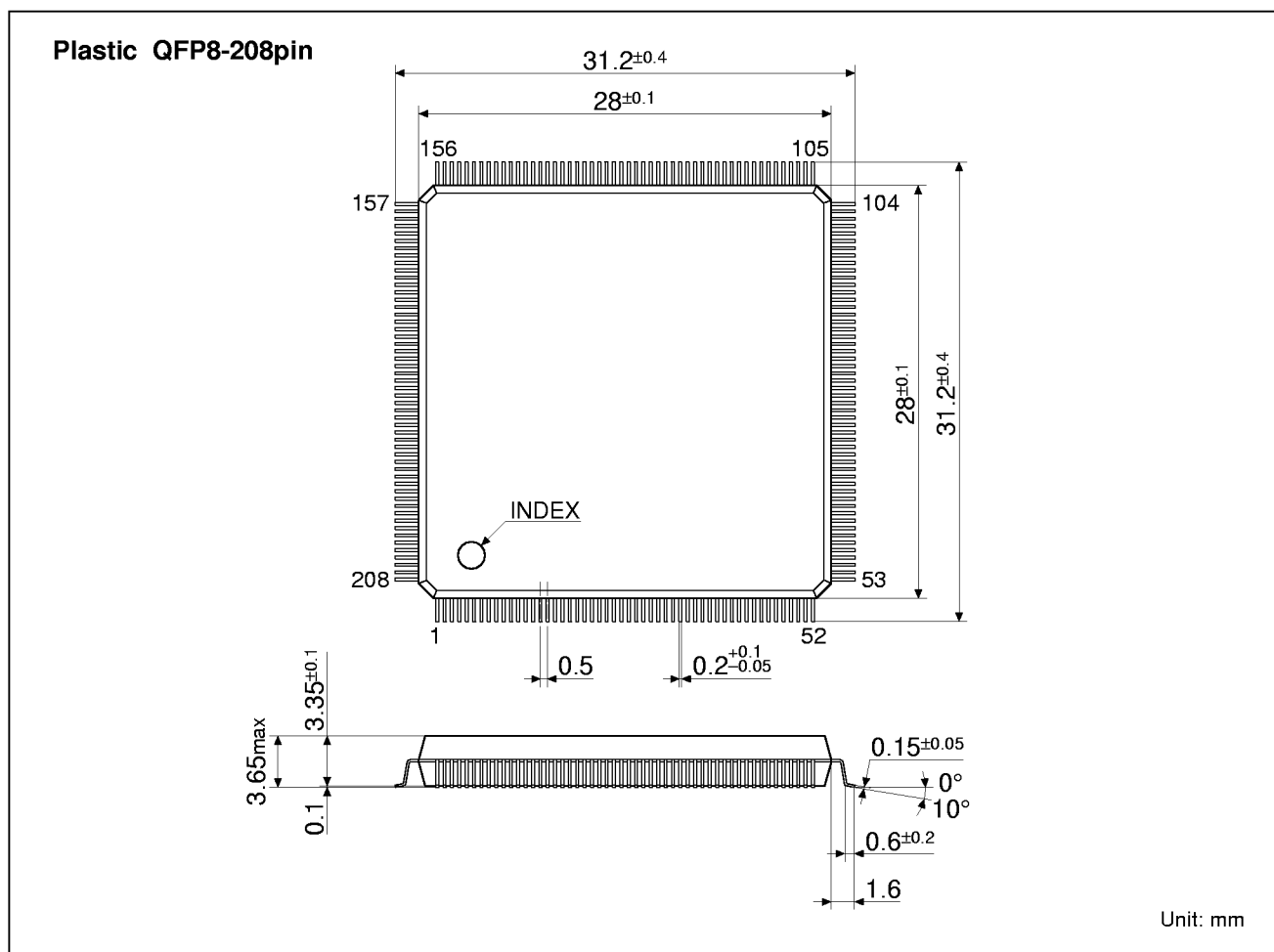
(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, Ceramic oscillation: 1MHz, $C_{GC}=C_{DC}=100pF$, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	Normal mode (V_{DD})	2.2			V
Oscillation start time	t _{sta}	$V_{DD}=2.2$ to $3.6V$			5	mS
Oscillation stop voltage	V _{stp}	Normal mode (V_{DD})	2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



■ PACKAGE DIMENSIONS



NOTICE:

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First issue Sep. 1995
Printed Jan. 1997 in Japan (M)