F72603R

Fintek ACPI Controller IC Datasheet

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F72603R Datasheet Revision History

Version	Date	Page	Revision History
0.1	Jan.2003		Original version
0.2	Feb.2003		Revise register description
0.33	Aprl.2003		Revise vendor ID and I2C ADDR can be programmable
0.34	July.2003		Revise some description
0.36	Apr 2004		Revise (1) Register index 01 initial value :from 1F to 03 (2) Version ID index5C : from 10 to 12

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1. General Description

The F72603R is a fully compliant ACPI controller IC. Used with an ATX power supply, this chip integrates one linear controller, four switch controller, monitoring and power signal control function into 28 pin SSOP package. The F72603R not only provides one adjustable linear regulator and four switch controllers but also integrates a charge pump engine to provide higher driving voltage for appropriate gate during standby. It also integrates Power OK and Reset signal circuit. On the other hand, this chip offers current limiting that protect each output, and provides soft-start function for linear regulator to avoid rush current. The power LED and suspend LED are programmable and compliant with PC2001. This chip is in VSB 5V operation and 28pin SSOP package.

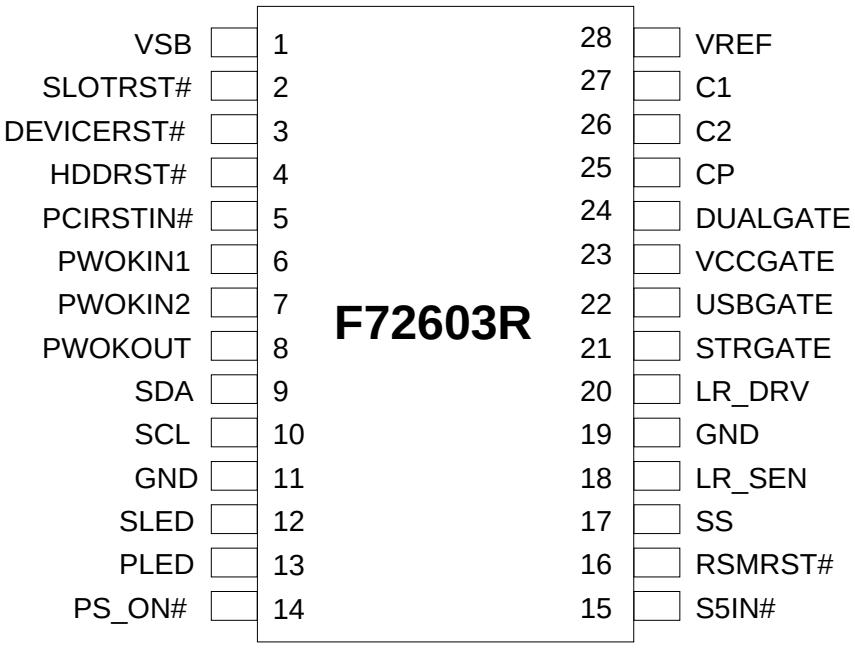
2. Features

- Support 1 adjustable linear regulator
- Provide 4 switch signal for power control
- 2 PWROK input signals(typically from ATX_PWGD & HWRSTIN) and 1 PWROK output signal
- Resume reset signal output
- 1 input reset signal to 3 output reset signals buffer
- Programmable power dual LED compliant with PC2001
- Power up soft-start(SS) for linear regulator
- Provide adjustable 1.25V reference voltage(V_{REF})
- Provide VSB 9V voltage(Charge Pump) for generating different kind of voltage
- 2-wire serial interface
- 28 pin SSOP package & VSB 5V operation

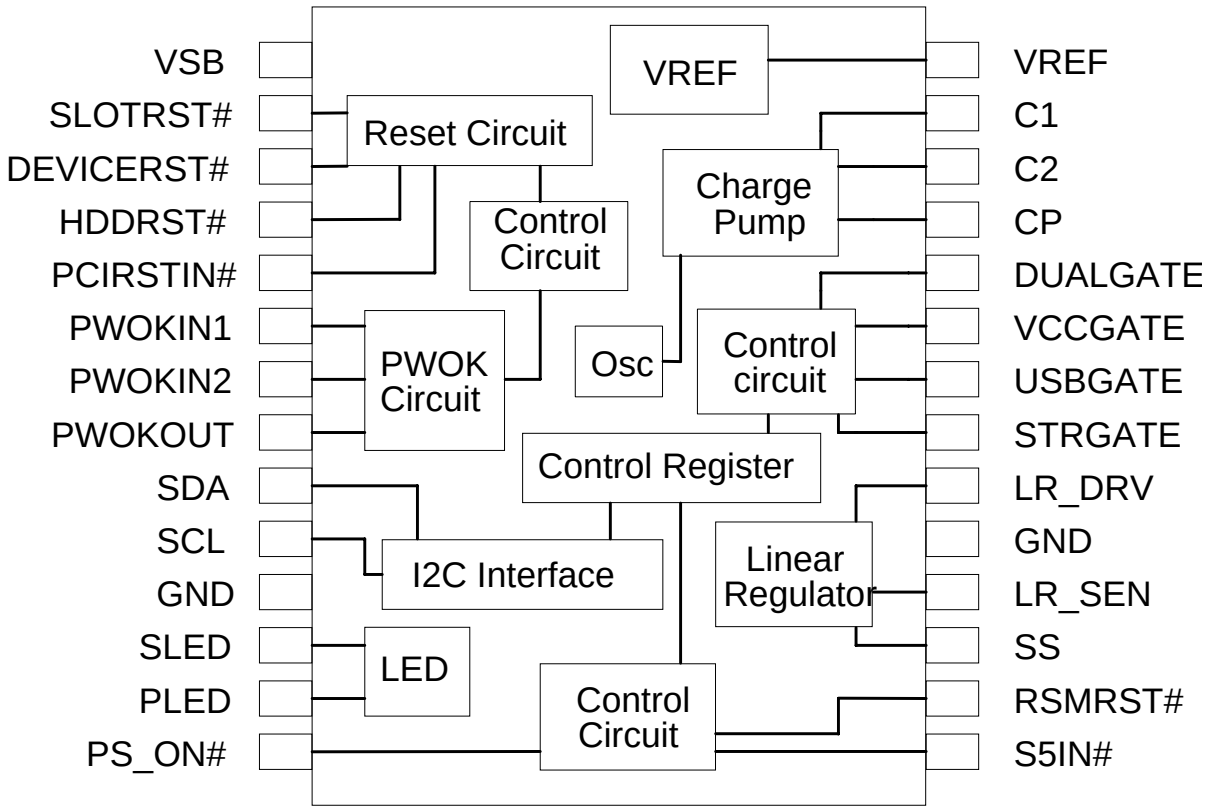
3. Key Specifications

- Supply Voltage 4.5V to 5.5V

4. Pin Configuration



5. Block Diagram



6. Pin Descriptions

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12ts} - TTL level and schmitt trigger

O_{12} - Output pin with 12 mA source-sink capability

O_{24V4} - Output pin with 24 mA source-sink capability, output 4V

AOUT - Output pin(Analog)

OD_{12} - Open-drain output pin with 12 mA sink capability

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

6.1 Power pins

PIN NO	PIN NAME	TYPE	DESCRIPTION
1	VSB	PWR	Power pins
11	GND		
19	GND		

6.2 Reset & Power Good signal pins

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
2	SLOTRST#	O_{24V4}	VSB5V	SLOT_RST # is an **active low** signal and act as “1 to 3” buffer **output.**
3	DEVICERST#	OD_{24}	VSB5V	DEVICERST# is an **active low** signal and acts as “1 to 3” buffer **output**. Open Drain output.
4	HDDRST#	OD_{24}	VSB5V	HDDRST# is an **active low** signal and acts as “1 to 3” buffer **output**.
5	PCIRSTIN#	IN_{ts}	VSB5V	PCIRST# is an **active low** signal and acts as “1 to 3” buffer **input**.
6	PWOKIN1	IN_{ts}	VSB5V	Power Good Schmitt trigger input
7	PWOKIN2	IN_{ts}	VSB5V	Power Good Schmitt trigger input
8	PWOKOUT	OD_{16}	VSB5V	Power Good Schmitt trigger output
16	RSMRST#	OD_{12}	VSB5V	RSMRST# output is an **active low** signal(delay 66ms)

6.3 Linear & Switch Controller

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
21	STRGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET
22	USBGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET
23	VCCGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET
24	DUALGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET
18	LR_SEN	AIN	VSB5V	Sense the voltage of linear regulator
20	LR_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET

6.4 Charge Pump

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
25	CHRPMP	P	VSB9V	Charge pump output (9V nominal). Decouple this pin with 1uF ceramic capacitor
26	C2	AIN	VSB9V	Positive end of charge pump capacitor
27	C1	AOUT	VSB9V	Negative end of charge pump capacitor. Connect a 1uF ceramic capacitor between pin27 (-) and pin26(+)

6.5 Power LED

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
12	SLED	OD_{24}	VSB5V	Suspend LED. Can be programmed by setting register
13	PLED	OD_{24}	VSB5V	Power LED. Can be programmed by setting register

6.6 Control Signal and Others

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
9	SDA	I/OD_{12}	VSB5V	2-wire serial bus data. Leakage free.
10	SCL	IN_{ts}	VSB5V	2-wire serial bus clock. Leakage free.
14	PS_ON#	IN_{ts}	VSB5V	Schmitt trigger input. Connect to ATX power. While connecting an inverter between this pin and ATX power, this pin will act as S3# input.
15	S5IN#	IN_{ts}	VSB5V	ACPI control signal governing the Soft Off state S5(Low active)
17	SS	AIN	VSB5V	Soft-Start. Connect this pin to a small ceramic capacitor to determine the soft-start rate. The value of capacitor is bigger, the slew rate is slower.
28	VREF	AOUT	VSB5V	Provide 1.25V reference voltage. As for VREF over-voltage, please refer to register description (Index 05h)

7. Functional Description

7.1 ACPI state

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state and in this state, the computer is being actively used. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state the processor is powered down but the last state is being stored in memory which is still active. S5 is a state that memory is off and the last state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state. But the disk is slower than the memory, the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen: S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5. Among them, S5→S3 is illegal transition and won't be allowed by state machine. In order to get to S5 from S3, it is necessary to enter S0 first. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

7.2 Charge pump

The F72603R incorporated with an embedded charge pump to provide higher driving voltage. Pin 22(CP) supports 10mA driving current and ensures 9V output voltage or above. In main operation, the VSB9V signals of F72603R are run from the +12V supplied by ATX power which also supplies to other MOSFET gates. However, during standby state, the +12V will be off and it needs to provide power to the chip and the appropriate gates. Therefore F72603R incorporated with a free running charge pump. As shown in schematic, there is a capacitor connected between pin 23 and 24 of the F72603R acts as a charge pump with internal diodes. The 12V input must has a serial diode to prevent back-feeding the charge pump to the +12V main when in standby. It also needs a bypass capacitor connected with 12V input line to filter high-frequency noise.

7.3 Soft-start

Pin27 of the F72603R acts as a soft-start. As shown in schematic, a ceramic capacitor is attached between this pin and ground. When power is first applied to the chip, a constant current is applied from the pin into an external capacitor, linearly ramping up the voltage. This ramp in turn controls the internal reference of F72603R providing a soft-start for linear regulator. As for switches, they must be either on or off in the system therefore soft-start has no effect on them. It is important to know soft-start is not an enable signal; pulling it low will not be sure to turn off all outputs. But if there are appropriate signals asserted, the switches will be turn on at once. The actual state of F72603R on power up will be determined by the controlled input signal. And the soft-start is effective only during power on. During a transition between states (not during power on), such as S3 to S0, the linear regulators won't be asserted.

7.5 Reference voltage

The pin28 (VREF) is an output pin that is driven by a small output buffer to provide the 1.25V reference voltage to other devices in the system.

7.6 Access Interface

The F72603R can be connected to a compatible 2-wire serial system Management Bus as a slave device under the control of the master device, using two device terminals SCL and SDA. The F72603R can provide a clock signal to the device SCL pin and read/write data from/to the device through the device SDA pin. The operation of device to the bus is described with details in the following sections.

(a) SMBus write to internal address register followed by the data byte

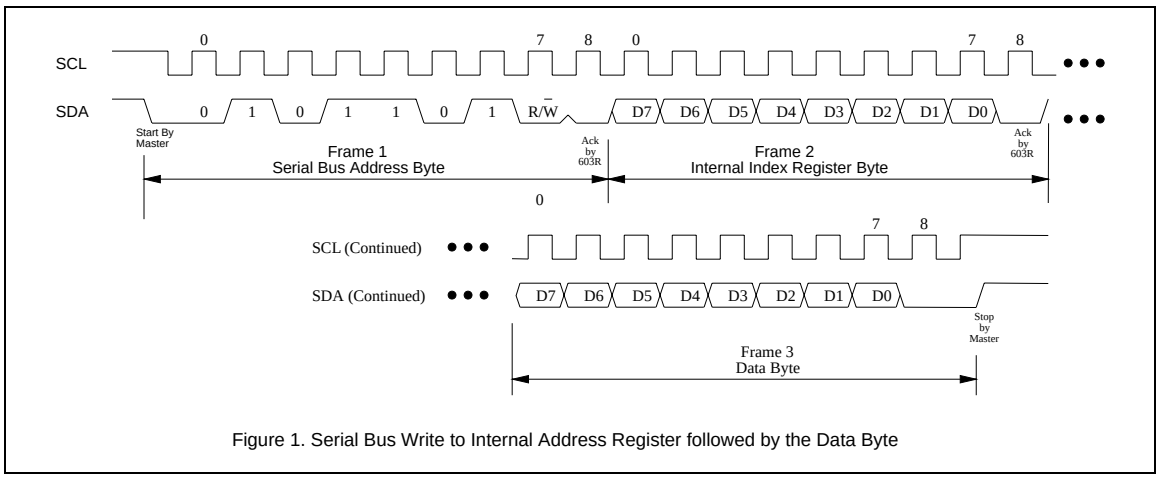


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

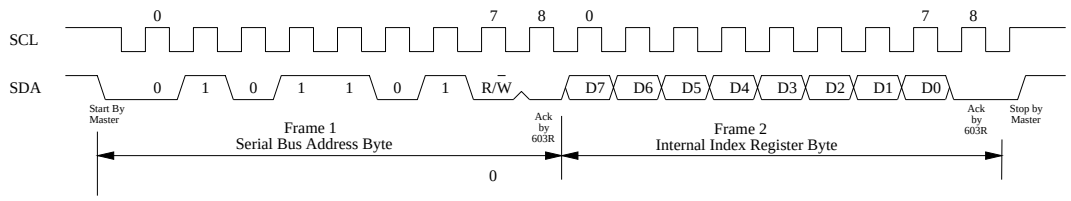


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

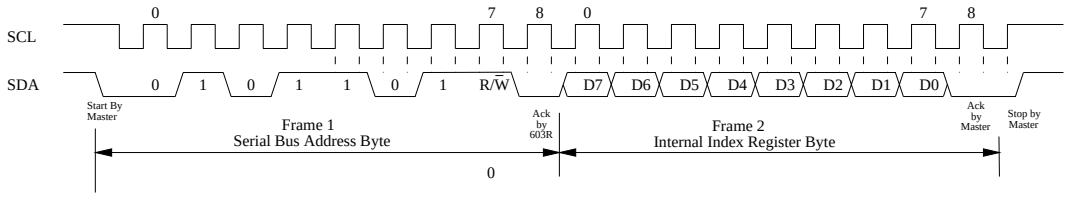


Figure 3. Serial Bus Read from Internal Address Register

8. Registers Description

8.1 PCIRST_N delay function Register, Default 0x03h — Index 01h

Bit	Name	PWD	Description
7	SLOT_SOFTRST	0	SLOTRST_N Software reset, when set to 1, it will produce one low pulse signal to SLOTRST_N, and the pulse width is set by Register0 [1:0] (after Reset, the bit will clean to 0)
6	DEV_SOFTRST	0	DEVICERST_N Software reset, when set to 1, it will produce one low pulse signal to DEVICERST_N, and the pulse width is set by Register0 [1:0] (after Reset, the bit will clean to 0)
5	HDD_SOFTRST	0	HDDRST_N Software reset, when set to 1, it will produce one low pulse signal to HDDRST_N, and the pulse width is set by Register0 [1:0] (after Reset, the bit will clean to 0)
4	SLOT_DELAY_EN	0	Enable the delay function of SLOTRST_N from PCIRST_N, default = 0, if set to 1, the delay function is enable, the delay time is set by Register0 [1:0]
3	DEV_DELAY_EN	0	Enable the delay function of DEVICERST_N from PCIRST_N, default = 0, if set to 1, the delay function is enable, the delay time is set by Register0 [1:0]
2	HDD_DELAY_EN	0	Enable the delay function of HDDRST_N from PCIRST_N, default = 0, if set to 1, the delay function is enable, the delay time is set by Register0 [1:0]
1	DELAY[1]	1	The SLOTRST_N and DEVICERST_N and HDDRST_N signals are delayed from PCIRST_N by followed setting 00 1ms 01 2ms 10 3ms 11 4ms
0	DELAY[0]	1	

8.2 PWOKOUT delay function Register, Default 0x07h — Index 02h

Bit	Name	PWD	Description

7	PWOK_SOFTRST	0	PWOKOUT Software reset, set to 1, it will produce one low pulse signal to PWOKOUT, and the pulse width is set by Register 01 [1:0] (after Reset, the bit will clean to 0)
6	Reserved	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	PWOK_DELAY_EN	1	Enable the delay function of PWOKOUT from PWOKIN(*1), default = 0, if set to 1, the delay function is enable, the delay time is set by Register1 [1:0]
1	DELAY[1]	1	The PWOKOUT signals are delayed from PWOKIN(*1) by followed setting
0	DELAY[0]	1	00 100ms 01 200ms 10 300ms 11 400ms

*1 PWOKIN = PWOKIN1 & PWOKIN2

8.3 PLED Register, Default 0x00h— Index 03h

Bit	*Name*	*PWD*	*Description*
7	PROG_EN	0	Set to 1 to enable program PLED and SLED frequency, set to 0 to hardware setting
6	PLED_FREQ[2]	0	111 : LED pin is tri-state (OD pin) or drived high (O pin) 110 : LED pin is 1 Hz toggle pulse with 50 duty cycle 101 : LED pin is 1/2 Hz toggle pulse with 50 duty cycle 100 : LED pin is 1/4 Hz toggle pulse with 50 duty cycle 000 : LED pin Is drived low
5	PLED_FREQ[1]	0	
4	PLED_FREQ[0]	0	
3	LED_MODE	0	PLED_MODE select
2	SLED_FREQ[2]	0	111 : LED pin is tri-state (OD pin) or drived high (O pin) 110 : LED pin is 1 Hz toggle pulse with 50 duty cycle 101 : LED pin is 1/2 Hz toggle pulse with 50 duty cycle 100 : LED pin is 1/4 Hz toggle pulse with 50 duty cycle 000 : LED pin Is drived low
1	SLED_FREQ[1]	0	
0	SLED_FREQ[0]		

8.4 DUALGAT, USBGAT, LR_DRV mode select Register, Default 0x12h— Index 04h

Bit	Name	PWD	Description
7	DUAL_MODE[1]	0	DUALGAT mode control, default mode is dual mode, 00: Dual mode, 01: STR mode, 10: Power off, 11: reserved
6	DUAL_MODE[0]	0	
5	USB_MODE[1]	0	USBGAT mode control, default mode is STR mode, 00: Dual mode, 01: STR mode, 10: Power off, 11: reserved
4	USB_MODE[0]	1	
3	LR_MODE[1]	0	Linear regulator mode control, default mode is dual mode, 00: Dual mode, 01: STR mode, 10: Power off, 11: reserved
2	LR_MODE[0]	0	
1	MODE	1	MODE=0, Linear regulator is used 1 MOS, MODE=1, is used 2 MOS
0	Reserved	0	

* The DUALGAT and USBGAT and LR must switch with VCCGAT

8.5 Over-voltage Configuration Register for VREF and LR regulator Default 0x08h — Index 05h

Bit	Name	PWD	Description
7	EN_VREF	0	Set to 1 Enable to increase VREF, the increase percentage is set by bit[6:5]; Set to 0 will not increase the percentage of VREF
6	OV_VREF[1]	0	VREF Over voltage percentage 00 1% 01 2% 10 3% 11 4%
5	OV_VREF[0]	0	
4	UV_EN	0	Set to 1 to enable under voltage protect, when the LR_SEN is below 1.0V, the under voltage event occurs, if UV_EN is set to 1, it will SD the linear regulator.
3	VSB_PWR_LOSS	1	When VSB 5V comes, it will set to 1, and write 1 to clear it
2	UV_SEL	0	UV_SEL : 0 the Under-voltage protect time is from PWOK is high UV_SEL : 1 the Under-voltage protect time is from SS_OK
1	Reserved	0	Reserved
0	Reserved	0	Reserved

8.6 Chip ID High Byte, Default 0x03h, Read Only — Index 5Ah

8.7 Chip ID Low Byte, Default 0x02h, Read Only — Index 5Bh

8.8 Version ID, Default 0x12h, Read Only — Index 5Ch

8.9 Vendor ID, Default 0x19h, Read Only— Index 5Dh

8.10 Vendor ID, Default 0x34h, Read Only — Index 5Eh

8.11 Vender ID, Default 0xA0h, Read Only — Index 6Ah(For Aopen use only)

8.12 Vender ID, Default 0xA0h, Read Only — Index 6Bh(For Aopen use only)

8.13 Register F0 (Test mode, Default 0x00h)

<table>
<tr><th>Bit</th><th>Name</th><th>PWD</th><th>Description</th></tr>
<tr><td>7</td><td>I2C_TEST</td><td>0</td><td>Set to 1 for I2C test, disable I2C 200ns filter</td></tr>
<tr><td>6</td><td>DIS_I2CTMOUT</td><td>0</td><td>Set to 1 for Disable I2CTIMOUT</td></tr>
<tr><td>5</td><td>TEST_CLK</td><td>0</td><td>Set to 1 for test internal clock 200K, It will generate a reset for internal
Counters which clocked by internal clock 200K</td></tr>
<tr><td>4</td><td>EN_CLKIN</td><td>0</td><td>Enable the test clock in</td></tr>
<tr><td>3</td><td>EN_CLKOUT</td><td>0</td><td>Enable the CLKOUT output to pin</td></tr>
<tr><td>2</td><td>CLKOUT_SEL[2]</td><td>0</td><td rowspan="3">The CLKOUT selection table
<table>
<tr><td>000</td><td>200K</td></tr>
<tr><td>001</td><td>CLK_1K</td></tr>
<tr><td>010</td><td>CLK_1HZ</td></tr>
<tr><td>011</td><td>0.5Hz</td></tr>
<tr><td>100</td><td>0.25Hz</td></tr>
<tr><td>101</td><td>200K/256(TCLK_OUT)</td></tr>
<tr><td>110</td><td>1</td></tr>
<tr><td>111</td><td>0</td></tr>
</table></td></tr>
<tr><td>1</td><td>CLKOUT_SEL[1]</td><td>0</td></tr>
<tr><td>0</td><td>CLKOUT_SEL[0]</td><td>0</td></tr>
</table>

8.14 Register F1 (Test mode, Default 0x00h)

Bit	Name	PWD	Description
7	COUNT OK	0	Read only, to read test clock which is internal 200K clock divided by 256
6	SPEED_UP	0	When set to 1, and EN_CLKIN = 1, it will speed up the CLK_2KHz and CLK_20Hz to T_CLK
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	Reserved	0	Reserved

8.15 Regter FF (I2C ADDR program Defaultt 0x5Eh)

If write 8'hC9 to Register FE, that will enable I2C ADDR to be programmable

Bit	Name	PWD	Description
7	I2C_ADDR[7]	0	I2C_ADDR[7]
6	I2C_ADDR[6]	1	I2C_ADDR[6]
5	I2C_ADDR[5]	0	I2C_ADDR[5]
4	I2C_ADDR[4]	1	I2C_ADDR[4]
3	I2C_ADDR[3]	1	I2C_ADDR[3]
2	I2C_ADDR[2]	1	I2C_ADDR[2]
1	I2C_ADDR[1]	1	I2C_ADDR[1]
0	I2C_ADDR[0]	0	I2C_ADDR[0]

9. Electrical characteristic

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

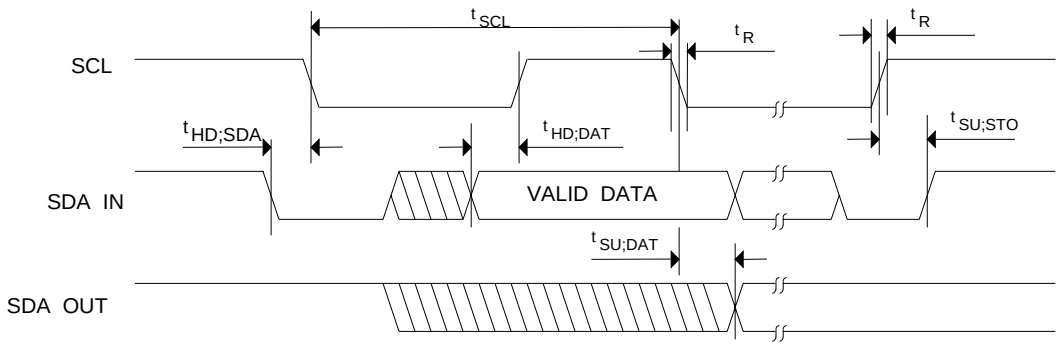
(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL	10	12		mA	VOL = 0.4V
Output High Current	IOH		-12	-10	mA	VOH = 2.4V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Output Low Current	IOL	10	12		mA	VOL = 0.4 V
Output High Current	IOH		-12	-10	mA	VOH = 2.4V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V

9.2 DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Current	IOL	12	16		mA	VOL = 0.4V
Output High Current	IOH		-14	-12	mA	VOH = 2.4V
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Current	IOL	6	8		mA	VOL = 0.4V
OD_{16} - Open-drain output pin with sink capability of 16 mA						
Output Low Current	IOL	12	16		mA	VOL = 0.4V
I/OOD_{16ts} - TTL level bi-directional pin, can select to OD or OUT by register, with 16 mA source-sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Output Low Current	IOL	6	8		mA	VOL = 0.4 V
Output High Current	IOH		-16	-12	mA	VOH = 2.4V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V
IN_t - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

9.3 AC Characteristics



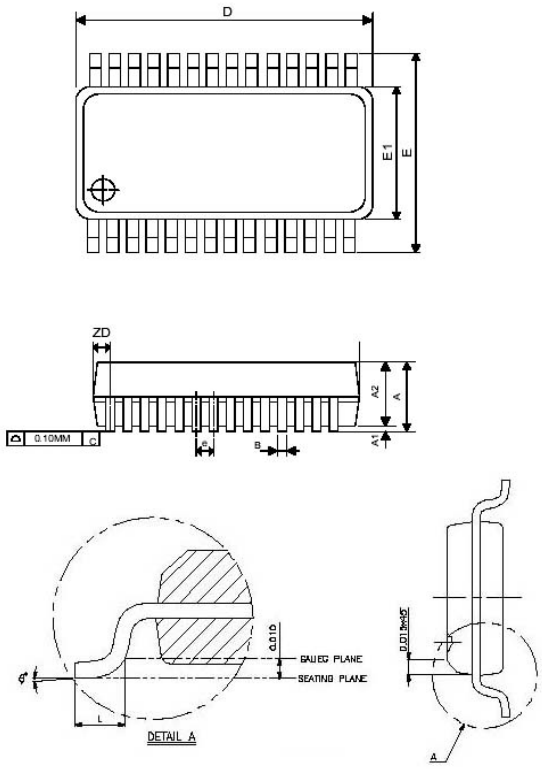
Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

10. Package specification

28-pin SSOP(150mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			0.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
H	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF		
θ	0^0		8^0	0^0		8^0

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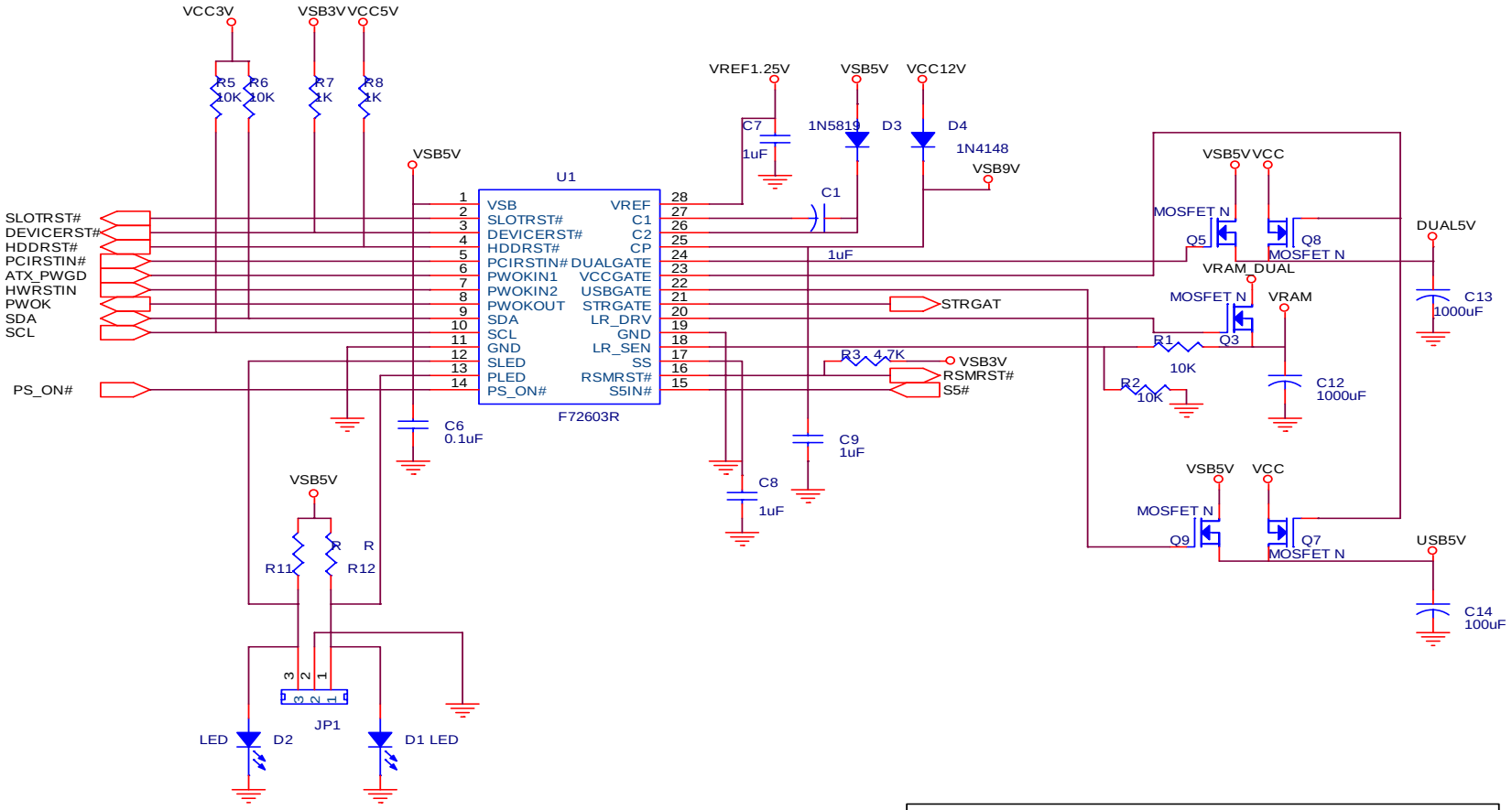
11 Application Circuit



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