High CMR Analog Isolation Amplifiers

Technical Data

HCPL-7820
HCPL-7825

Features

- **Fast Propagation Delays for Over-Current and Fault Detection Sensing**
- **High Common Mode Rejection (CMR): 30 kV/μs at V_{CM} = 1000 V***
- **3% Gain Tolerance: HCPL-7820**
  5% Gain Tolerance: HCPL-7825
- **0.05% Nonlinearity**
- **Low Offset Voltage and Offset Drift vs. Temperature**
- **200 kHz Bandwidth**
- **Performance Specified for Common Motor Control Applications over -40°C to 100°C Temperature Range**
- **Worldwide Safety and Regulatory Approval: UL 1577 (3750 V rms/1 Min), VDE 0884 and CSA**
- **Compact Auto-Insertable Standard 8-Pin DIP Package**
- **Advanced Sigma-Delta (ΣΔ) A/D Converter Technology**
- **1 μm CMOS IC Technology**

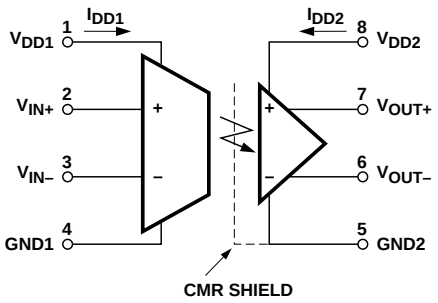
Applications

- **Motor Phase and Rail Current Sensing**
- **General Purpose Current Sensing and Monitoring**
- **High-Voltage Monitoring**
- **Switched Mode Power Supply Signal Isolation**
- **General Purpose Analog Signal Isolation**
- **Transducer Isolation**

Description

The HCPL-7820/7825 high CMR isolation amplifier consists of a sigma-delta analog-to-digital converter optically coupled to an integrated output digital-to-analog converter. When used with a shunt resistor in the current path, the HCPL-7820/7825 provides a cost-effective, auto-insertion compatible current sense solution. Fast propagation delays allow this part to be used in either motor drive or inverter applications for either phase current monitoring or rail current fault detection applications. High isolation mode rejection makes this product suitable for noisy electrical environments, such as those generated by the high switching rates of power IGBTs. Low offset voltage together with low offset change vs. temperature permits accurate use of auto-calibration techniques. Tight gain tolerance with good nonlinearity further provide the characteristics needed to insure highly accurate motor speed control. A high operating temperature range with specified performance parameters allow

Functional Diagram



A 0.1 μF bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

*The terms common-mode rejection (CMR) and isolation-mode rejection (IMR) are used interchangeably throughout this data sheet.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

this device to be used in hostile industrial environments. This performance is delivered in an auto-insertable, industry standard 8-pin DIP package that meets major worldwide regulatory and safety approval ratings to help ensure that your equipment can be certified in many geographic areas.

Ordering Information

HCPL-782x

- 0 = ± 3% Gain Tolerance
- 5 = ± 5% Gain Tolerance

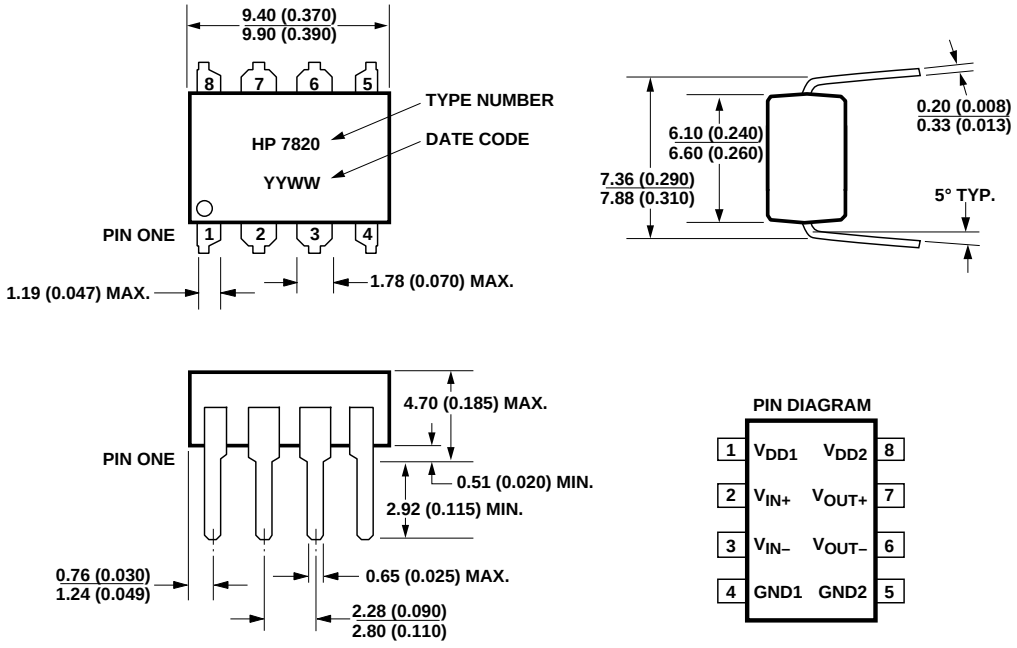
Option yyy

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option datasheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

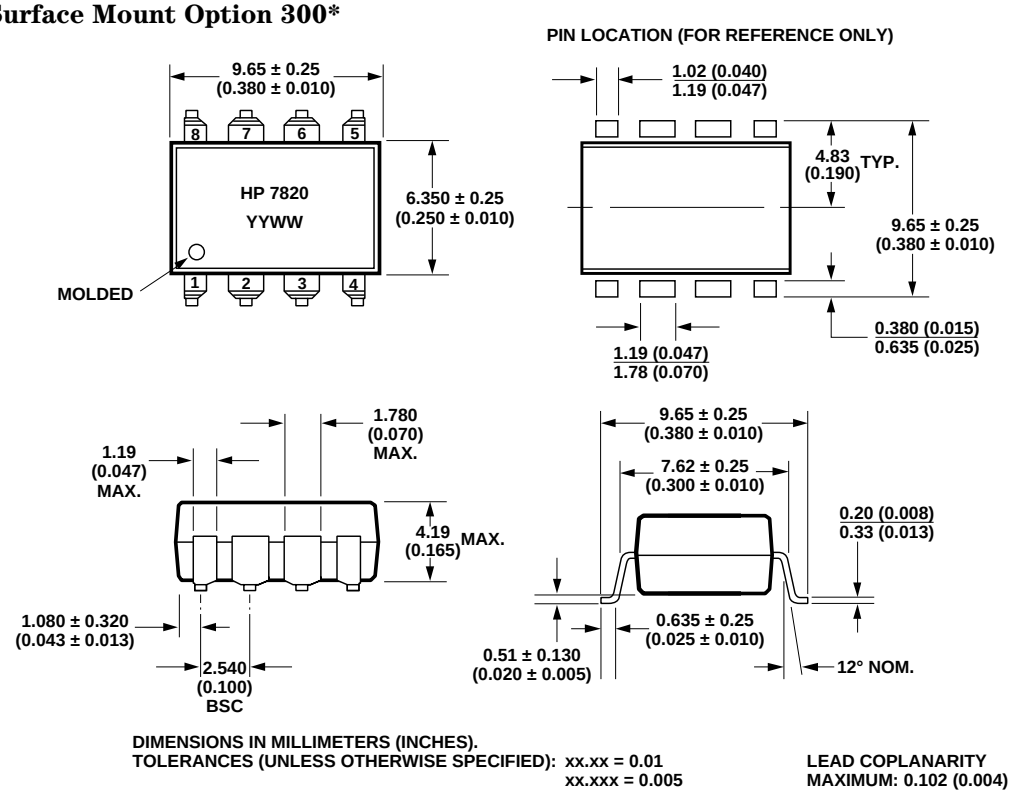
Package Outline Drawings

Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

Gull Wing Surface Mount Option 300*

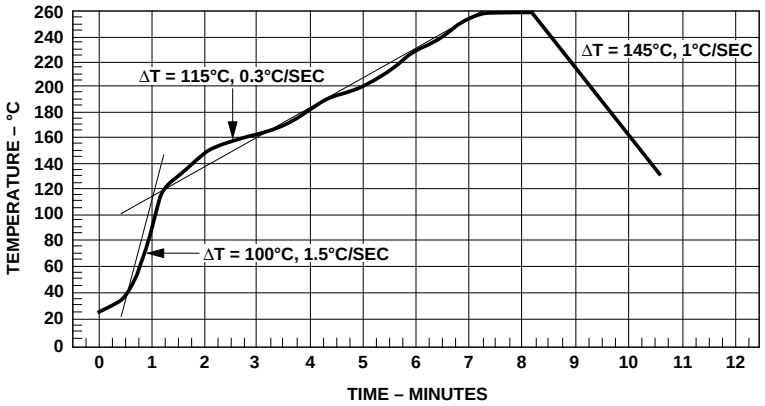


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

*Refer to Option 300 Data Sheet for more information.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7820/7825 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, FILE E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		III a		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** V_{PR} = 1.875 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** V_{PR} = 1.5 x V_{IORM}, Type and sample test with t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage t_{TR} = 10 sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 22) Case Temperature Input Power Output Power	 T_S $P_{S,Input}$ $P_{S,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 1 \times 10^{12}$	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section of the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	℃	
Ambient Operating Temperature	T_A	-40	100	℃	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5	V	
Two Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature (1.6 mm below seating plane, 10 sec.)	T_{LS}		260	℃	1
Reflow Temperature Profile	See **Package Outline Drawings** Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	100	℃	
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage	V_{IN+}, V_{IN-}	-200	200	mV	2

DC Electrical Specifications

All specifications are at the nominal (typical) operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-0.8	0.45	1.7	mV		1	3
		-2.0	0.45	2.9		-40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	1,2,3	
Absolute Value of Input Offset Change vs. Temperature	$\lvert\Delta V_{OS}/\Delta T\rvert$		7.8		µV/°C		1,2	3,4
Gain: HCPL-7820	G	7.76	8.00	8.24	V/V	-200 mV ≤ V_{IN+} ≤ 200 mV	5	
		7.60	8.00	8.40		-200 mV ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,6,7	
Gain: HCPL-7825	G	7.60	8.00	8.40	V/V	-200 mV ≤ V_{IN+} ≤ 200 mV	5	
		7.44	8.00	8.56		-200 mV ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,6,7	
200 mV Nonlinearity	NL_{200}		0.06	0.15	%	-200 mV ≤ V_{IN+} ≤ 200 mV	5,8	5
				0.3		-200 mV ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,8, 9,10, 12	
100 mV Nonlinearity	NL_{100}		0.03	0.08		-100 mV ≤ V_{IN+} ≤ 100 mV	5,8	
				0.1		-100 mV ≤ V_{IN+} ≤ 100 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,8, 9,11, 12	
Maximum Input Voltage Before Output Clipping	$\lvert V_{IN+}\rvert_{max}$		320		mV		4	
Average Input Bias Current	I_{IN}		-1		µA		13	6
Average Input Resistance	R_{IN}		280		kΩ			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		52		dB			
Output Resistance	R_O		1.2		Ω			
Output Low Voltage	V_{OL}		1.30		V	V_{IN+} = 400 mV	4	7
Output High Voltage	V_{OH}		3.90		V	V_{IN+} = -400 mV		
Output Common-Mode Voltage	V_{OCM}	2.30	2.60	2.90	V	-400 mV < V_{IN+} < 400 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V		
Input Supply Current	I_{DD1}		11.1	17.0	mA		14	
Output Supply Current	I_{DD2}		10.0	14.0	mA		15	
Output Short-Circuit Current	$\lvert I_{OSC}\rvert$		12		mA	V_{OUT} = 0 V or V_{DD2}		8

AC Electrical Specifications

All specifications and figures are at the nominal (typical) operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Isolation Mode Rejection	IMR	20	30		kV/μs	V_{IM} = 1 kV -40°C < T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	16	9
Isolation Mode Rejection Ratio at 60 Hz	IMRR		>140		dB			10
Propagation Delay to 50%	t_{PD50}	1.20	1.85	2.85	μs	V_{IN+} = 0 to 100 mV step -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	17,18	
Propagation Delay to 90%	t_{PD90}	1.60	2.75	4.10				
Rise/Fall Time (10-90%)	$t_{R/F}$	0.85	1.50	2.25				
Small-Signal Bandwidth (-3 dB)	f_{-3dB}	150	200	380	kHz	-40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	17,19, 20	
Small-Signal Bandwidth (-45°)	$f_{-45°}$		85					
RMS Input-Referred Noise	V_N		1.4		mV rms	In recommended application circuit	21,24	11
Power Supply Rejection	PSR		150		mV p-p			12

Package Characteristics

All specifications and figures are at the nominal (typical) operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH ≤ 50%			13,14
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C	V_{I-O} = 500 Vdc		13
		10^{11}				T_A = 100°C			
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz			
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W	Thermocouple located at center underside of package			
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W				

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. HP recommends the use of non-chlorine activated fluxes.
2. If V_{IN-} is brought above V_{DD1}-2 V with respect to GND1 an internal test mode may be activated. This test mode is not intended for customer use.
3. Exact offset value is dependent on layout of external bypass capacitors. The offset value in the data sheet corresponds to HP's recommended layout (see Figures 26 and 27).
4. Data sheet value is the average magnitude of the difference in offset voltage from T_A = 25°C to T_A = 100°C, expressed in microvolts per °C.
5. Nonlinearity is defined as half of the peak-to-peak deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.
6. Because of the switched-capacitor nature of the input sigma-delta A/D converter, time-averaged values are shown.
7. When the differential input signal exceeds approximately 320 mV, the outputs will limit at the typical values shown.
8. Short-circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
9. IMR (also known as CMR or Common Mode Rejection) specifies the minimum rate of rise of an isolation mode noise signal at which small output perturbations begin to appear. These output perturbations can occur with both the rising and falling edges of the isolation mode waveform and may be of either polarity. A CMR failure is defined as a perturbation exceeding 200 mV at the output of the recommended application circuit (Figure 24). See applications section for more information on CMR.
10. IMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 2 and 3) to the isolation mode gain (input pins tied to pin 4 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.
11. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 500 kHz) and is not attenuated by the on-chip output filter. The on-chip filter does eliminate most, but not all, of the sigma-delta quantization noise. An external filter circuit may be easily added to the external post-amplifier to reduce the total RMS output noise. See applications section for more information.
12. Data sheet value is the amplitude of the transient at the differential output of the HCPL-7820/7825 when a 1 V_{p-p}, 1 MHz square wave with 200 ns rise and fall times (measured at pins 1 and 8) is applied to both V_{DD1} and V_{DD2}.
13. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.
14. In accordance with UL 1577, for devices with minimum V_{ISO} specified at 3750 V rms, each optocoupler is proof-tested by applying an insulation test voltage greater than 4500 V rms for one second (leakage current detection limit I_{I-O} < 5 μA). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.

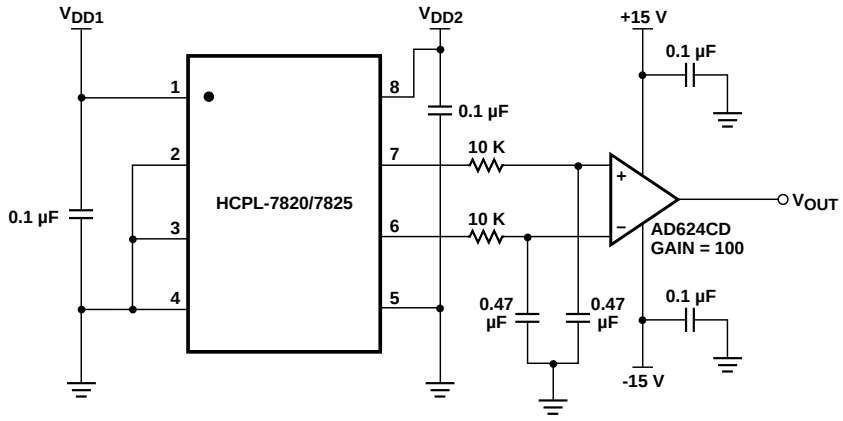


Figure 1. Input Offset Voltage Test Circuit.

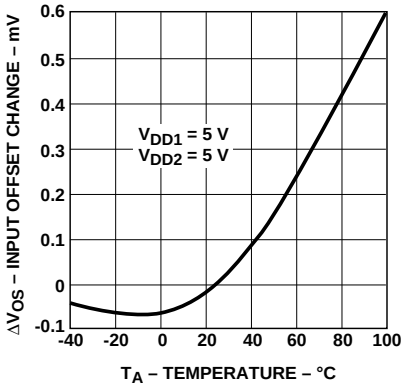


Figure 2. Input Offset Change vs. Temperature.

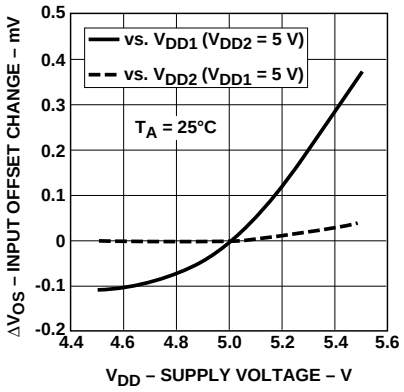


Figure 3. Input Offset Change vs. V_{DD1} and V_{DD2}.

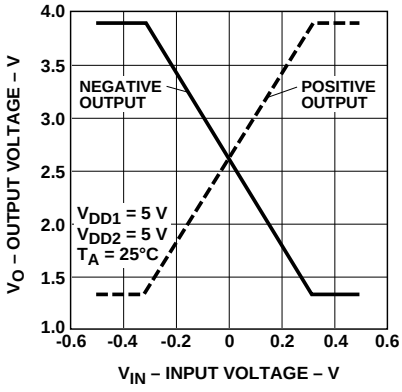


Figure 4. Output Voltages vs. Input Voltage.

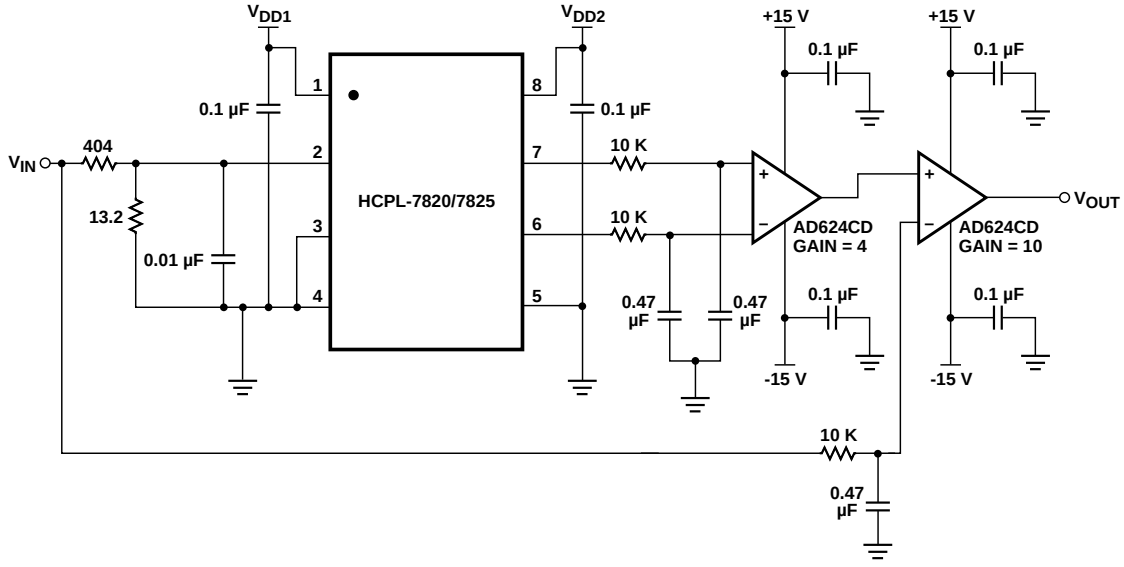


Figure 5. Gain and Nonlinearity Test Circuit.

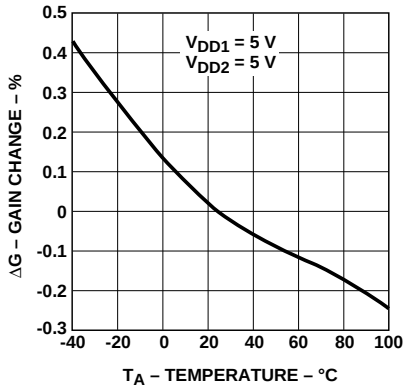


Figure 6. Gain Change vs. Temperature.

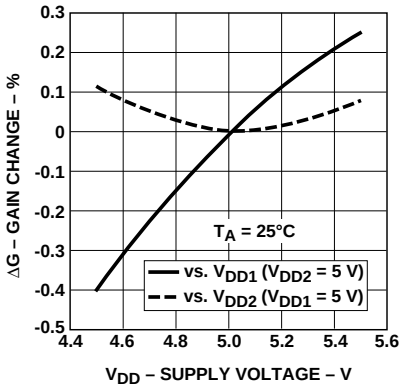


Figure 7. Gain Change vs. V_{DD1} and V_{DD2}.

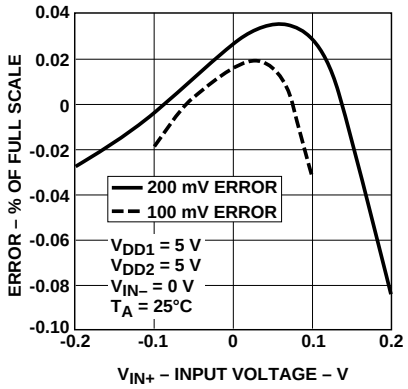


Figure 8. Nonlinearity Error Plot vs. Input Voltage.

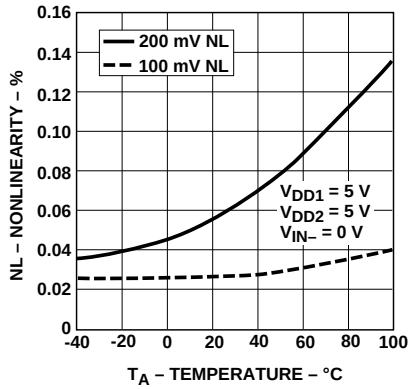


Figure 9. Nonlinearity vs. Temperature.

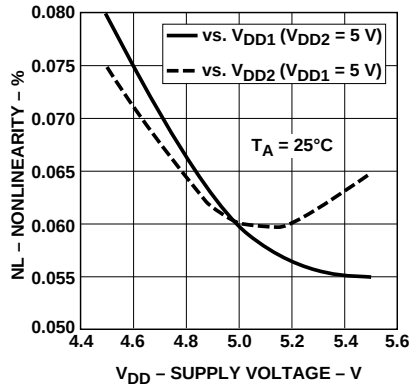


Figure 10. 200 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

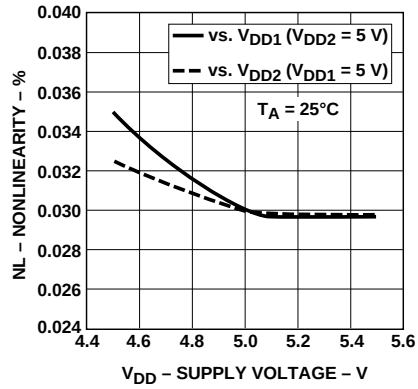


Figure 11. 100 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

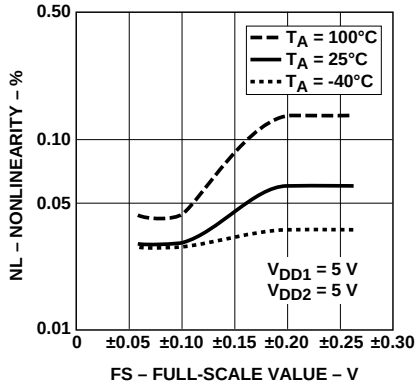


Figure 12. Nonlinearity vs. Full-Scale Value.

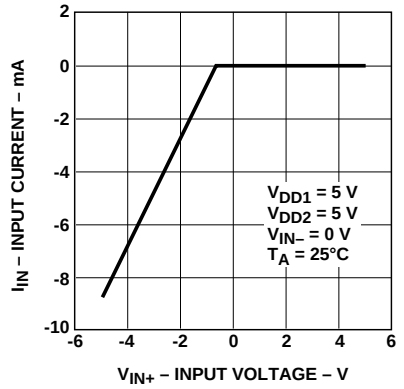


Figure 13. Input Current vs. Input Voltage.

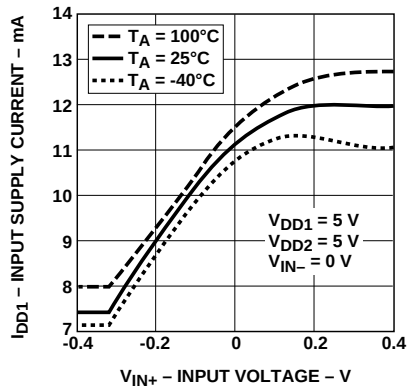


Figure 14. Input Supply Current vs. Input Voltage.

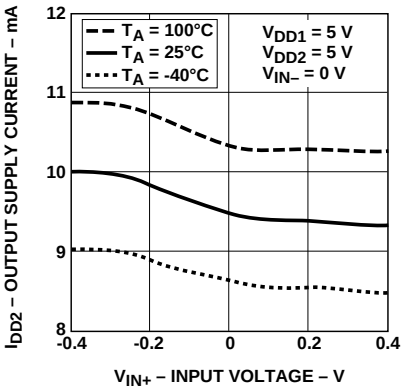


Figure 15. Output Supply Current vs. Input Voltage.

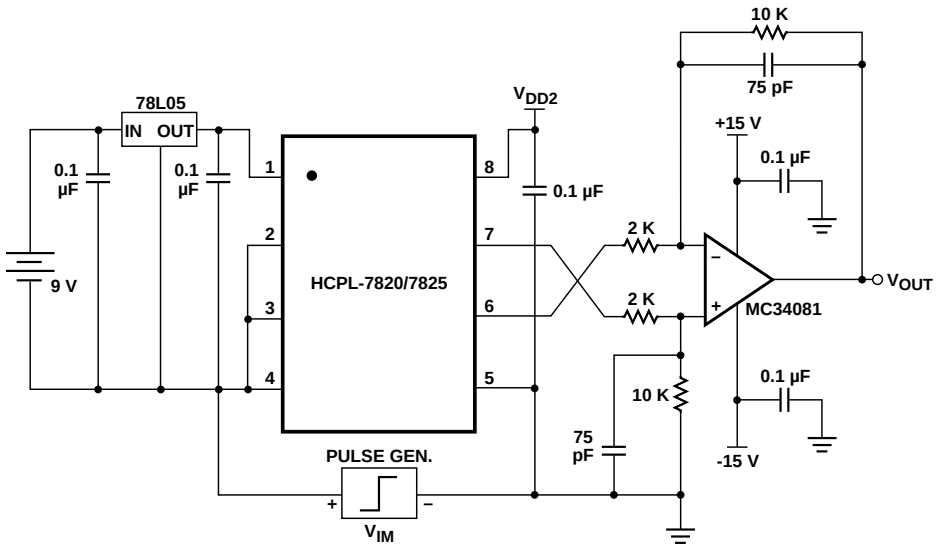


Figure 16. Isolation Mode Rejection Test Circuit.

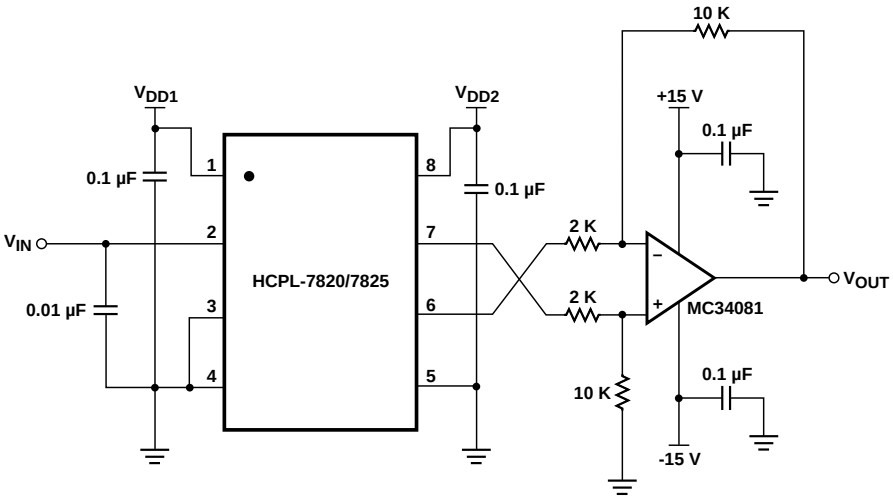


Figure 17. Propagation Delay, Rise/Fall Time and Bandwidth Test Circuit.

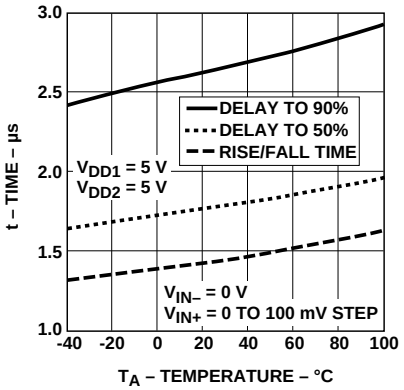


Figure 18. Propagation Delays and Rise/Fall Time vs. Temperature.

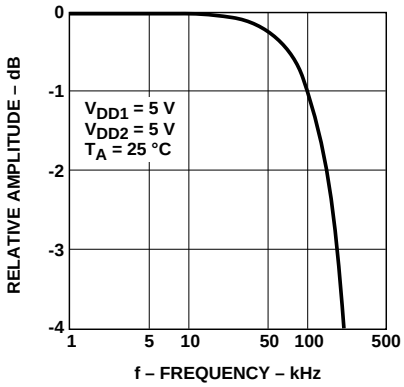


Figure 19. Amplitude Response vs. Frequency.

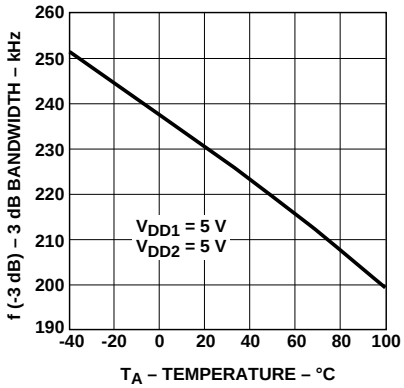


Figure 20. 3 dB Bandwidth vs. Temperature.

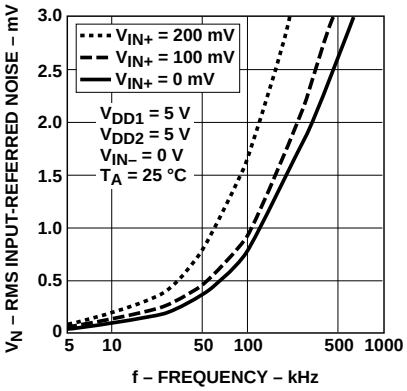


Figure 21. RMS Input-Referred Noise vs. Recommended Application Circuit Bandwidth.

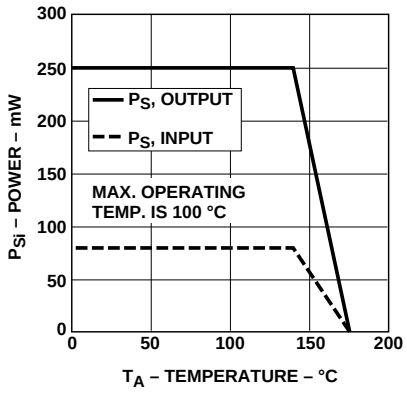


Figure 22. Dependence of Safety-Limiting Values on Temperature.

Applications Information

Functional Description

Figure 23 shows the primary functional blocks of the HCPL-7820/7825. In operation, the sigma-delta modulator converts the analog input signal into a high-speed serial bit stream. The time average of this bit stream is directly proportional to the input signal. This stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted back into an analog signal, which is filtered to obtain the final output signal.

Application Circuit

The recommended application circuit is shown in Figure 24. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator (U1). The voltage from the current sensing resistor, or shunt (R_{SENSE}), is applied to the input of

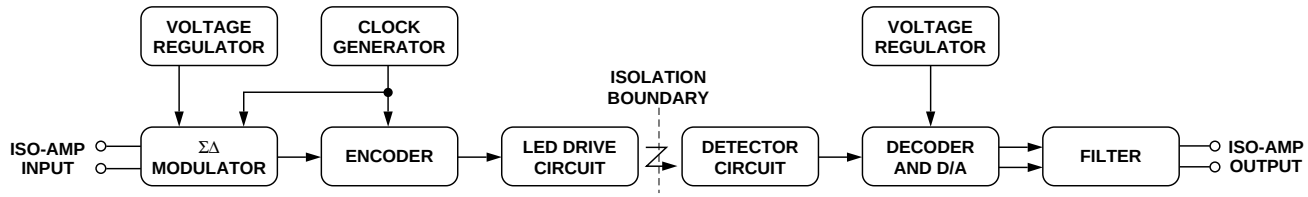


Figure 23. HCPL-7820/7825 Block Diagram.

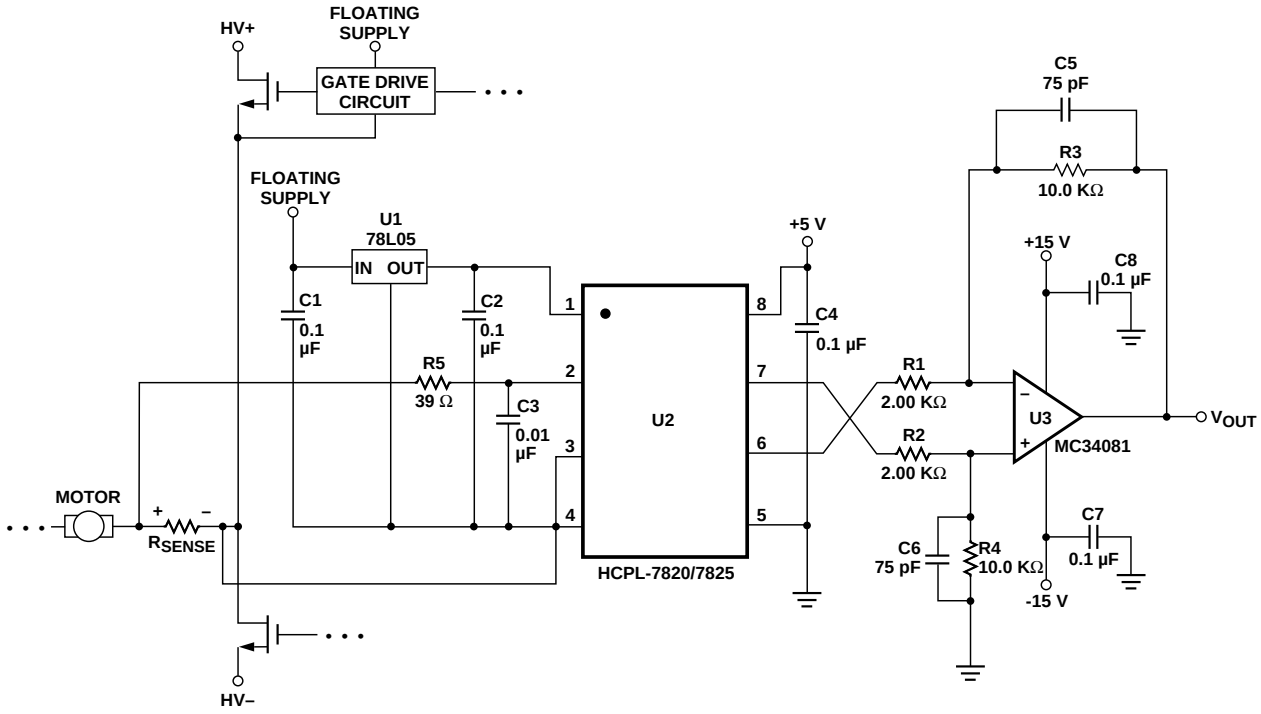


Figure 24. Recommended Application Circuit.

the HCPL-7820/7825 through an RC anti-aliasing filter (R5, C3). And finally, the differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit (U3 and associated components). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

Supplies and Bypassing

As mentioned above, an inexpensive 78L05 three-terminal regulator can be used to reduce the gate-drive power supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 24, 0.1 µF bypass capacitors (C2, C4) should be located as close as possible to the input and output power supply pins of the HCPL-7820/7825. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 0.01 µF bypass capacitor (C3) is also recommended at the input pin(s) due to the switched-capacitor nature of the input circuit. The input bypass capacitor should be at least 1000 pF to maintain gain accuracy of the isolation amplifier. Inductive coupling between the input power-supply bypass capacitor and the input circuit, which includes the input bypass capacitor and the input leads of the HCPL-7820/7825, can introduce additional DC offset in the circuit. Several steps can be taken to minimize the mutual coupling between the two parts of the circuit, thereby improving the offset performance of the design. Separate the two bypass capacitors C2 and C3 as much as possible (even putting them on opposite sides of the PC board), while keeping the total lead lengths, including traces, of each bypass capacitor less than 20 mm. PC board traces should be made as short as possible and placed close together or over ground plane to minimize loop area and pickup of stray magnetic fields. Avoid using sockets, as they will typically increase both loop area and inductance. And finally, using capacitors with small body size and orienting them perpendicular to each other on the PC board can also help. For more information concerning inductive coupling, see the Application Note *Designing with Hewlett-Packard Isolation Amplifiers*.

Shunt Resistor Selection

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). The value of the shunt should be chosen as a compromise between minimizing power dissipation by making the shunt resistance smaller and improving circuit accuracy by making it larger and using more of the input range of the HCPL-7820/7825. Hewlett-Packard recommends 4 different shunts which can be used to sense average currents in motor drives up to 35 A and 35 hp. Table 1 shows the maximum current and horsepower range for each of the LVR-series shunts from Dale. Even higher currents can be sensed with lower value shunts available from vendors such as Dale, IRC, and Isotek (Isabellenhuette). When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient of the shunt can introduce nonlinearity due to the amplitude dependent temperature rise of the shunt. Using a heat sink for the shunt or using a shunt with a lower tempco can help minimize this effect. The Application Note *Designing with Hewlett-Packard Isolation Amplifiers* contains additional information on designing with current shunts.

The recommended method for connecting the isolation amplifier to the shunt resistor is shown in

Table 1. Current Shunt Summary

Shunt Resistor Part Number	Shunt Resistance	Maximum Power Dissipation	Maximum RMS Current	Maximum Horsepower Range
LVR-3.05-1%	50 mΩ	3 W	3 A	0.8-3.0 hp
LVR-3.02-1%	20 mΩ	3 W	8 A	2.2-8.0 hp
LVR-3.01-1%	10 mΩ	3 W	15 A	4.1-15 hp
LVR-5.005-1%	5 mΩ	5 W	35 A	9.6-35 hp

Figure 24. Pin 2 (V_{IN+}) is connected to the positive terminal of the shunt resistor, while pin 3 (V_{IN-}) is shorted to pin 4 (GND1), with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the shunt resistor. In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting pin 3 to the negative terminal of the shunt resistor separately from the power supply return path. When connected this way, both input pins should be bypassed. Whether two or three wires are used, it is recommended that twisted-pair wire or very close PC board traces be used to connect the current shunt to the isolation amplifier circuit to minimize electromagnetic interference to the sense signal.

The 39 Ω resistor in series with the input lead forms a low-pass anti-aliasing filter with the input bypass capacitor with a 400 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

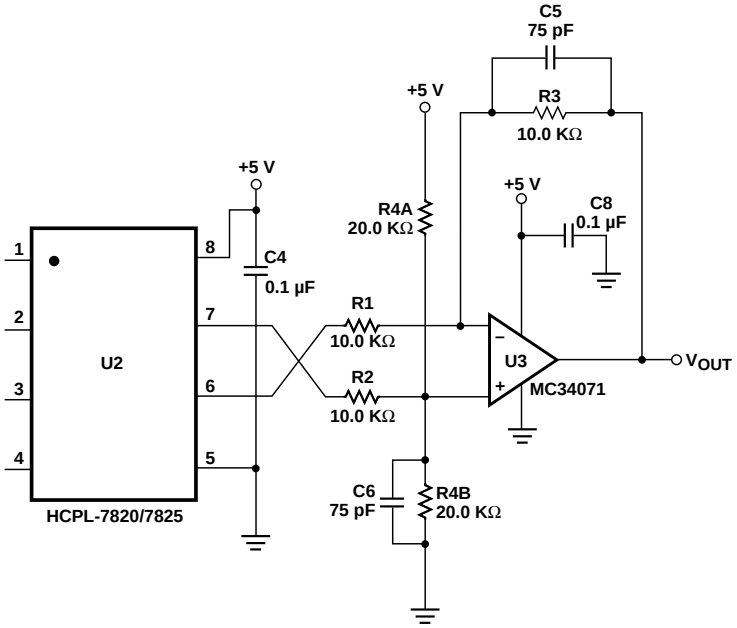


Figure 25. Single-Supply Post-Amplifier Circuit.

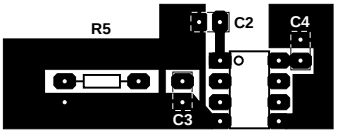


Figure 26. Top Layer of Printed Circuit Board Layout.

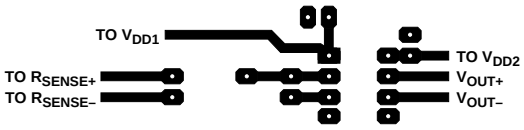


Figure 27. Bottom Layer of Printed Circuit Board Layout.

PC Board Layout

In addition to affecting offset, the layout of the PC board can also affect the common mode rejection (CMR) performance of the isolation amplifier, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below or extend much wider than the HCPL-7820/7825. Using surface-mount components can help achieve many of the PCB objectives discussed in the preceding paragraphs. An example through-hole PCB layout illustrating some of the more important layout recommendations is shown in Figures 26 and 27. See the Application Note *Designing with Hewlett-Packard Isolation Amplifiers* for more information on PCB layout considerations.

Post-Amplifier Circuit

The recommended application circuit (Figure 24) includes a post-amplifier circuit that serves three functions: to reference the output signal to the desired level (usually ground), to amplify the signal to appropriate levels, and to help filter output noise. The particular op-amp used in the post-amp is not critical; however, it should have low enough offset and high enough bandwidth and slew rate so that it does not adversely affect circuit performance. The offset of the op-amp should be low relative to the output offset of the HCPL-7820/7825, or less than about 5 mV.

To maintain overall circuit bandwidth, the post-amplifier circuit should have a bandwidth at least twice the minimum bandwidth of the isolation amplifier, or about 400 kHz. To obtain a bandwidth of 400 kHz with a gain of 5, the op-amp should have a gain-bandwidth greater than 2 MHz. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter. These capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier (doubling the capacitor values halves the circuit bandwidth). The component values shown in Figure 24 form a differential amplifier with a gain of 5 and a cutoff frequency of approximately 200 kHz and were chosen as a compromise between low noise and fast response times. The overall recommended application circuit has a bandwidth of 130 kHz, a rise time of 2.6 µs and delay to 90% of 4.2 µs.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and gain tolerance for the overall circuit. Resistor networks with even better ratio tolerances can be used which offer better performance, as well as reducing the total component count and board space.

The post-amplifier circuit can be easily modified to allow for single-supply operation. Figure 25 shows a schematic for a post-amplifier for use in 5 V single-supply applications. One additional resistor is needed and the gain is decreased to allow circuit operation over the full input voltage range. See the Application Note *Designing with Hewlett-Packard Isolation Amplifiers* for more information on the post-amplifier circuit.

Other Information

As mentioned above, reducing the bandwidth of the post amplifier circuit reduces the amount of output noise. Figure 21 shows how the output noise changes as a function of the post-amplifier bandwidth. The post-amplifier circuit exhibits a first-order low-pass filter characteristic. For the same filter bandwidth, a higher-order filter can achieve even better attenuation of modulation noise due to the second-order noise shaping of the sigma-delta modulator. For more information on the noise characteristics of the HCPL-7820/7825, see the Application Note *Designing with Hewlett-Packard Isolation Amplifiers.*

The HCPL-7820/7825 can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (280 kΩ) and input bias current (1 µA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 39 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth.