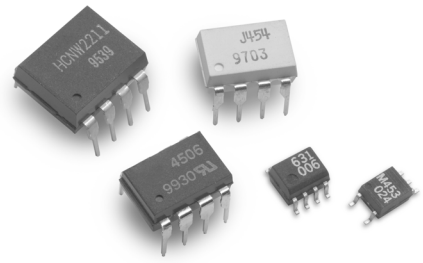
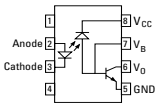
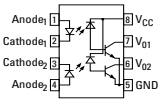
1 MBd Digital Transistor Output Optocoupler

Product Selection



Device	Part No.	Package				If	Prop Delay		CTR		CMR-V/μs @ (Vcm)			VDE 0884			Insulation		Note
		300 mil DIP	SO8	400 mil DIP	SO 5	mA	tPHL μs (max)	tPLH μs (max)	Min %	Max %	1000 (10 V)	10000 (1.5 kV)	15000 (1.5 kV)	Peak Voltage 630 V	Peak Voltage 890 V	Peak Voltage 1414 V	UL = 1 min. 2500 V	UL = 1 min. 5000 V	
Single	6N135	•				16	2.0	2.0	7	50	•						•	B	
	HCPL-0500		•			16	2.0	2.0	7	50	•						•		
	HCNW135			•		16	2.0	2.0	7	150	•					•		•	
	6N136	•				16	1.0	1.0	19	50	•						•	B	
	HCPL-0501		•			16	1.0	1.0	19	50	•						•		
	HCNW136			•		16	1.0	1.0	19	150	•					•		•	
	HCPL-4502	•				16	1.0	1.0	19	50	•						•	B	1
	HCPL-M452				•	16	1.0	1.0	19	50		•					•		3
	HCPL-0452		•			16	1.0	1.0	19	50	•						•		1
	HCNW4502			•		16	1.0	1.0	19	150	•					•		•	1
	HCPL-4503	•				16	1.0	1.0	19	50			•	•			•	B	1,2
	HCPL-0453		•			16	1.0	1.0	19	50			•				•		1
	HCNW4503			•		16	1.0	1.0	19	150			•			•		•	1
	HCPL-M453				•	16	1.0	1.0	19	50			•				•		3
	HCPL-M454				•	12	1.0	1.4	26	65		•					•		3
	HCPL-M456				•	10	0.4	0.55	44	>90			•				•		
	HCPL-4504	•				12	1.0	1.14	26	65		•		•			•	B	1,2
	HCPL-0454		•			12	1.0	1.14	26	65		•					•		1
	HCPL-J454	•				12	0.5	0.7	21	65			•		•		•		
	HCNW4504			•		12	0.5	0.7	25	65		•				•		•	1
	HCPL-4506	•				10	0.4	0.55	44	>90			•	•			•	B	3
	HCPL-0466		•			10	0.4	0.55	44	>90			•				•		
	HCPL-J456	•				10	0.4	0.55	44	>90			•		•		• A		
	HCNW4506			•		10	0.4	0.5	44	>90			•			•		•	
Dual	HCPL-2530	•				16	2.0	2.0	7	50	•						•	B	
	HCPL-0530		•			16	2.0	2.0	7	50	•						•		
	HCPL-2531	•				16	1.0	1.0	19	50	•						•	B	
	HCPL-0531		•			16	1.0	1.0	19	50	•						•		
	HCPL-4534	•				16	1.0	1.0	19	50			•				•	B	
	HCPL-0534		•			16	1.0	1.0	19	50			•				•		

Shaded Text–RECOMMENDED FOR NEW DESIGNS

NOTES: 1. PIN 7 not connected. 2. 630 V peak VDE 0884 with option 060. 3. No built-in pull resistor. A. 3750 Vrms / 1 min B. Option 020

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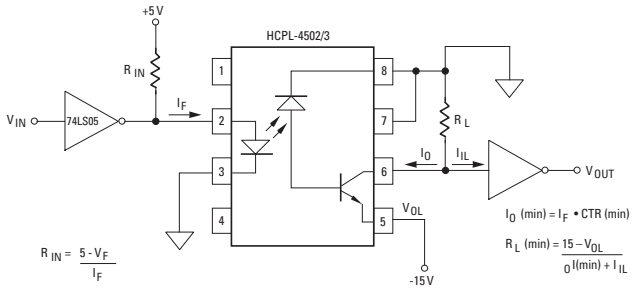
The circuit shows how a 0 to 5 V logic signal can be level shifted to a -15 to 0 V signal. This circuit can safely be used for level shifting up to ±800 V. The circuit uses an open collector output logic gate, the 74LS405, to drive the LED of the HCPL-4502/3 optocoupler. The HCPL-4502/3 also has an open-collector output. The designer chooses R_{IN} to agree with the equation shown in the schematic. This equation sets the value of the optocoupler LED forward current. The output of the HCPL-4502/3 requires a pull-up resistor, R_L. The current-transfer ratio (CTR) of the optocoupler determines the maximum amount of current the optocoupler output can sink while maintaining the output voltage (between pins 5 and 6) of 0.5 V or less.

The benefits of the application is that it reduces transient immunity problem and is a convenient way of replacing pulse transformer for high-voltage level shifting.

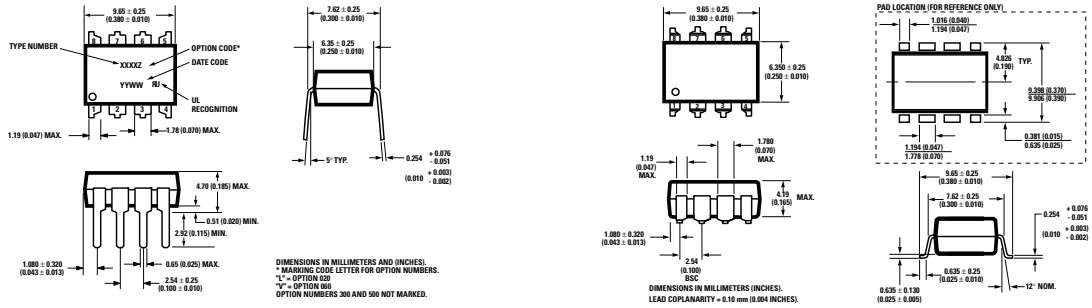
Typical applications include:
- High Speed Logic Ground Isolation
- Replace slow Phototransistor Isolators
- Replace Pulse Transformers
- Line Receivers
- Analog Signal Ground Isolation

Typical Level Shifting/TTL Interface Block Diagram

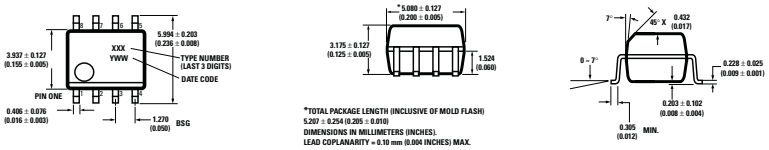


NOTE: FOR BEST CMR PERFORMANCE, CONNECT PIN 7 TO PIN 8.

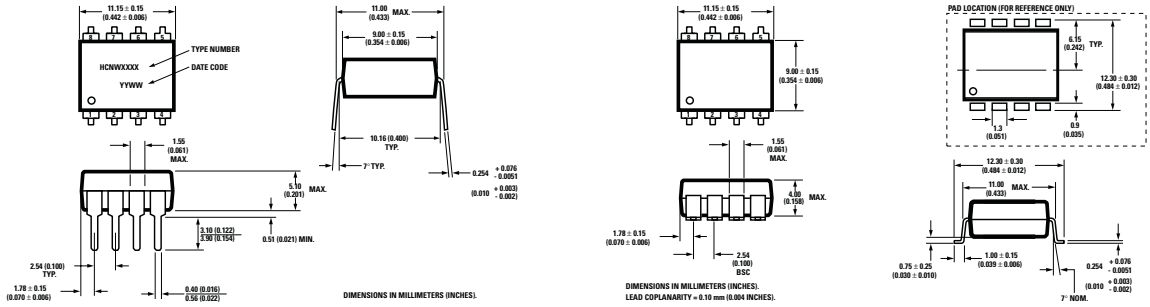
300 mil 8-pin DIP



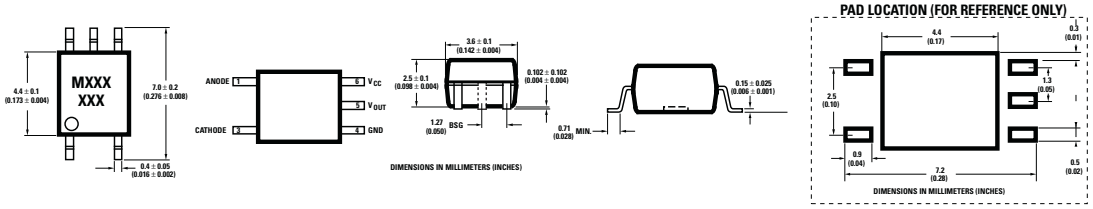
SO-8 SMD



400 mil 8-pin DIP



SO-5



Options Available

#020 - UL 5000 V rms/1 Minute Option
#060 - VDE 0884 Approved Part Option
#300 - Gull Wing Surface Mount Option
#500 - Tape & Reel Packaging Option
Remarks: The notation '#' is used for existing products, while (new) products launched since 15th July 01 will use '-'.

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