
HD74HC160/HD74HC161/ HD74HC162/HD74HC163

Synchronous Decade Counter (Direct Clear)
Synchronous 4-bit Binary Counter (Direct Clear)
Synchronous Decade Counter (Synchronous Clear)
Synchronous 4-bit Binary Counter (Synchronous Clear)

HITACHI

Description

The HD74HC160 and the HD74HC162 are 4 bit decade counters, and the HD74HC161 and the HD74HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the clock input waveform.

These counters may be preset using the load input. Presetting of all four flip-flops is synchronous to the rising edge of clock. When load is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of clock. If the load input is taken high before the positive edge of clock the count operation will be unaffected.

All of these counters may be cleared by utilizing the clear input. The clear function on the HD74HC162 and HD74HC163 counters is synchronous to the clock. That is, the counters are cleared on the positive edge of clock while the clear input is held low.

The HD74HC160 and HD74HC161 counters are cleared asynchronously. When the clear is taken low the counter is cleared immediately regardless of the clock.

Two active high enable inputs Enable P and Enable T and a ripple carry output are provided to enable easy cascading of counters. Both enable inputs must be high to count. The Enable T input also enables the Ripple Carry output. When enabled, the Ripple Carry outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A outputs. The Ripple Carry output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 18 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max

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- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

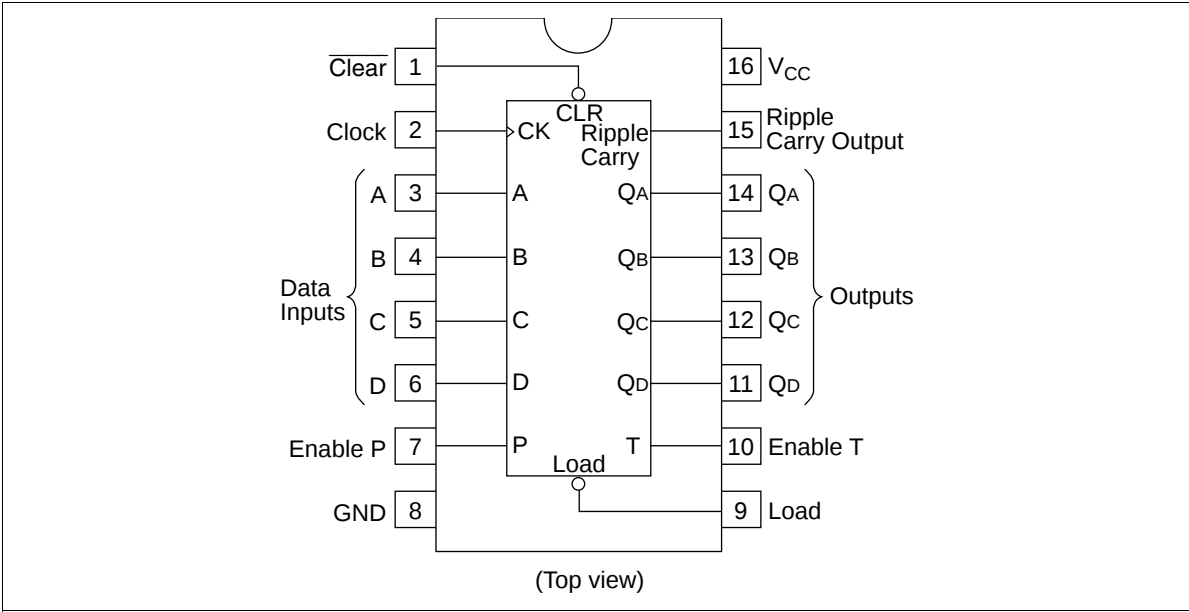
Function Table

Inputs					Outputs
Clock	$\overline{\text{Clear}}^{*1}$	Load	Enable P	Enable T	Q_n
	L	X	X	X	Reset-clear
	H	L	X	X	Load input data
	H	H	H	H	Count
	H	H	L	X	No count
	H	H	X	L	No count

Note: 1. 162 and 163 Only-160 and 161 are Asynchronous Clear Devices

	Decade Counter	Binary Counter
Asynchronous clear	HD74HC160P	HD74HC161P
Synchronous clear	HD74HC162P	HD74HC163P

Pin Arrangement



DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

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AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{cc} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	23		
Propagation delay time	t _{PLH}	2.0	—	—	160	—	200	ns	Clock to Q
		4.5	—	18	32	—	40		
		6.0	—	—	27	—	34		
	t _{PHL}	2.0	—	—	225	—	280	ns	Clear to Q (HC160, HC161 only)
		4.5	—	23	45	—	56		
		6.0	—	—	38	—	48		
		2.0	—	—	150	—	190	ns	Enable T to Ripple Carry output
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
		2.0	—	—	200	—	250	ns	Clock to Ripple carry output
		4.5	—	16	40	—	50		
		6.0	—	—	34	—	43		
Setup time	t _{su}	2.0	125	—	—	156	—	ns	Data to Clock
		4.5	25	9	—	31	—		
		6.0	21	—	—	26	—		
		2.0	125	—	—	156	—		Load to Clock
		4.5	25	15	—	31	—		
		6.0	21	—	—	26	—		
		2.0	125	—	—	156	—		Clear to Clock (HC162, HC163 only)
		4.5	25	—	—	31	—		
		6.0	21	—	—	26	—		
Hold time	t _h	2.0	0	—	—	0	—	ns	
		4.5	0	-7	—	0	—		
		6.0	0	—	—	0	—		
Removal time	t _{rem}	2.0	100	—	—	125	—	ns	
		4.5	20	7	—	25	—		
		6.0	17	—	—	21	—		

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$) (cont)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$		$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min		
Pulse width	t_w	2.0	80	—	—	100	—	ns
		4.5	16	6	—	20	—	
		6.0	14	—	—	17	—	
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns
		4.5	—	5	15	—	19	
		6.0	—	—	13	—	16	
Input capacitance	C_{in}	—	—	5	10	—	10	pF

Function Table

Count Enable/Disable

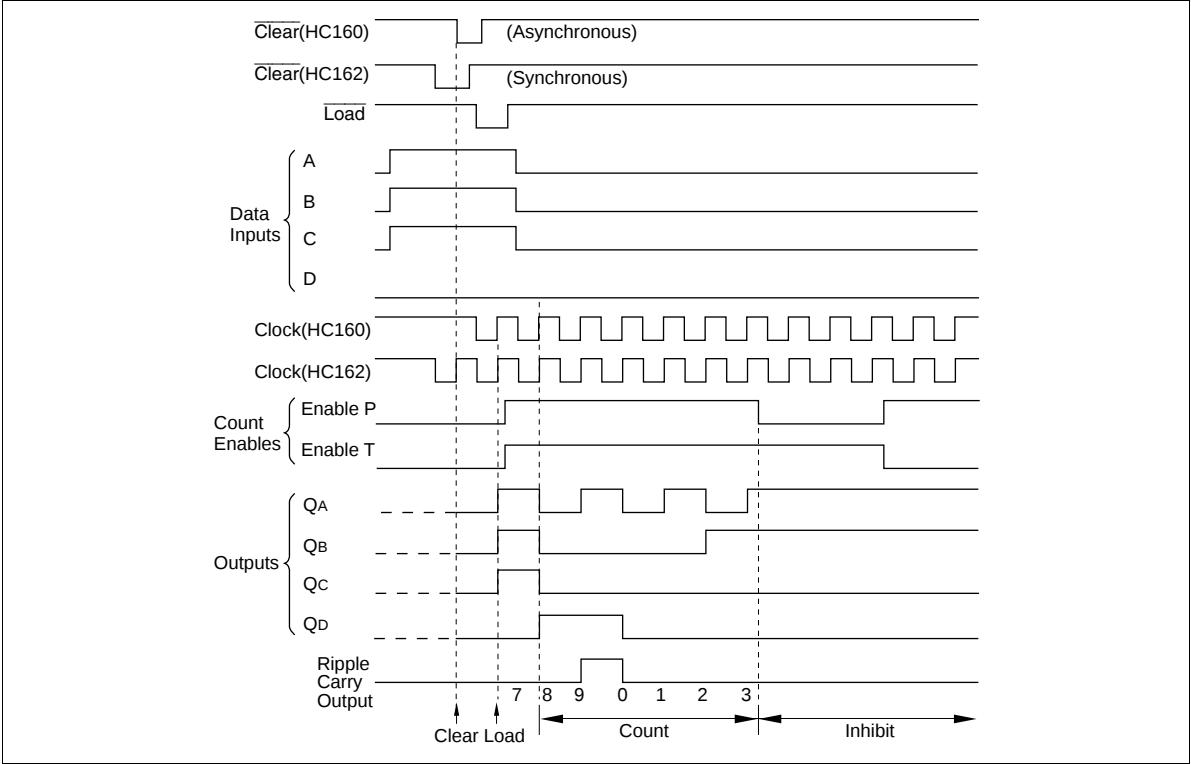
Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q_A to Q_D	Ripple Carry Output
H	H	H	Count	High when Q_A to Q_D are maximum
L	H	H	No count	
X	L	H	No count	High when Q_A to Q_D are maximum
X	H	L	No count	L
X	L	L	No count	L

Timing Diagram

HD74HC160/HD74HC162

Sequence illustrated in waveforms.

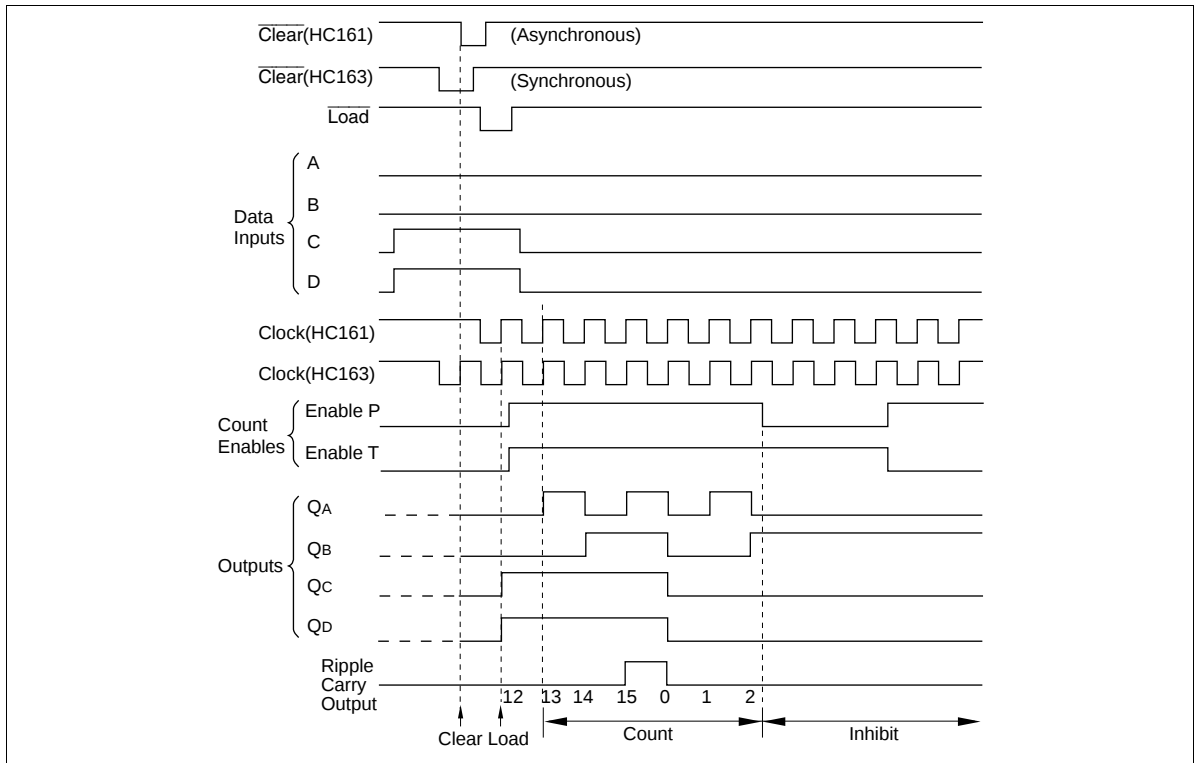
- 1. Clear outputs to zero.
- 2. Preset to BCD seven.
- 3. Count to eight, nine, zero, one, two and three.
- 4. Inhibit



HD74HC161/HD74HC163

Sequence illustrated in waveforms.

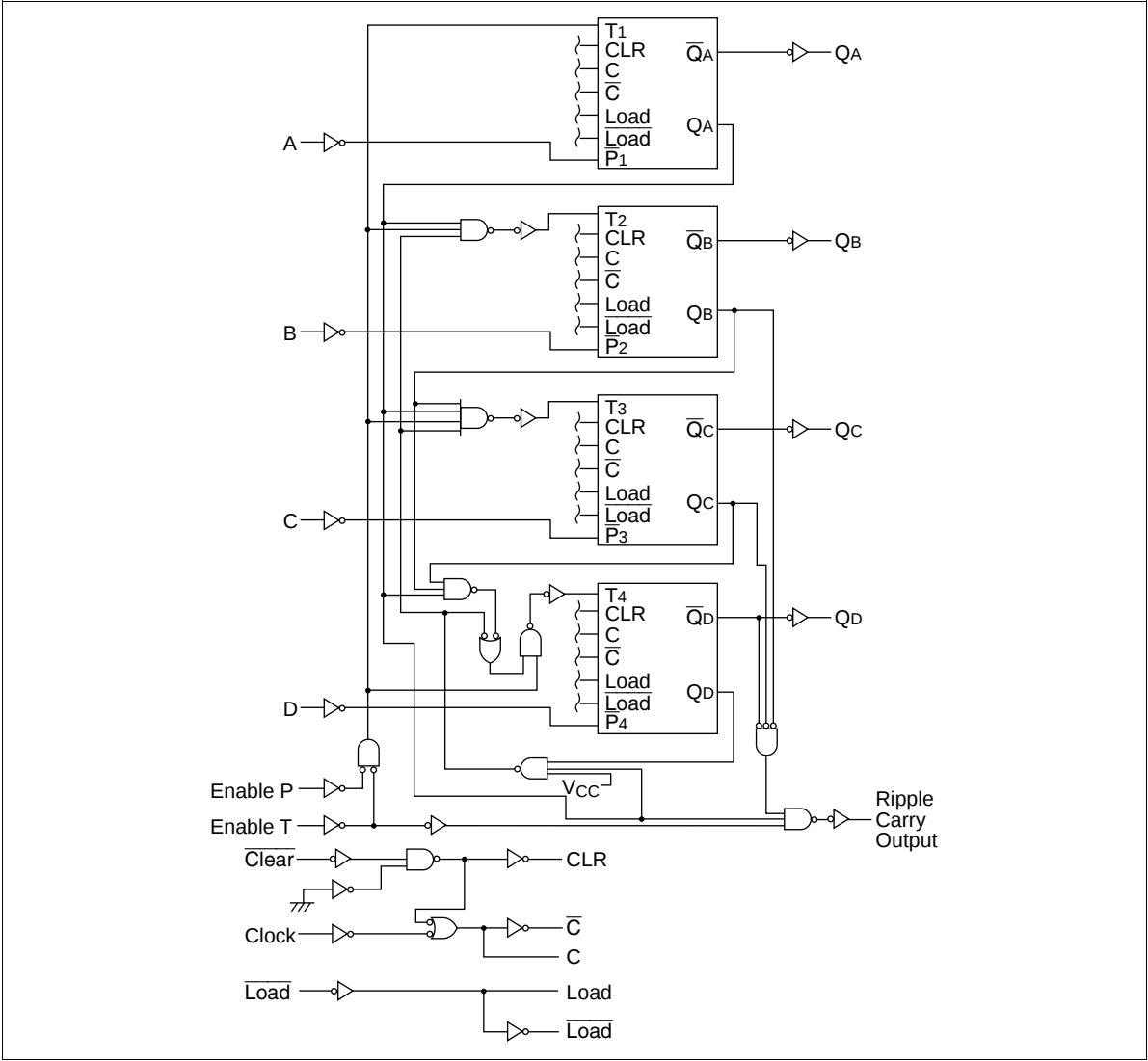
1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit



Logic Diagram

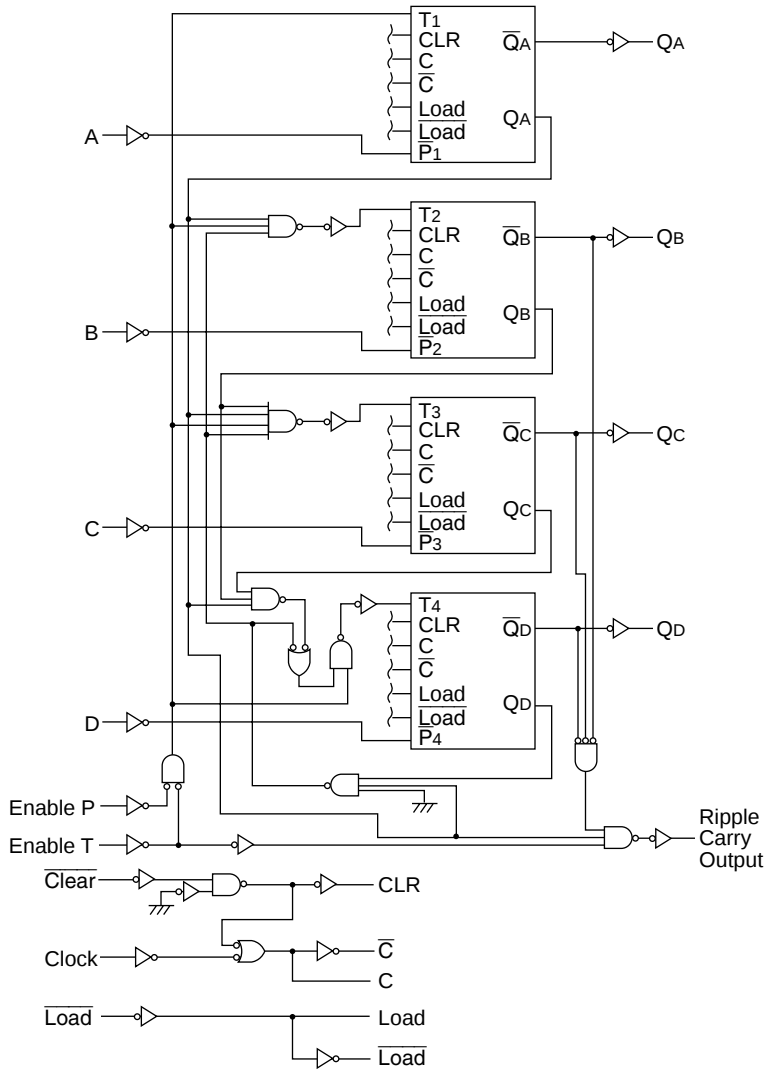
HD74HC160

Decade Counter with Asynchronous Clear



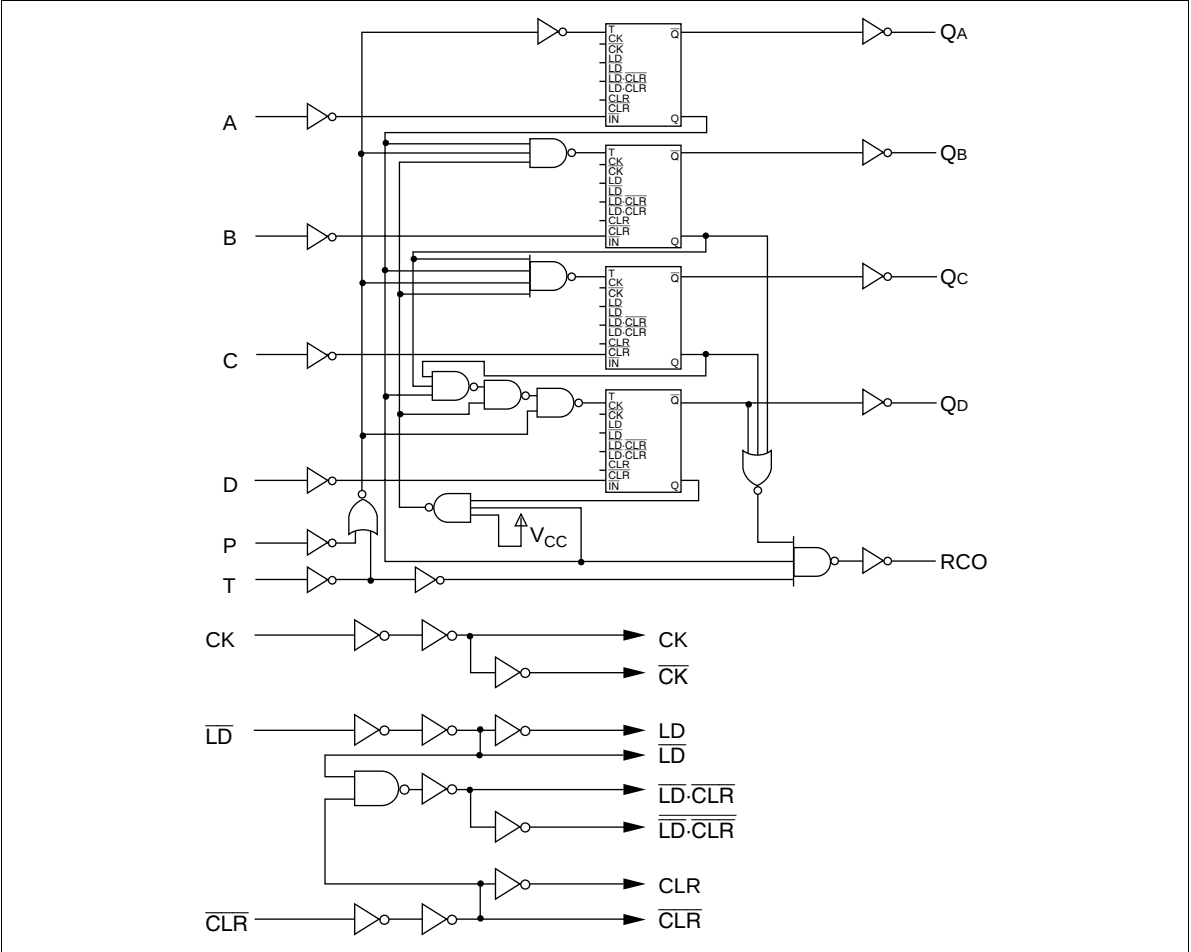
HD74HC161

4-bit Binary Counter with Asynchronous Clear



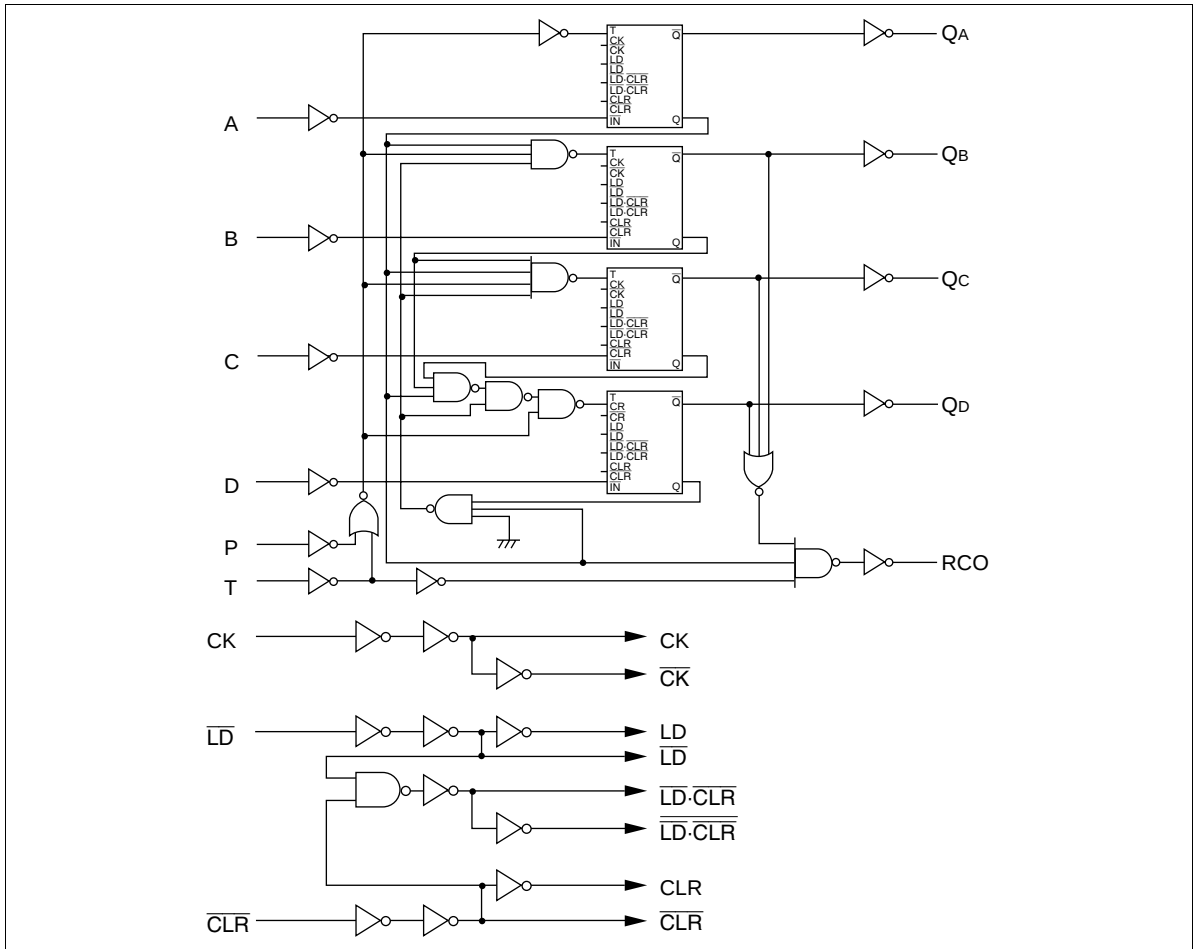
HD74HC162

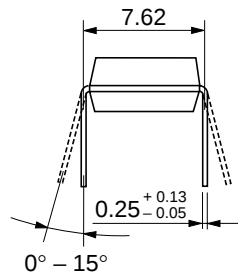
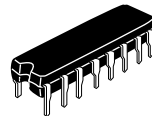
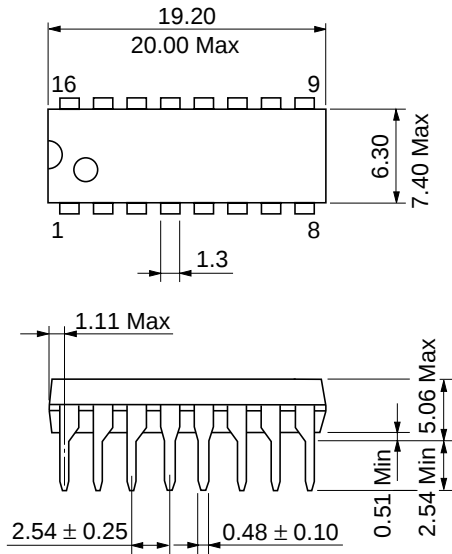
Decade Counter with Synchronous Clear



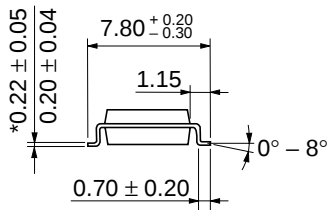
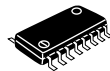
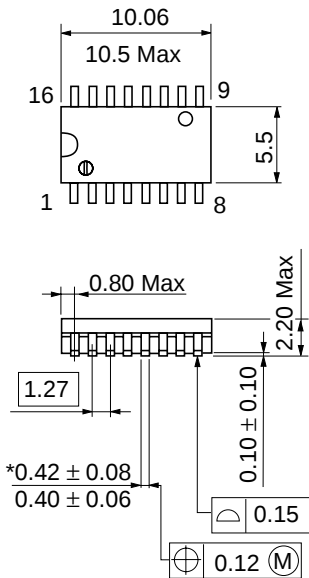
HD74HC163

4-bit Binary Counter with Synchronous Clear



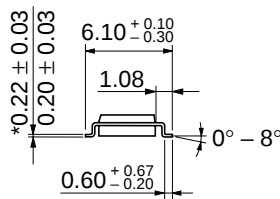
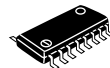
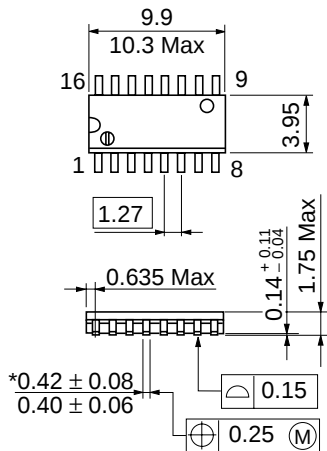


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



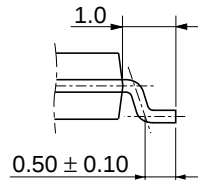
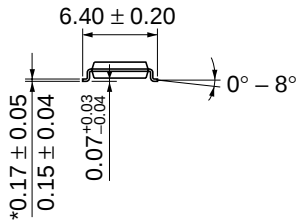
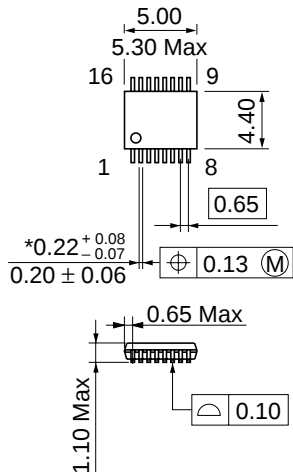
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension



*Dimension including the plating thickness
Base material dimension

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EIAJ	Conforms
Weight (reference value)	0.15 g



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JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

$$\frac{\text{*Dimension including the plating thickness}}{\text{Base material dimension}}$$

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