

# HD74HC165

## Parallel-load 8-bit Shift Register

# HITACHI

### Description

This 8-bit serial shift register shifts data from  $Q_A$  to  $Q_H$  when clocked. Parallel inputs to each stage are enabled by a low level at the Shift/Load input. Also included is a gated clock input and a complementary output from the eighth bit.



Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

### Features

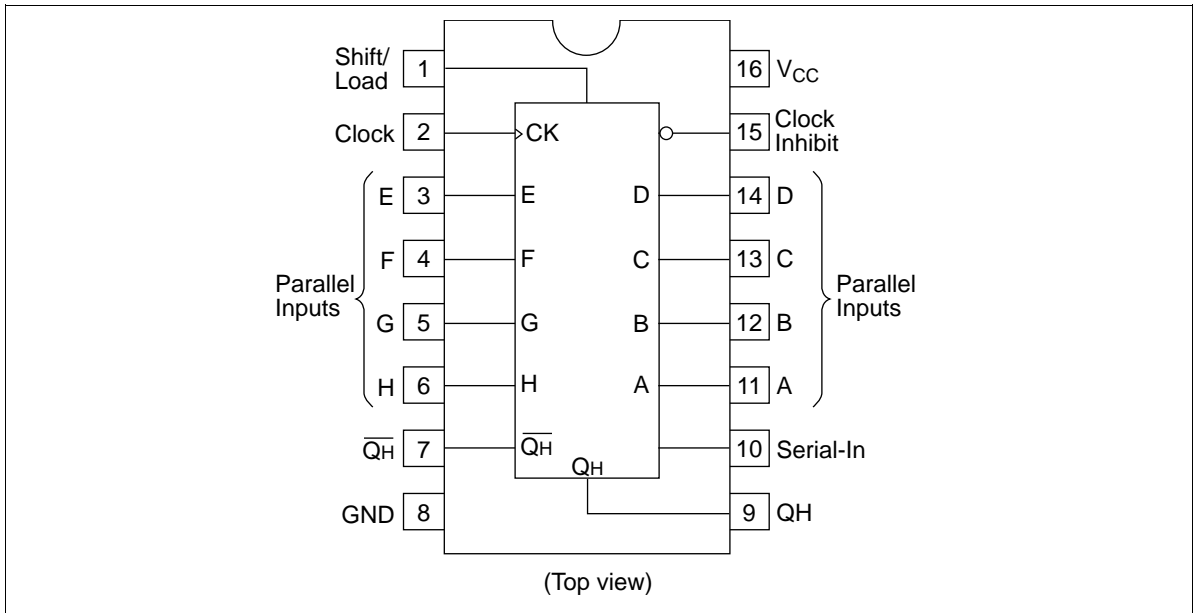
- High Speed Operation:  $t_{pd}$  (Clock to  $Q_H$ ) = 21 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

### Function Table

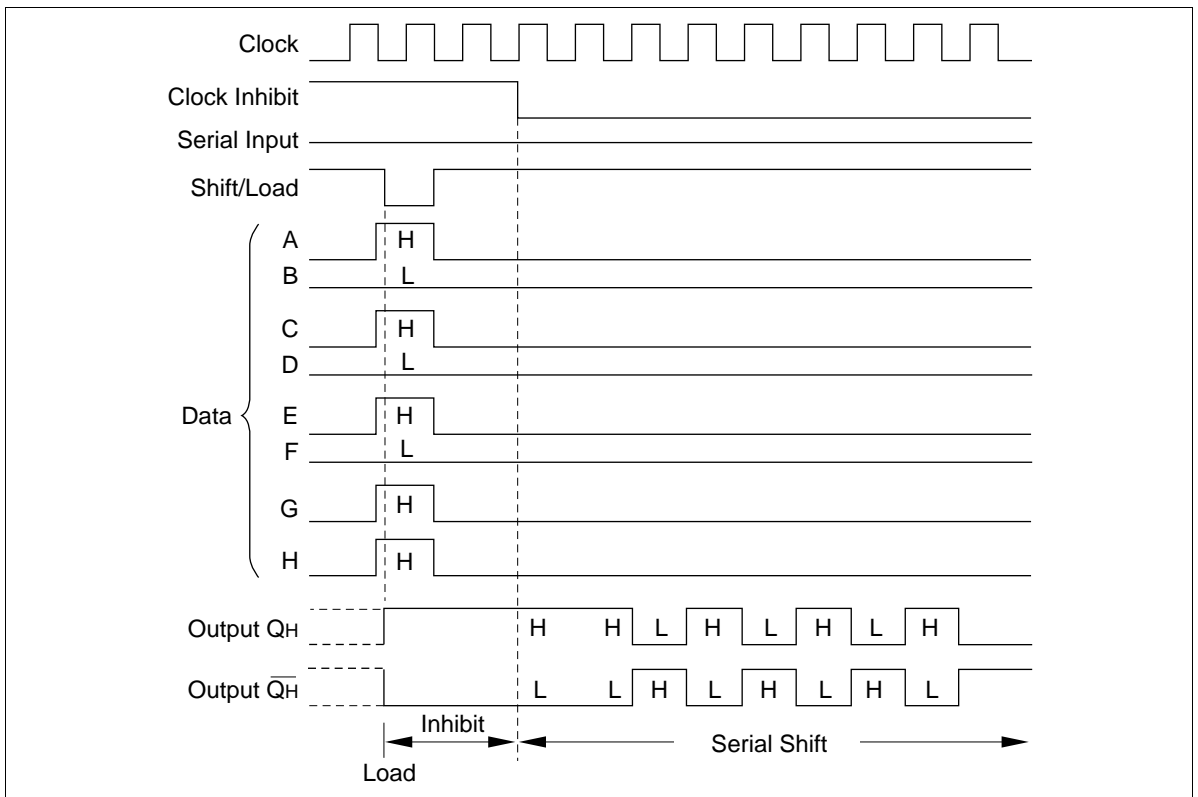
#### Inputs

Shift/Load	Clock Inhibit	Clock	Serial	Parallel	Internal outputs		Output
				A ..... H	$Q_A$	$Q_B$	$Q_H$
L	X	X	X	a ..... h	a	b	h
H	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L		H	X	H	$Q_{An}$	$Q_{Gn}$
H	L		L	X	L	$Q_{An}$	$Q_{Gn}$
H	H	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

## Pin Arrangement



## Timing Diagram



DC Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			I <sub>OH</sub> = -5.2 mA
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I <sub>OL</sub> = 4 mA
		6.0	—	—	0.26	—	0.33			I <sub>OL</sub> = 5.2 mA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA	

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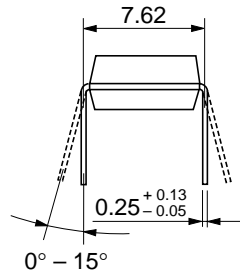
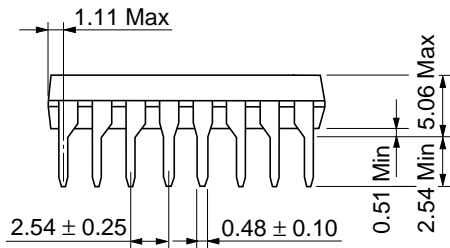
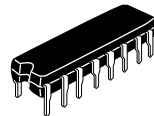
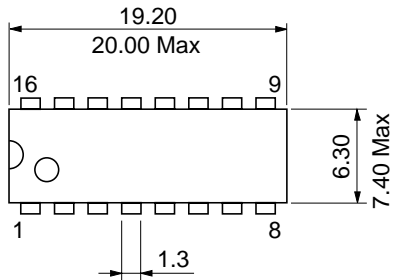
## AC Characteristics ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions							
			Min	Typ	Max	Min	Max									
Maximum clock frequency	$f_{max}$	2.0	—	—	5	—	4	MHz								
		4.5	—	—	27	—	21									
		6.0	—	—	32	—	25									
Propagation delay time	$t_{PLH}$	2.0	—	—	150	—	190	ns	Clock to $Q_H$ or $\overline{Q}_H$							
		4.5	—	21	30	—	38									
		6.0	—	—	26	—	33									
	$t_{PHL}$	2.0	—	—	160	—	200		Shift/Load to $Q_H$ or $\overline{Q}_H$							
		4.5	—	23	32	—	40									
		6.0	—	—	27	—	34									
		2.0	—	—	150	—	190			H to $Q_H$ or $\overline{Q}_H$						
		4.5	—	21	30	—	38									
		6.0	—	—	26	—	33									
	Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Parallel data inputs to Shift/Load						
			4.5	20	-3	—	25	—								
			6.0	17	—	—	21	—								
2.0			100	—	—	125	—	—	ns	Serial input to Clock						
											4.5	20	3	—	25	—
											6.0	17	—	—	21	—
2.0			100	—	—	125	—	—	ns	Shift/load to Clock						
											4.5	20	—	—	25	—
											6.0	17	—	—	21	—
Removal time			$t_{rem}$	2.0	100	—	—	125	—	ns	Clock to Clock inhibit or Clock inhibit to Clock					
				4.5	20	6	—	25	—							
				6.0	17	—	—	21	—							
Hold time	$t_h$	2.0	5	—	—	5	—	ns	Shift/Load to parallel data input							
		4.5	5	-3	—	5	—									
		6.0	5	—	—	5	—									
		2.0	5	—	—	5	—	—	ns	Clock to Serial data input						
											4.5	5	3	—	5	—
											6.0	5	—	—	5	—
		2.0	5	—	—	5	—	—	ns	Clock to Shift/Load						
											4.5	5	—	—	5	—
											6.0	5	—	—	5	—

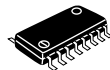
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AC Characteristics ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns) (cont)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	Clock, Shift/Load
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	$t_{TLH}$	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



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