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April 1st, 2010 Renesas Electronics Corporation

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HD74HC195

4-bit Parallel-Access Shift Register

REJ03D0590-0200 (Previous ADE-205-467) Rev.2.00 Jan 31, 2006

Description

This shift register features parallel inputs, parallel outputs, J- \overline{K} serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; shift from Q_A towards Q_D .

Parallel loading is accomplished by applying the four bits of data, and taking the Shift/Load control Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the Shift/Load control input is high. Serial data for this mode is entered at the $J-\overline{K}$ inputs. These inputs allow the first stage to perform as a $J-\overline{K}$ or toggle flip-flop as shown in the function table.

Features

• High Speed Operation: t_{pd} (Clock to Q) = 13 ns typ ($C_L = 50 \text{ pF}$)

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage: $V_{CC} = 2$ to 6 V

• Low Input Current: 1 µA max

• Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC195P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_

Function Table

Inputs								Outputs					
Clear Shift/ Clo		Clock	Se	rial	Parallel				Outputs				
Clear	Load Clock	CIOCK	J	K	Α	В	С	D	Q_A	Q _B	Qc	\mathbf{Q}_{D}	\mathbf{Q}_{D}
L	Х	Х	Χ	X	Χ	Х	Х	Х	L	L	L	L	Н
Н	L		Х	Х	а	b	С	d	а	b	С	d	d
Н	Н	L	Х	Х	Х	Х	Х	Х	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\overline{Q}_{D0}
Н	Н		L	Н	Χ	Χ	Х	Х	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\overline{Q}_Cn
Н	Н		L	L	Χ	Χ	Х	Х	Ц	Q_{An}	Q_{Bn}	Q_{Cn}	\overline{Q}_Cn
Н	Н		Н	Н	Х	Х	Х	Х	Н	Q_{An}	Q_{Bn}	Q _{Cn}	$\overline{\mathbf{Q}}_{Cn}$
Н	Н		Н	L	Х	Х	Х	Х	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\overline{Q}_Cn

H : high level (steady state)L : low level (steady state)

X : don't care

 \int : transition from low to high level.

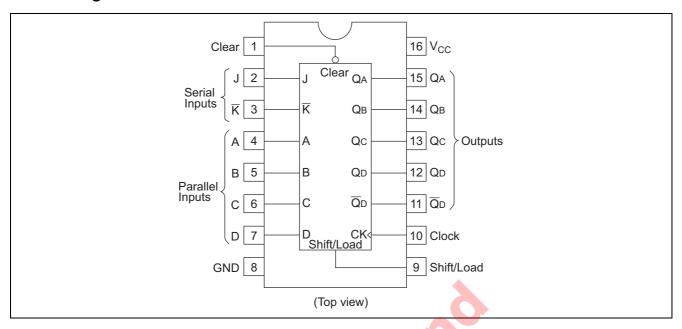
a, b, c, d : the level of steady-state input at inputs A, B, C or D respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} : the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady-state input conditions were

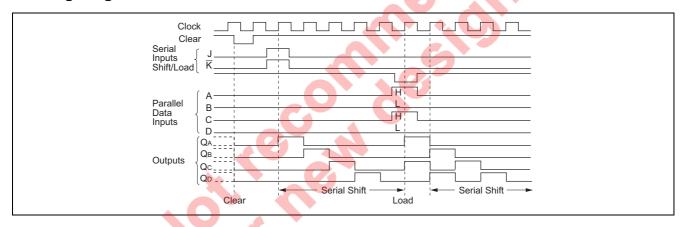
established.

 Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} : the level of Q_A , Q_B , Q_C or Q_D respectively before the most recent $\sqrt{}$ transition of the clock.

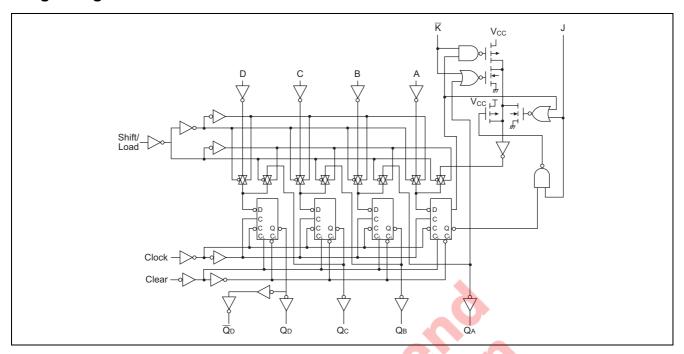
Pin Arrangement



Timing Diagram



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to V _{CC} +0.5	V
Input / Output diode current	I _{IK} , I _{OK}	±20	mA
Output current	lo	±25	mA
V _{CC} , GND current	I _{CC} or I _{GND}	±50	mA
Power dissipation	P _T	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	2 to 6	V	
Input / Output voltage	V _{IN} , V _{OUT}	0 to V _{CC}	V	
Operating temperature	Та	-40 to 85	°C	
Input rise / fall time*1	t _r , t _f	0 to 1000	ns	V _{CC} = 2.0 V
		0 to 500		V _{CC} = 4.5 V
		0 to 400		$V_{CC} = 6.0 \text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

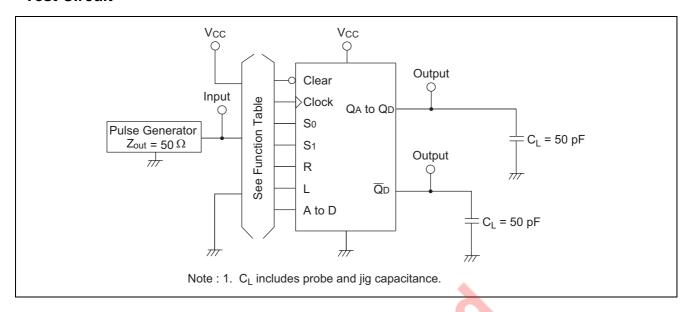
Electrical Characteristics

Switching Characteristics

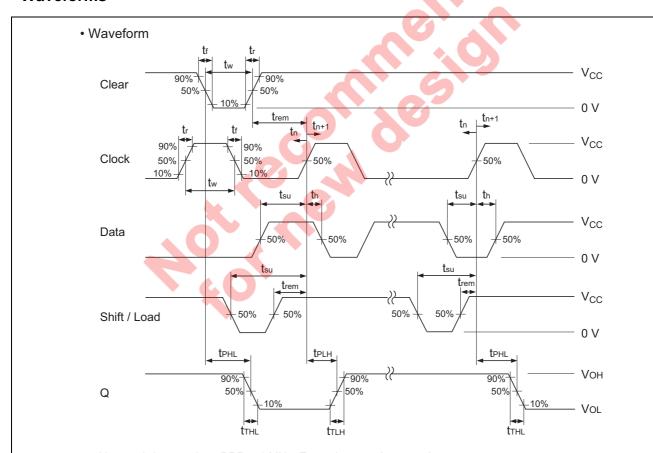
 $(C_L = 50 \text{ pF, Input } t_r = t_f = 6 \text{ ns})$

11	Symbol	V 00	Ta = 25°C		$Ta = -40 \text{ to } +85^{\circ}C$		11!1	Table Caraditions	
Item		V _{CC} (V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
Maximum clock	f _{max}	2.0		_	6	_	5	MH_Z	
frequency		4.5		_	30	_	24		
		6.0		_	35	_	28		
Propagation delay	t _{PHL}	2.0		_	140	_	175	ns	Clock to Q
time		4.5		13	28	_	35		
		6.0	l	_	24	_	30		
	t _{PLH}	2.0	-	_	140	_	175	ns	
		4.5	1	13	28		35		
		6.0		_	24	_	30		
	t _{PHL}	2.0	-	_	150	_	190	ns	Clear to Q
		4.5	-	15	30	_	38		
		6.0	_	_	26	_	33		
Pulse width	t _w	2.0	80	_	_	100	_	ns	Clock to Clear
		4.5	16	7	_	20	_		
		6.0	14	_	_	17	70		
Setup time	t _{su}	2.0	100	_	_	125	\	ns	A, B, C, D, J, \overline{K} to Clock
		4.5	20	6	_	25			
		6.0	17	_	_	21		A	
		2.0	100	_	_	125		ns	Shift/Load to Clock
		4.5	20	13	_	25			
		6.0	17	_	-	21			
Hold time	t _h	2.0	0	_		0	1	ns	Any input except Shift/Load
		4.5	0	-3		0	_		
		6.0	0		_	0	_		
Removal time	t _{rem}	2.0	75		_	95	_	ns	Shift/Load to Clock
		4.5	15	8	4	19	_		
		6.0	13	- (93	16	_		
		2.0	25		9	31	_	ns	Clear inactive to Clock
		4.5	5	0	_	6	_		
		6.0	4	_		5	_		
Output rise/fall	t_{TLH}	2.0		_	75		95	ns	
time	t _{THL}	4.5		5	15	_	19		
		6.0	_	_	13	_	16		
Input capacitance	Cin		_	5	10	_	10	pF	

Test Circuit



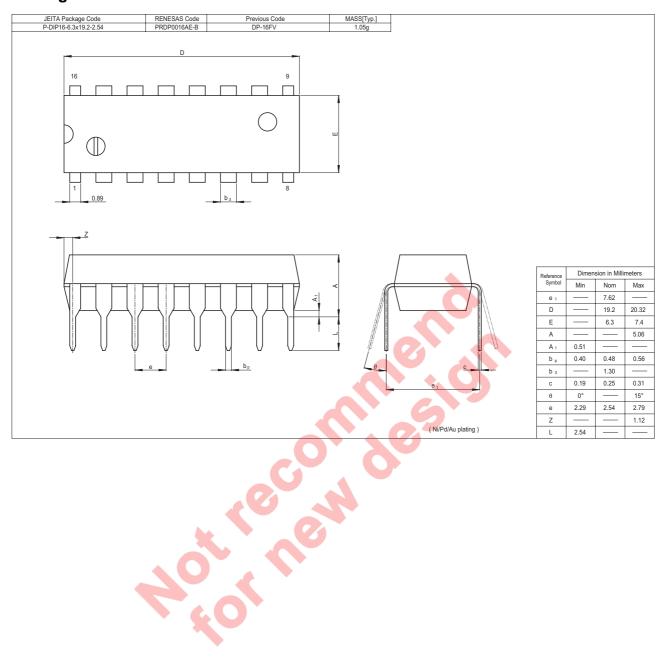
Waveforms



Notes : 1. Input pulse : PRR \leq 1 MHz, Zo = 50 $\Omega,\,t_{r} \leq$ 6 ns, $t_{f} \leq$ 6 ns

- 2. A clear pulse is applied prior to each test.
- 3. Propagation delay times (tPLH and tPHL) are measured at tn+1. Proper shifting of data is verified at tn+4 with a functional test.
- 4. J and \overline{K} inputs are tested the same as data A, B, C and D inputs except that Shift / Load input remains high.
- 5. tn: bit time before clocking transition.
- 6. tn+1: bit time after one clocking transition.
- 7. tn+4: bit time after four clocking transition.

Package Dimensions



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