HD74HCT620, HD74HCT623

Octal Bus Transceivers (with inverted 3-state outputs)
Octal Bus Transceivers (with 3-state outputs)

REJ03D0671–0200
(Previous ADE-205-561)
Rev.2.00
Mar 30, 2006

Description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{GBA}$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{GBA}$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the HD74HCT623 or complementary for the HD74HCT620.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Bus to Bus) = 15 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads (Q_A to Q_H outputs)
- Wide Operating Voltage: V_{CC} = 4.5 to 5.5 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)
- Ordering Information

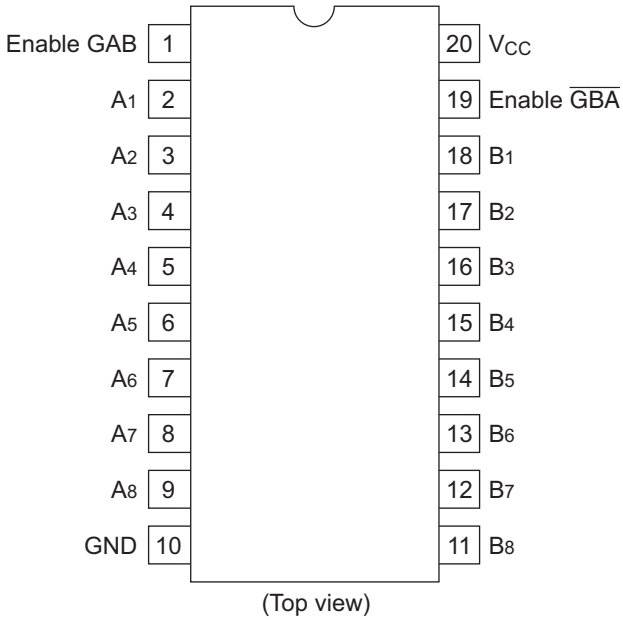
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT623FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HCT620RPEL HD74HCT623RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Enable Inputs		Operation	
$\overline{GBA}$	GAB	HD74HCT620	HD74HCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

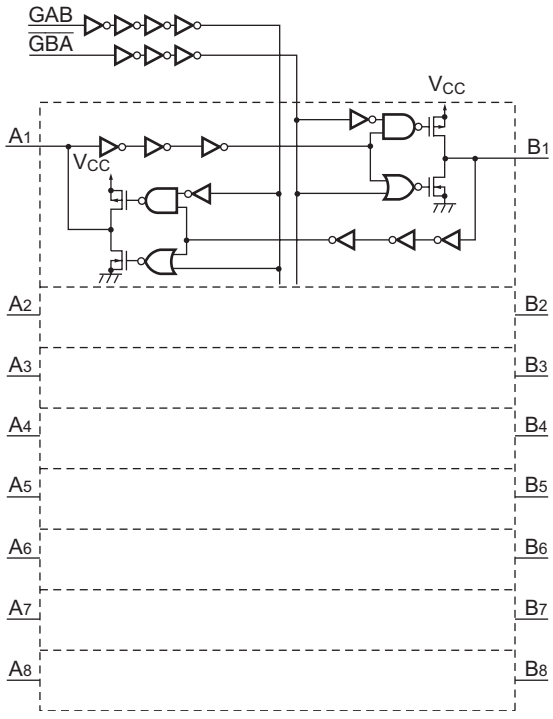
Pin Arrangement



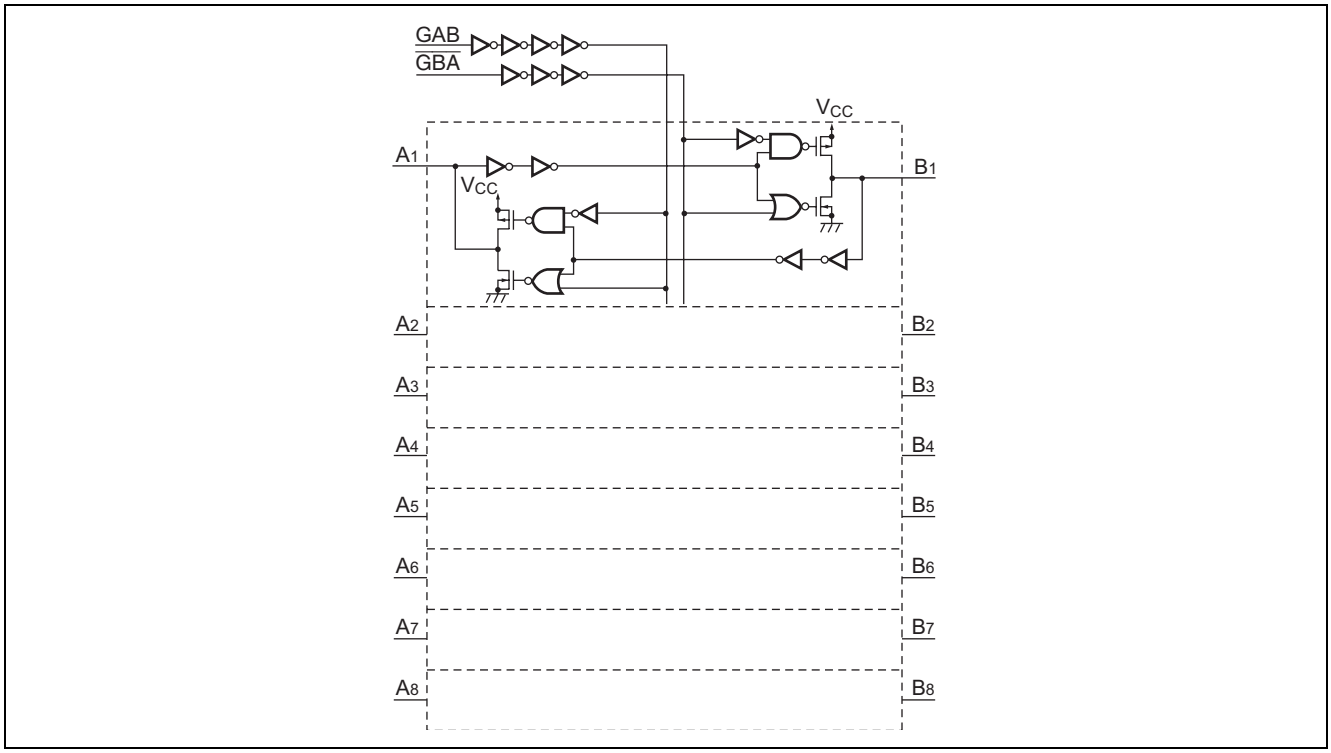
(Top view)

Logic Diagram

HD74HCT620



HD74HCT623



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	–0.5 to V_{CC} +0.5	V
Input / Output diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_{OUT}	±35	mA
V_{CC}, GND current	I_{CC} or I_{GND}	±75	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to 85	°C	
Input rise / fall time[*1]	t_r, t_f	0 to 500	ns	V_{CC} = 4.5 V

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V_{IL}	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V_{OH}	4.5	4.4	—	—	4.4	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.18	—	—	4.13	—			I_{OH} = –6 mA
	V_{OL}	4.5	—	—	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	—	0.26	—	0.33			I_{OL} = 6 mA
Off-state output current	I_{OZ}	5.5	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	5.5	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	5.5	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 mA	

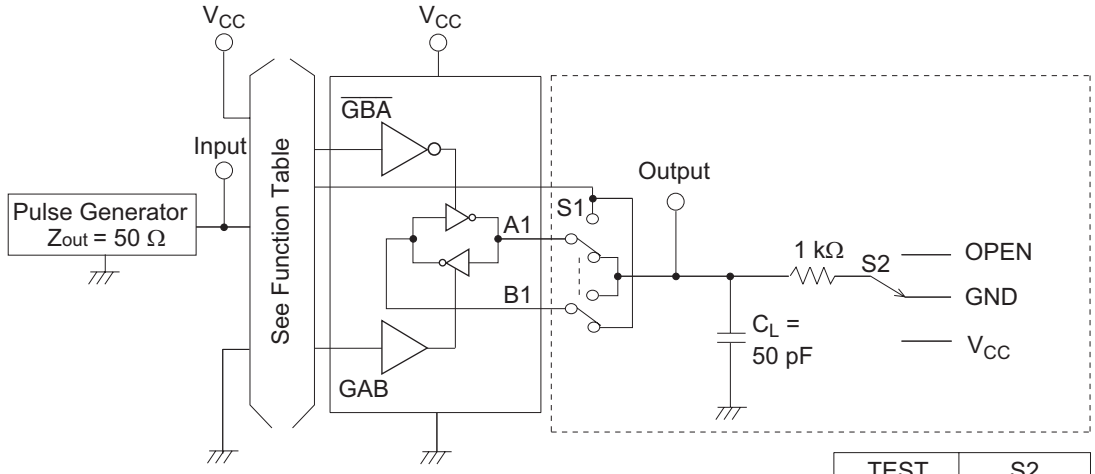
Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t_{PLH}	4.5	—	13	20	—	25	ns	
	t_{PHL}	4.5	—	16	20	—	25		
Output enable time	t_{ZH}	4.5	—	16	30	—	38	ns	
	t_{ZL}	4.5	—	16	30	—	38		
Output disable time	t_{HZ}	4.5	—	19	30	—	38	ns	
	t_{LZ}	4.5	—	21	30	—	38		
Output rise/fall time	t_{TLH} t_{THL}	4.5	—	4	12	—	15	ns	
Input capacitance	Cin	—	—	5	10	—	10	pF	

Test Circuit

HD74HCT620



TEST	S2
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	V_{CC}

Note : 1. C_L includes probe and jig capacitance.
2. A2–B2, A3–B3, A4–B4, A5–B5, A6–B6, A7–B7, A8–B8 are identical to above load circuit.
3. S1 is a input / output swich.

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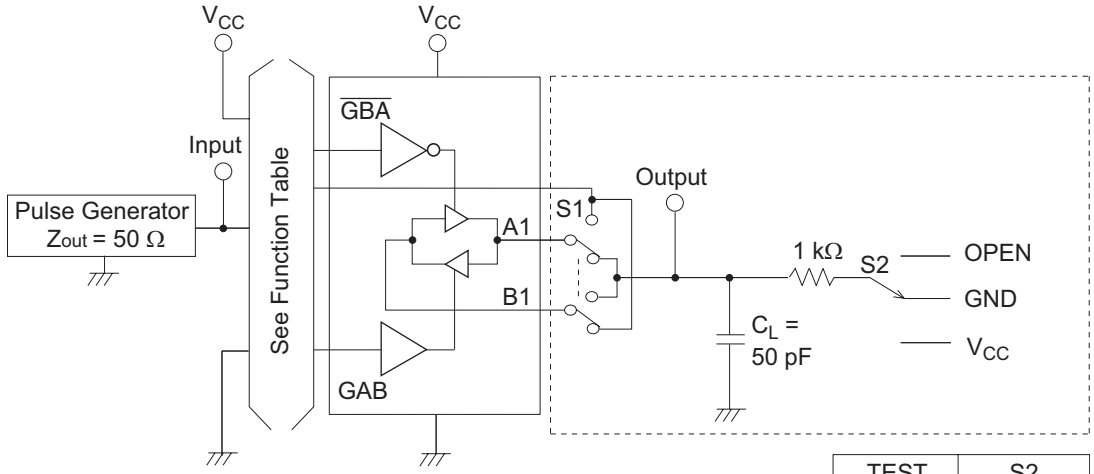

TEST	S2
t_{PLH} / t_{PHL}	OPEN
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t_{ZL} / t_{LZ}	V_{CC}

Note : 1. C_L includes probe and jig capacitance.
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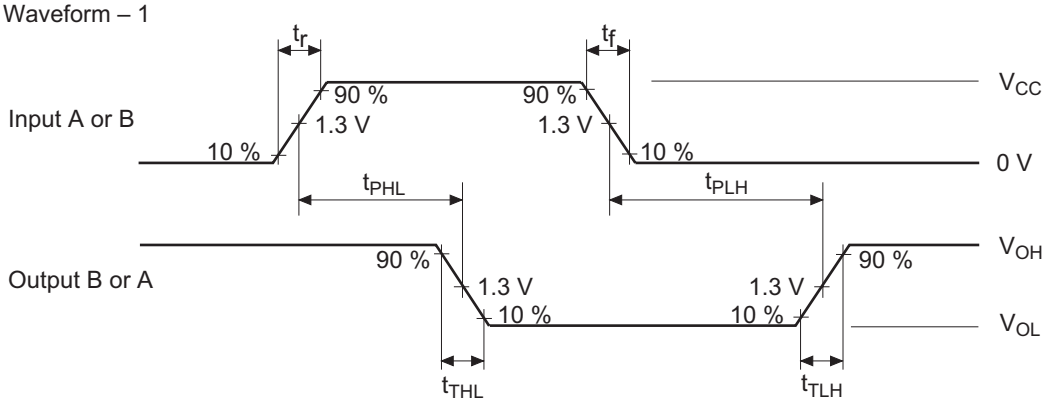
Waveforms

HD74HCT620

• Waveform – 1



Notes : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t_r ≤ 6 ns, t_f ≤ 6 ns
2. The output are measured one at a time with one transition per measurement.

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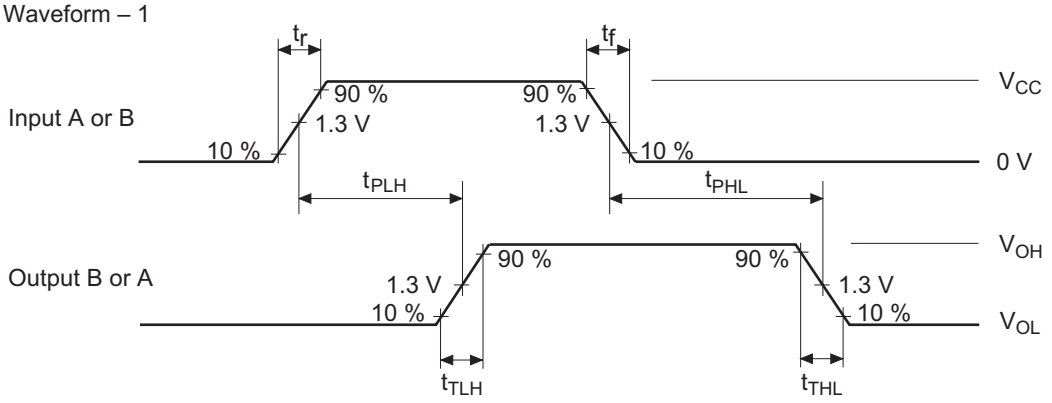
• Waveform – 1



Notes : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t_r ≤ 6 ns, t_f ≤ 6 ns
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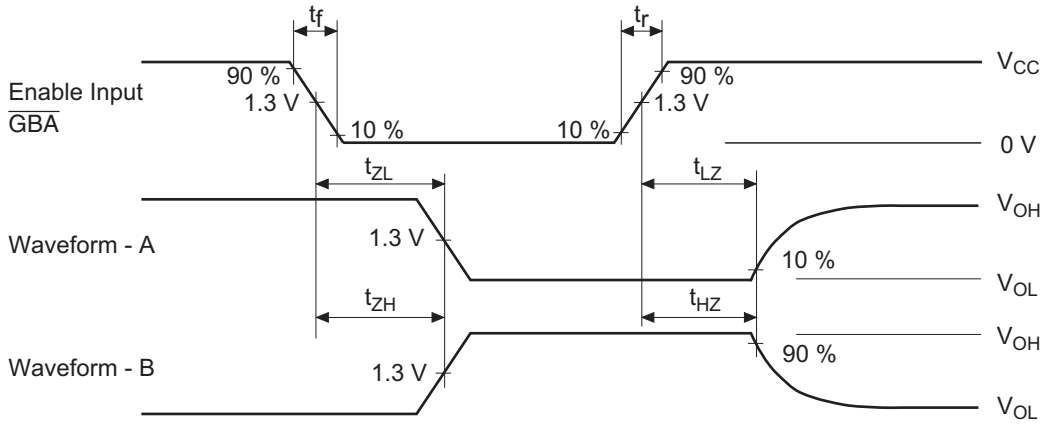
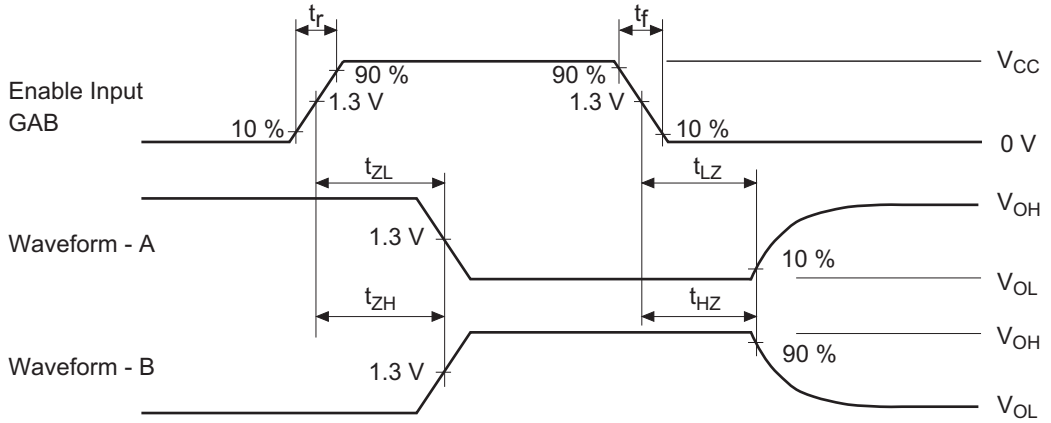
• Waveform – 2



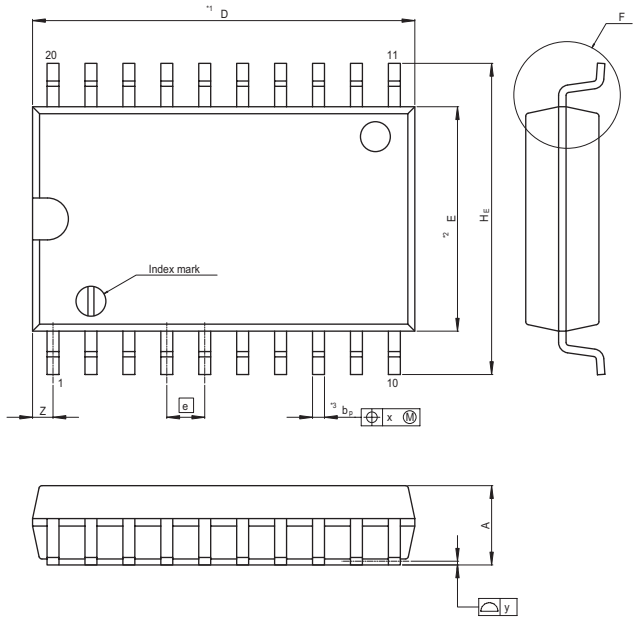
• Waveform – 3

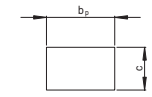


Notes : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns
2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

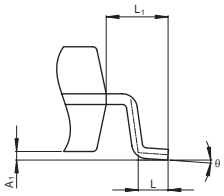
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-7.5x12.8-1.27	PRSP0020DC-A	FP-20DBV	0.52g





Terminal cross section
(Ni/Pd/Au plating)

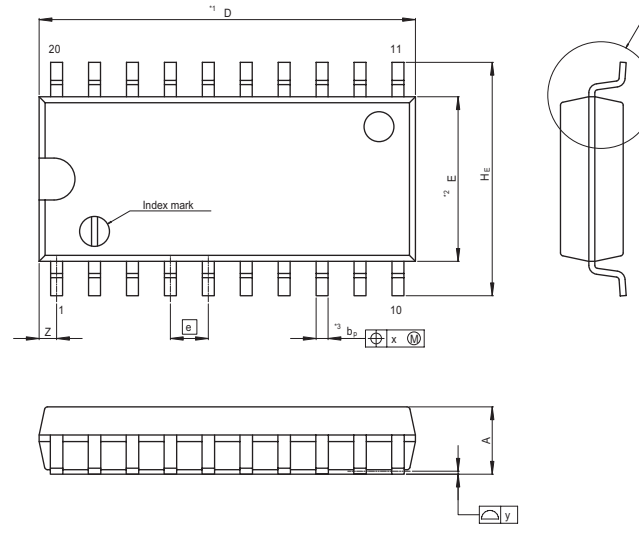


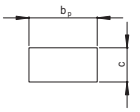
Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   @ DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   @ INCLUDE TRIM OFFSET.

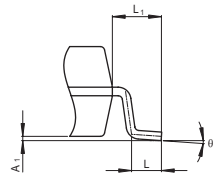
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.80	13.2
E	—	7.50	—
A_2	—	—	—
A_1	0.10	0.20	0.30
A	—	—	2.65
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.20	0.25	0.30
c_1	—	—	—
θ	0°	—	8°
H_E	10.00	10.40	10.65
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.935
L	0.40	0.70	1.27
L_1	—	1.45	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g





Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

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