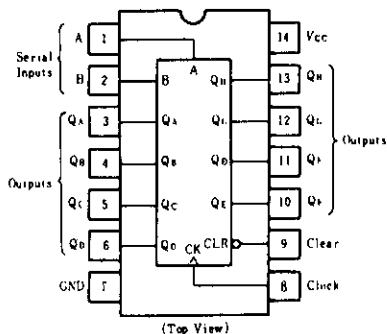


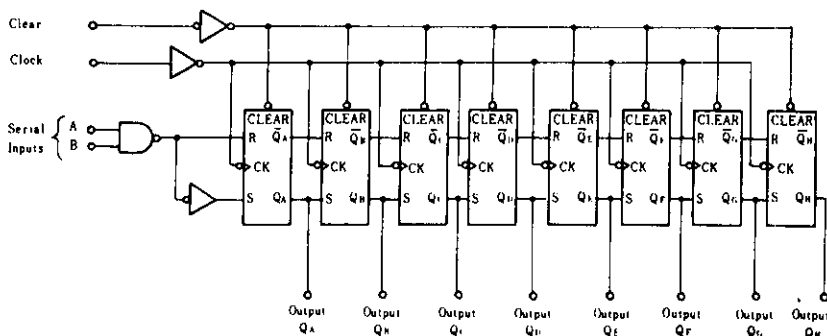
HD74LS164 ● 8-Bit Parallel-Out Serial-In Shift Registers

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ FUNCTION TABLE

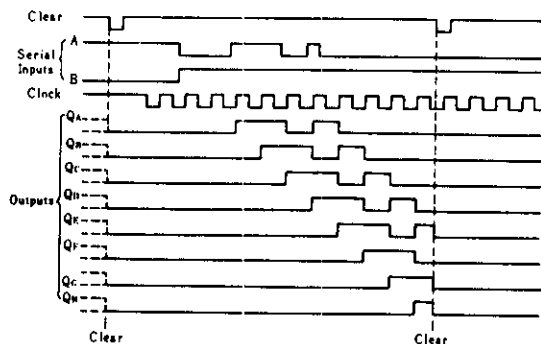
Inputs				Outputs			
Clear	Clock	A	B	QA	QB	...	QH
L	X	X	X	L	L		L
H	L	X	X	QA0	QB0		QH0
H	↑	H	H	H	QA _n		QG _n
H	↑	L	X	L	QA _n		QG _n
H	↑	X	L	L	QA _n		QG _n

- Notes) 1. H; high level, L; low level, X; irrelevant
 2. ↑; transition from low to high level
 3. QA₀, QB₀, QH₀; the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
 4. QA_n, QG_n; the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_{CK(CK)}$	20	—	—	ns
Clear pulse width	$t_{CLR(CLR)}$	20	—	—	ns
Data setup time	t_{su}	15	—	—	ns
Data hold time	t_h	5	—	—	ns

■ TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



HD74LS164

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0		—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}$				
					0.4	V
					0.5	V
Input current	I_{IH}	$V_{CC} = 5.25\text{V}, V_I = 2.7\text{V}$	—	—	20	μA
	I_{IL}	$V_{CC} = 5.25\text{V}, V_I = 0.4\text{V}$	—	—	0.4	mA
	I_I	$V_{CC} = 5.25\text{V}, V_I = 7\text{V}$	—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.25\text{V}$	—20	—	100	mA
Supply current**	I_{CC}	$V_{CC} = 5.25\text{V}$	—	16	27	mA
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}, I_{IK} = -18\text{mA}$	—	—	1.5	V

* $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

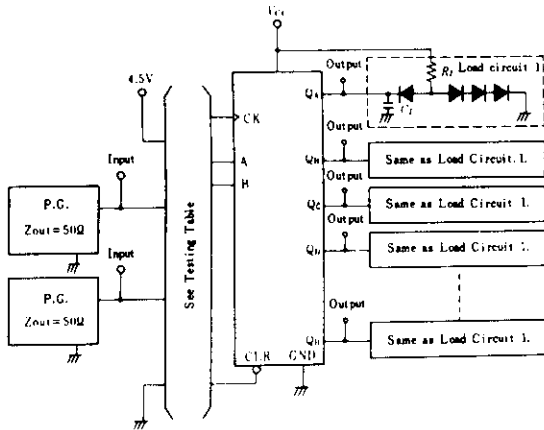
** I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary grounded, then 4.5V applied to clear.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}				25	36	—	MHz
Propagation delay time	t_{PHL}	Clear	Q	$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$	—	24	36	ns
	t_{PLH}	Clock	Q		—	17	27	ns
	t_{PHL}	Clock	Q		—	21	32	ns

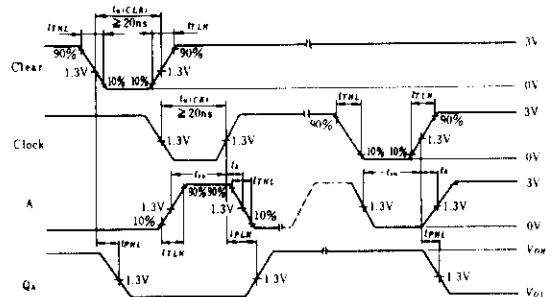
TESTING METHOD

1) Test Circuit



- Notes) 1. Input pulse: $t_{TLH} \leq 15\text{ns}, t_{THL} \leq 6\text{ns}, PRR = 1\text{MHz}$,
 (Clock, Clear), $PRR = 500\text{kHz}$ (A or B)
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074 (E)

Waveform



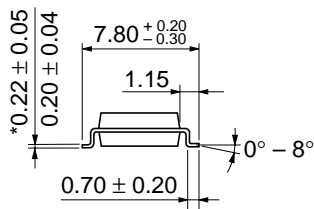
Notes) Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the timing chart.

2) Testing Table

Item	From input to output	Inputs				Outputs							
		CLR	CK	A	B	Q_A	Q_H	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H
f_{max}		4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PLH}	Clear → Q	IN	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PHL}	CK → Q	4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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