To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS174 / HD74LS175

Hex / Quadruple D-type Flip-Flops (with clear)

REJ03D0451–0300
Rev.3.00
Jul.15.2005

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the HD74LS175 features complementary outputs from each flip-flops. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the outputs.

Features

- Ordering Information

• HD74LS174

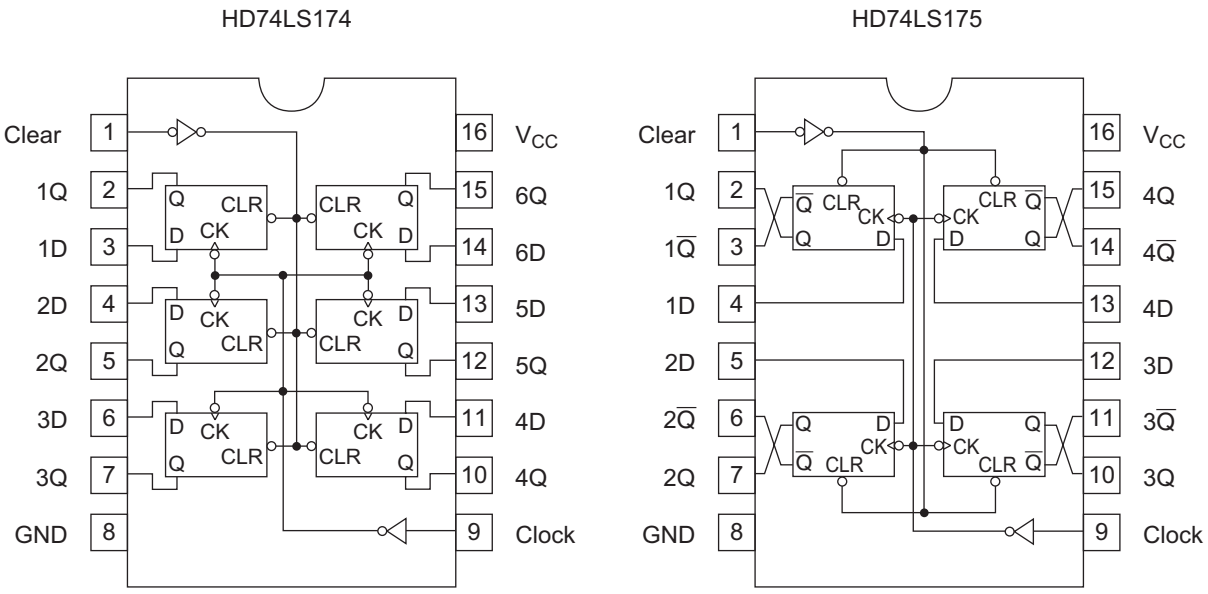
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS174P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS174FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS174RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

• HD74LS175

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS175P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS175FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS175RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

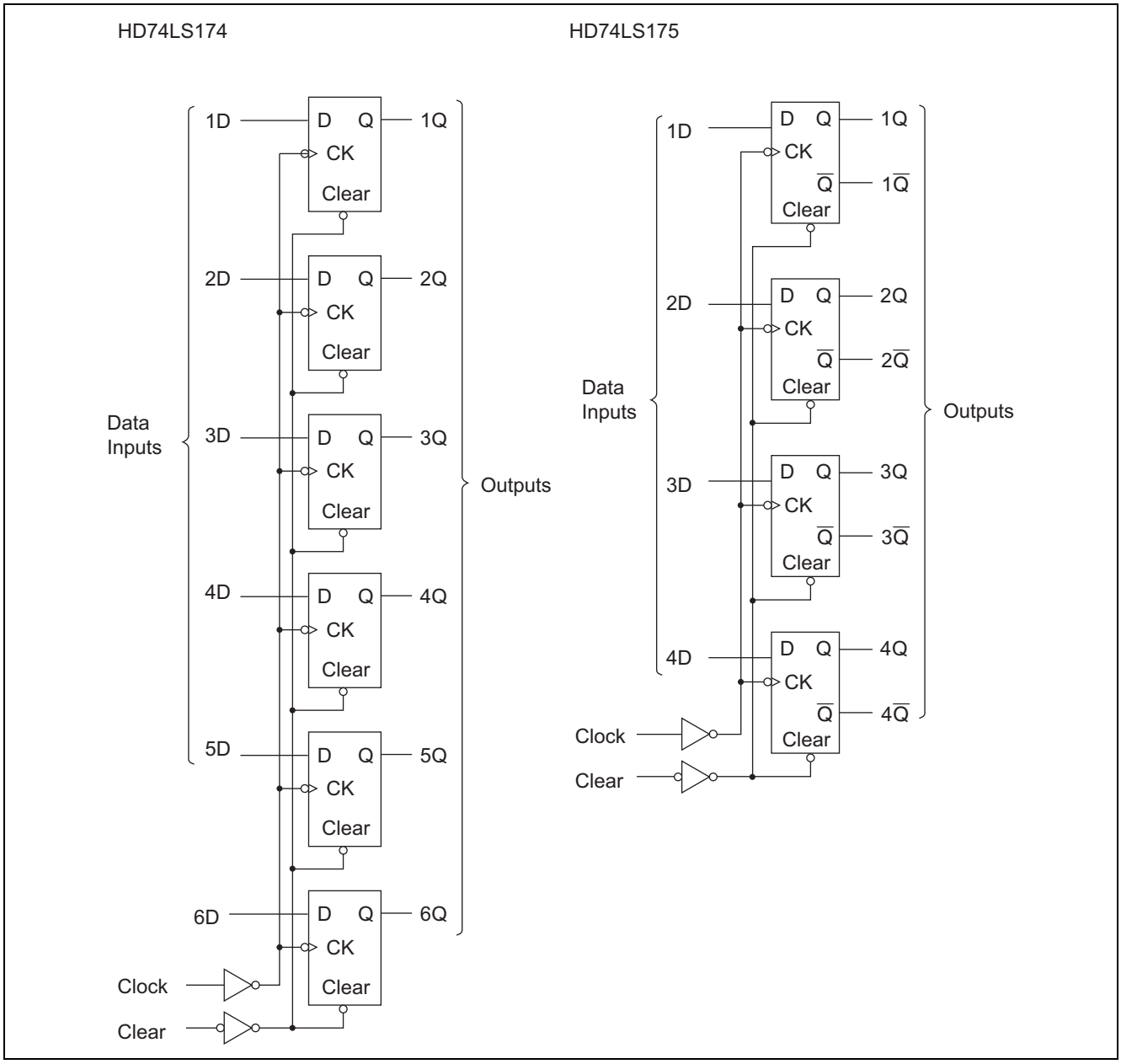


Function Table

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes: 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. Q_0; the level of Q before the indicated steady-state input conditions were established.
4. $\overline{Q}$ is applied to HD74LS175 only.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

• **HD74LS174**

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Clock frequency		f_{clock}	0	—	30	MHz
Clock pulse width		$t_{w\ (CK)}$	20	—	—	ns
Clear pulse width		$t_{w\ (CLR)}$	20	—	—	ns
Setup time	Data input	$t_{su\ (data)}$	20	—	—	ns
	Clear inactive-state	$t_{su\ (CLR)}$	25	—	—	ns
Data hold time		$t_{h\ (data)}$	5	—	—	ns

• **HD74LS175**

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Clock frequency		f_{clock}	0	—	30	MHz
Clock pulse width		$t_{w\ (CK)}$	20	—	—	ns
Clear pulse width		$t_{w\ (CLR)}$	20	—	—	ns
Setup time	Data input	$t_{su\ (data)}$	20	—	—	ns
	Clear inactive-state	$t_{su\ (CLR)}$	25	—	—	ns
Data hold time		$t_{h\ (data)}$	5	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.4		I_{OL} = 4 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**	I_{CC}	—	16	26	mA	HD74LS174, V_{CC} = 5.25 V
		—	11	18		HD74LS175, V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** With all outputs open and 4.5 V applied to all data and cleat inputs, I_{CC} is measured after a momentary grounded, then 4.5 V, is applied to clock.

Switching Characteristics

• **HD74LS174**

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q	30	40	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PHL}	Clear	Q	—	23	35	ns	
	t_{PLH}	Clock	Q	—	20	30		
	t_{PHL}	Clock	Q	—	21	30		

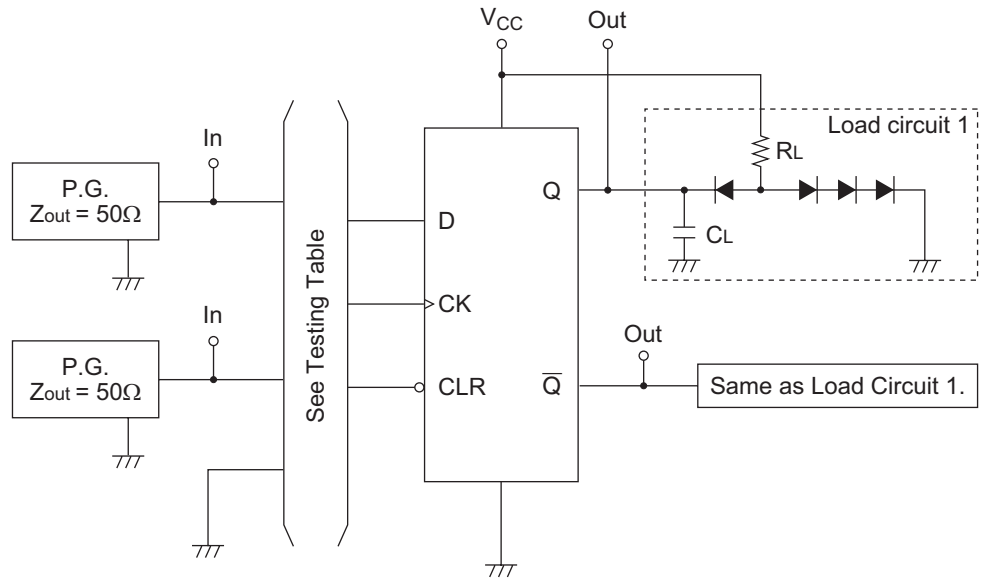
• **HD74LS175**

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q, $\overline{Q}$	30	40	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clear	$\overline{Q}$	—	16	25	ns	
	t_{PHL}		Q	—	20	30		
	t_{PLH}	Clock	Q, $\overline{Q}$	—	13	25		
	t_{PHL}	Clock	Q, $\overline{Q}$	—	16	25		

Testing Method

Test Circuit



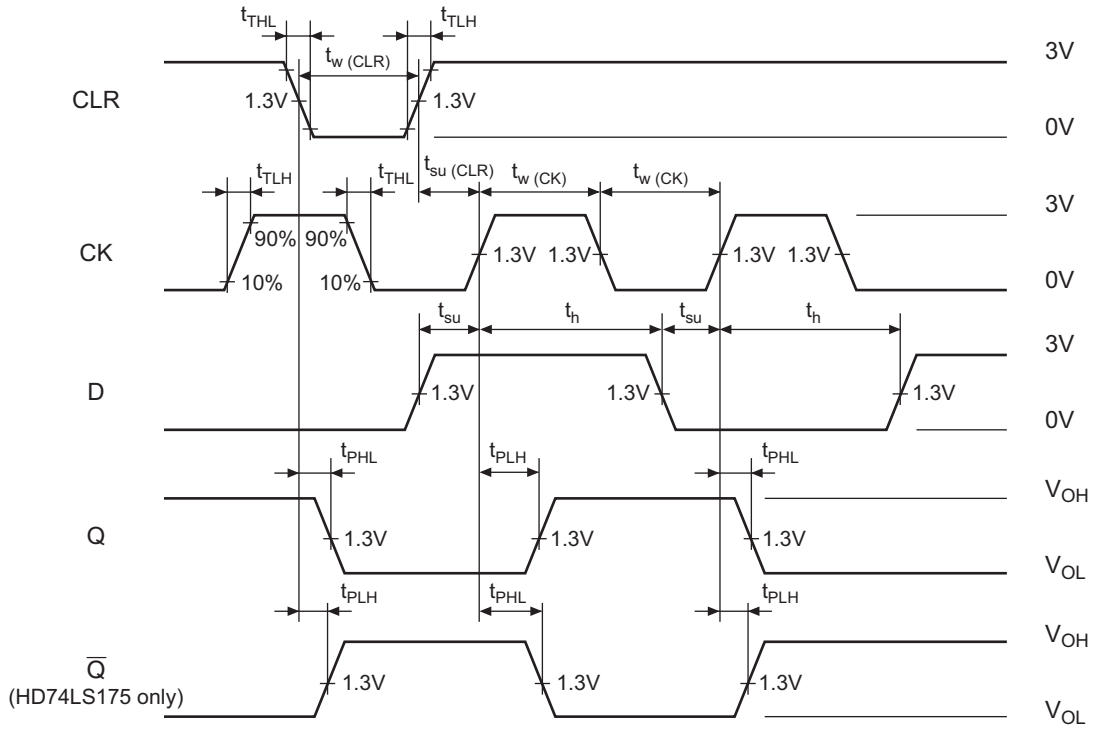
Notes: 1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

Testing Table

Item	From input to output	Inputs			Outputs	
		CLR	CK	D	Q	$\overline{Q}$
f_{max}	CK→Q, $\overline{Q}$*	4.5 V	IN	IN	OUT	OUT
t_{PLH}	CK→Q, $\overline{Q}$*	4.5 V	IN	IN		
t_{PHL}	CLR→Q, $\overline{Q}$*	IN	IN	4.5 V		

Note: *. HD74LS175 only

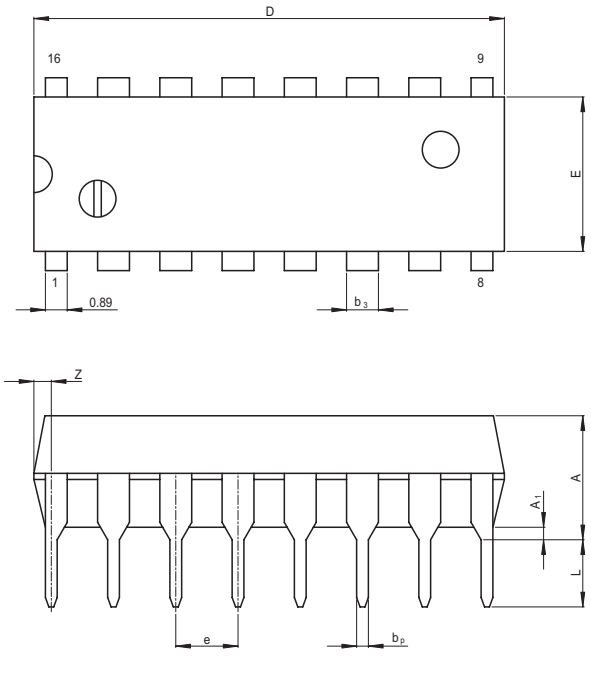
Waveform



Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, and: for f_{max}, $t_{TLH} = t_{THL} \leq 2.5$ ns.

Package Dimensions

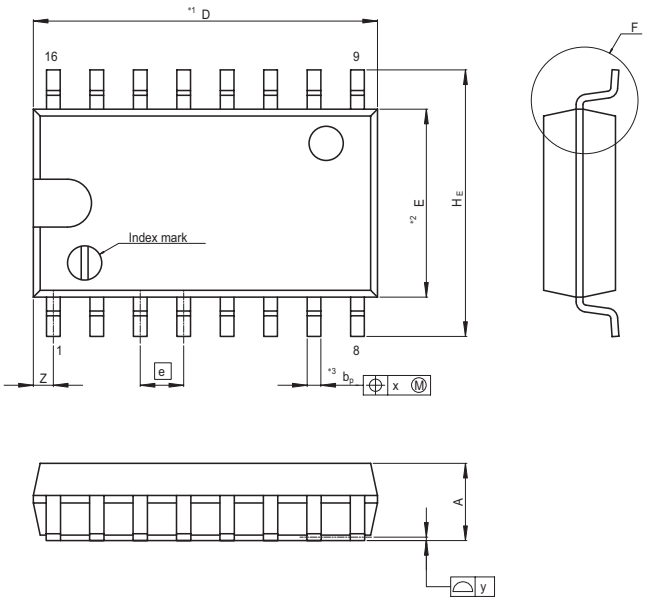
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g

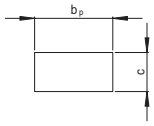


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

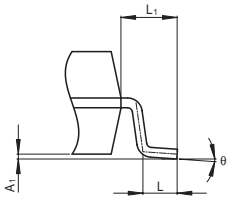
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.





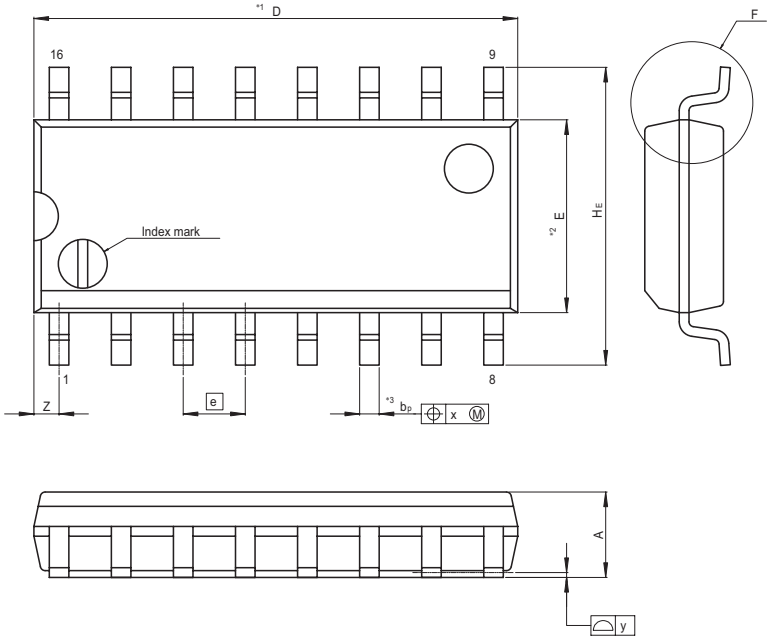
Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g



NOTE)
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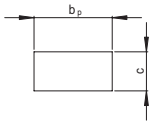
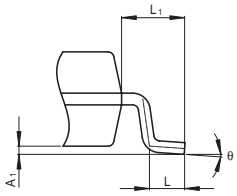
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	9.90	10.30
E	——	3.95	——
A_2	——	——	——
A_1	0.10	0.14	0.25
A	——	——	1.75
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.15
Z	——	——	0.635
L	0.40	0.60	1.27
L_1	——	1.08	——

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