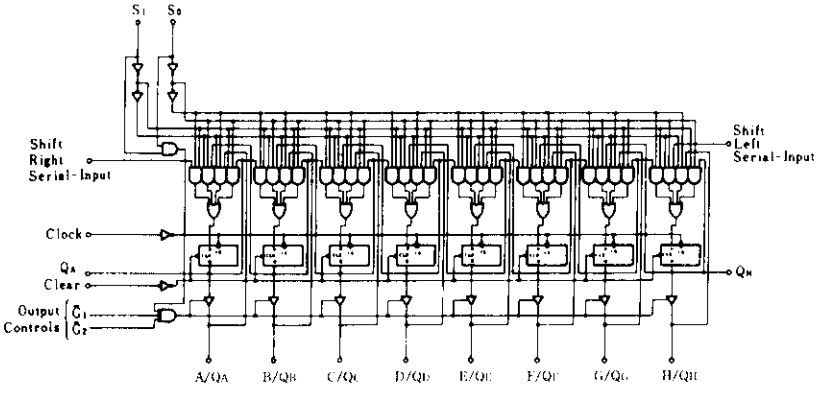
HD74LS299 ●8-bit Universal Shift/Storage Registers (with three-state outputs)

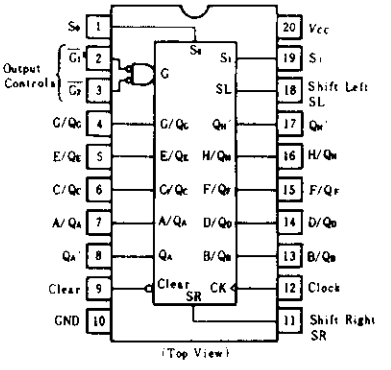
This eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function select lines, S_0 and S_1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	7.0	V
Output voltage (off-state)	$V_{O(off)}$	5.5	V
Operating temperature range	T_{opr}	−20~+75	°C
Storage temperature range	T_{stg}	−65~+150	°C

■FUNCTION TABLE

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S_1	S_0	$\overline{G_1}$ ↑	$\overline{G_2}$ ↑		S_L	S_R										
Clear	L	×	L	L	L	×	×	×	L	L	L	L	L	L	L	L	L	L
	L	L	×	L	L	×	×	×	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	×	×	L	L	L	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	×	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	×	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	×	×	↑	×	×	a	b	c	d	e	f	g	h	a	h

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a~h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.
4. Q_{A0}~Q_{H0}; the level of Q_A through Q_H, respectively, before the indicated steady-state input conditions were established.
5. Q_{An}~Q_{Hn}; the level of Q_A through Q_H, respectively, before the most-recent ↑ transition of the clock.
6. ↑ =; When one or both output controls are high the eight input/output terminals are desabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Output current	Q_A~Q_H	I_{OH}	—	—	−2.6	mA
	Q_A' or Q_H'		—	—	−0.4	
Output current	Q_A~Q_H	I_{OL}	—	—	24	mA
	Q_A' or Q_H'		—	—	8	
Clock frequency		f_{clock}	0	—	25	MHz
Clock pulse width	Clock high	$t_{w(CK)}$	30	—	—	ns
	Clock low		10	—	—	
Clear pulse width	Clear low	$t_{w(CLR)}$	20	—	—	ns
Setup time	Select	t_{su}	35 ↑	—	—	ns
	High-level data		20 ↑	—	—	
	Low-level data		20 ↑	—	—	
	Clear inactive-state		20 ↑	—	—	
Hold time	Select	t_h	10 ↑	—	—	ns
	Data		10 ↑	—	—	

↑ The arrow indicates the rising edge.

■ELECTRICAL CHARACTERISTICS (Ta=−20~+75°C)

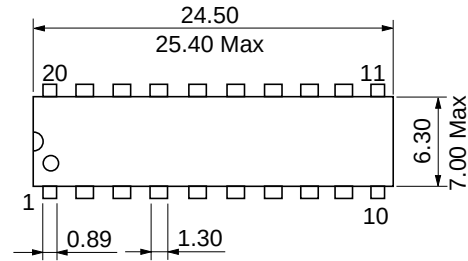
Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	—	—	V
		V_{IL}			—	—	0.8	V
Output voltage	Q_A thru Q_H	V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OH}=−2.6mA	2.4	—	—	V
	Q_A' or Q_H'			I_{OH}=−400μA	2.7	—	—	
	Q_A thru Q_H	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=12mA	—	—	0.4	V
				I_{OL}=24mA	—	—	0.5	
	Q_A' or Q_H'			I_{OL}=4mA	—	—	0.4	
				I_{OL}=8mA	—	—	0.5	
Output current	Q_A thru Q_H	I_{OZH}	V_{CC}=5.25V, V_{IH}=2V, V_O=2.7V		—	—	40	μA
	Q_A thru Q_H	I_{OZL}	V_{CC}=5.25V, V_{IH}=2V, V_O=0.4V		—	—	−400	μA
Input current	S_0, S_1, A~H	I_{IH}	V_{CC}=5.25V, V_I=2.7V		—	—	40	μA
	Any other				—	—	20	
	S_0, S_1	I_{IL}	V_{CC}=5.25V, V_I=0.4V		—	—	−0.8	mA
	Any other				—	—	−0.4	
	S_0, S_1	I_I	V_{CC}=5.25V	V_I=7V	—	—	0.2	mA
	A~H			V_I=5.5V	—	—	0.1	
	Any other			V_I=7V	—	—	0.1	
Short-circuit output current	Q_A thru Q_H	I_{OS}	V_{CC}=5.25V		−30	—	−130	mA
	Q_A' or Q_H'				−20	—	−100	
Supply current		I_{CC}	V_{CC}=5.25V		—	33	53	mA
Input clamp voltage		V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		—	—	−1.5	V

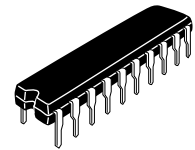
* V_{CC} = 5V, Ta = 25°C

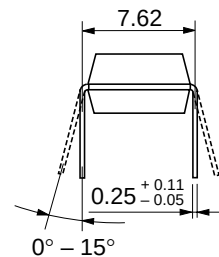
■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			C_L=15pF, R_L=2kΩ	25	35	—	MHz
Propagation delay time	t_{PLH}	Clock	Q_A' or Q_H'		—	22	33	ns
	t_{PHL}				—	26	39	
	t_{PHL}	Clear	Q_A' or Q_H'		—	27	40	
	t_{PLH}	Clock	Q_A~Q_H	C_L=45pF, R_L=665Ω	—	17	25	ns
	t_{PHL}				—	26	39	
	t_{PHL}	Clear	Q_A~Q_H		—	26	40	ns
Output enable time	t_{ZH}	$\overline{G}_1$, $\overline{G}_2$	Q_A~Q_H		—	13	21	ns
	t_{ZL}				—	19	30	
Output disable time	t_{HZ}	$\overline{G}_1$, $\overline{G}_2$	Q_A~Q_H	C_L=5pF, R_L=665Ω	—	10	15	ns
	t_{LZ}				—	10	15	

Unit: mm

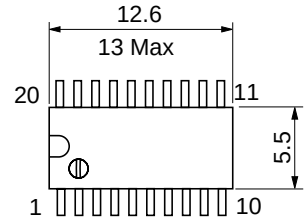


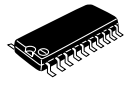


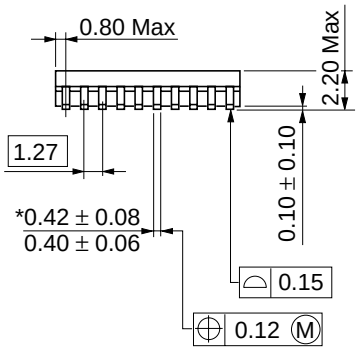


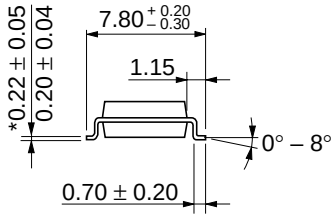
Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g

Unit: mm





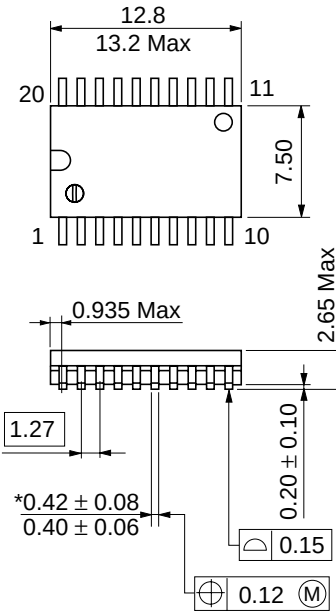


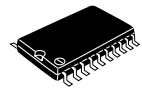


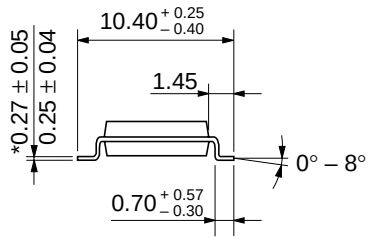
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX