

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74LS374

## Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

REJ03D0483-0200

Rev.2.00

Feb.18.2005

The HD74LS374, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

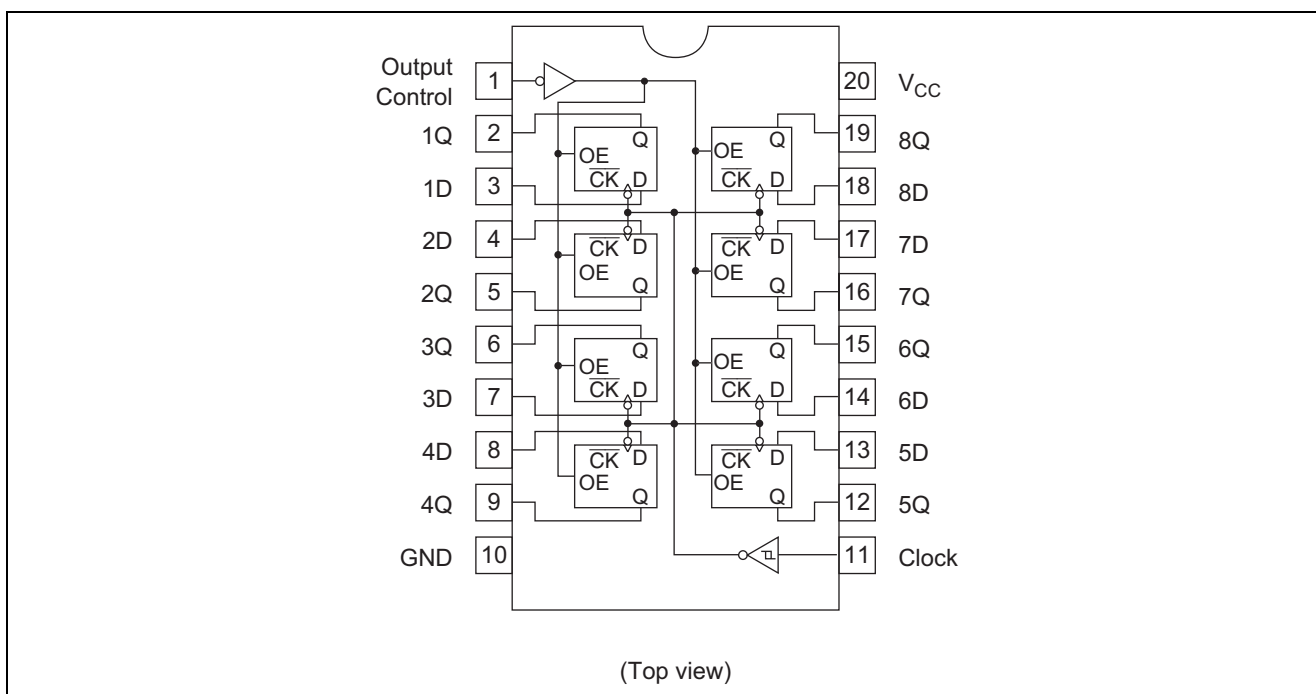
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS374P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS374FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS374RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement

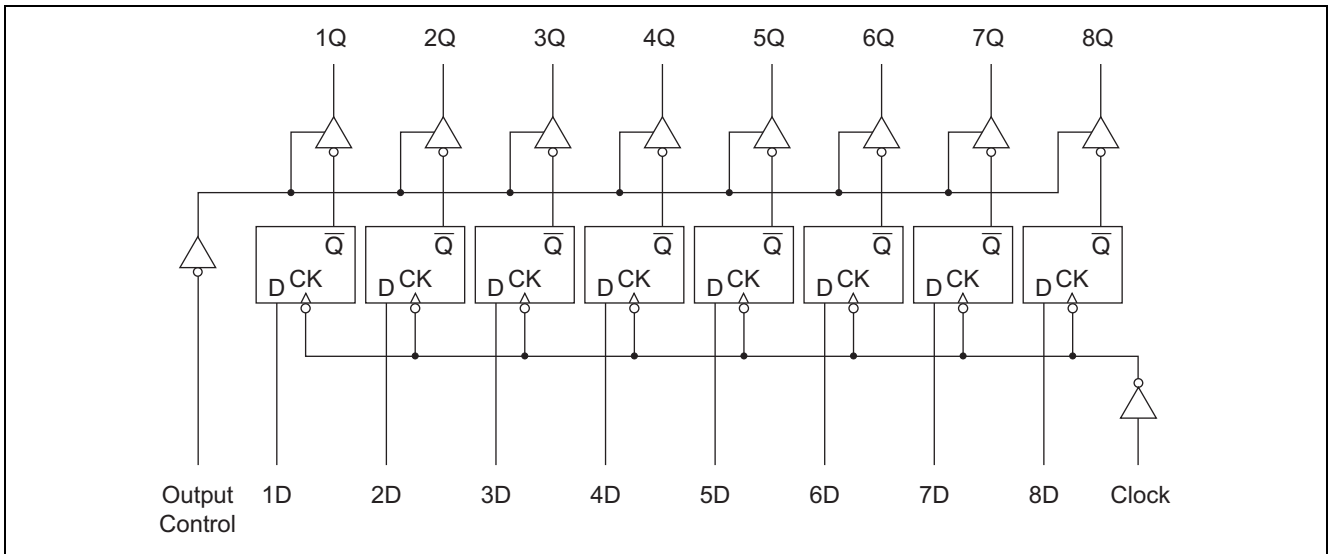


**Function Table**

Inputs		Outputs
Output control	Clock	Q
L	↑	H
L	↑	L
L	L	Q <sub>0</sub>
H	X	Z

Notes: H; high level, L; low level, X; irrelevant  
 ↑; transition from low to high level  
 Q<sub>0</sub>; level of Q before the indicated steady state input conditions were established  
 Z; off (high-impedance) state of a three state output

**Block Diagram**



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage	V <sub>OH</sub>	—	—	5.5	V
Output current	I <sub>OH</sub>	—	—	-2.6	mA
	I <sub>OL</sub>	—	—	24	mA
Operating temperature	T <sub>opr</sub>	-20	25	75	°C
Clock pulse width	t <sub>w</sub>	"H" Level	15	—	ns
		"L" Level	15	—	ns
Data setup time	t <sub>su</sub>	20↑	—	—	ns
Data hold time	t <sub>h</sub>	0↑	—	—	ns

## Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.8	V	
Output voltage	V <sub>OH</sub>	2.4	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -2.6 mA
	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 12 mA
—		—	0.5	I <sub>OL</sub> = 24 mA		V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
Output current	I <sub>OZH</sub>	—	—	20	μA	V <sub>O</sub> = 2.7 V
	I <sub>OZL</sub>	—	—	-20		V <sub>O</sub> = 0.4 V
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
Short-circuit output current	I <sub>OS</sub>	-30	—	-130	mA	V <sub>CC</sub> = 5.25 V
Supply current	I <sub>CC</sub>	—	27	40	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 4.5 V (Output control)
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Note: \* V<sub>CC</sub> = 5 V, Ta = 25°C

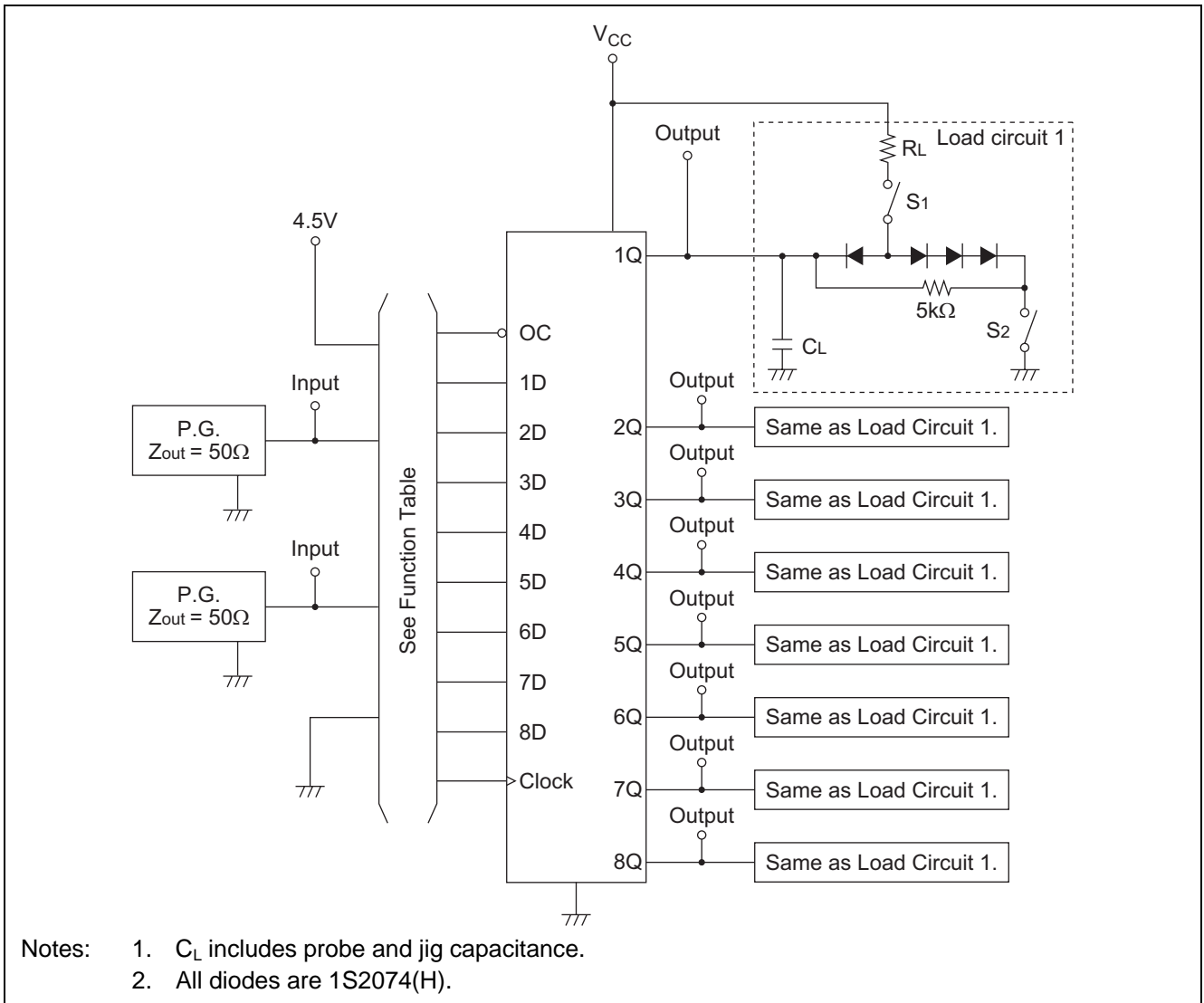
## Switching Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C)

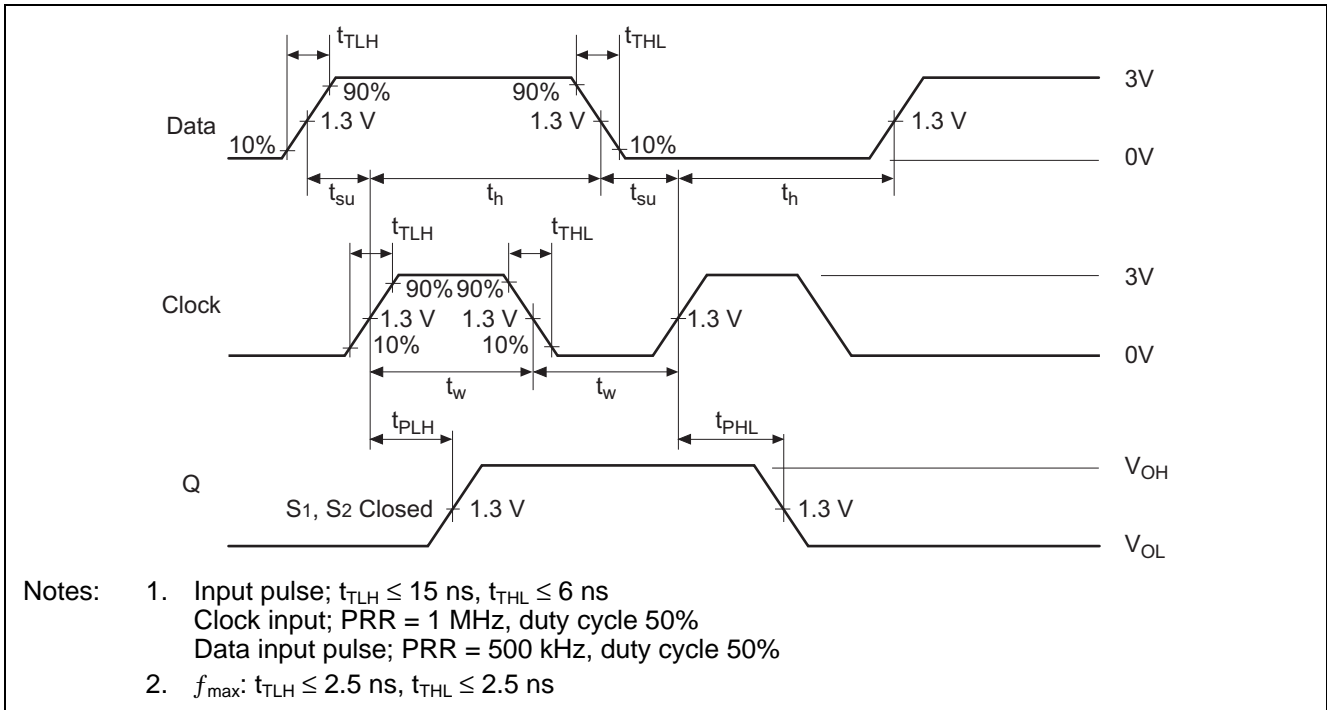
Item	Symbol	Inputs	Output	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>	Clock	Q	35	50	—	MHz	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
Propagation delay time	t <sub>PLH</sub>	Clock	Q	—	15	28	ns	
	t <sub>PHL</sub>			—	19	28		
Output enable time	t <sub>ZH</sub>	OC	Q	—	20	28		
	t <sub>ZL</sub>			—	21	28		
Output disable time	t <sub>HZ</sub>	OC	Q	—	12	20		
	t <sub>LZ</sub>			—	14	25		

## Testing Method

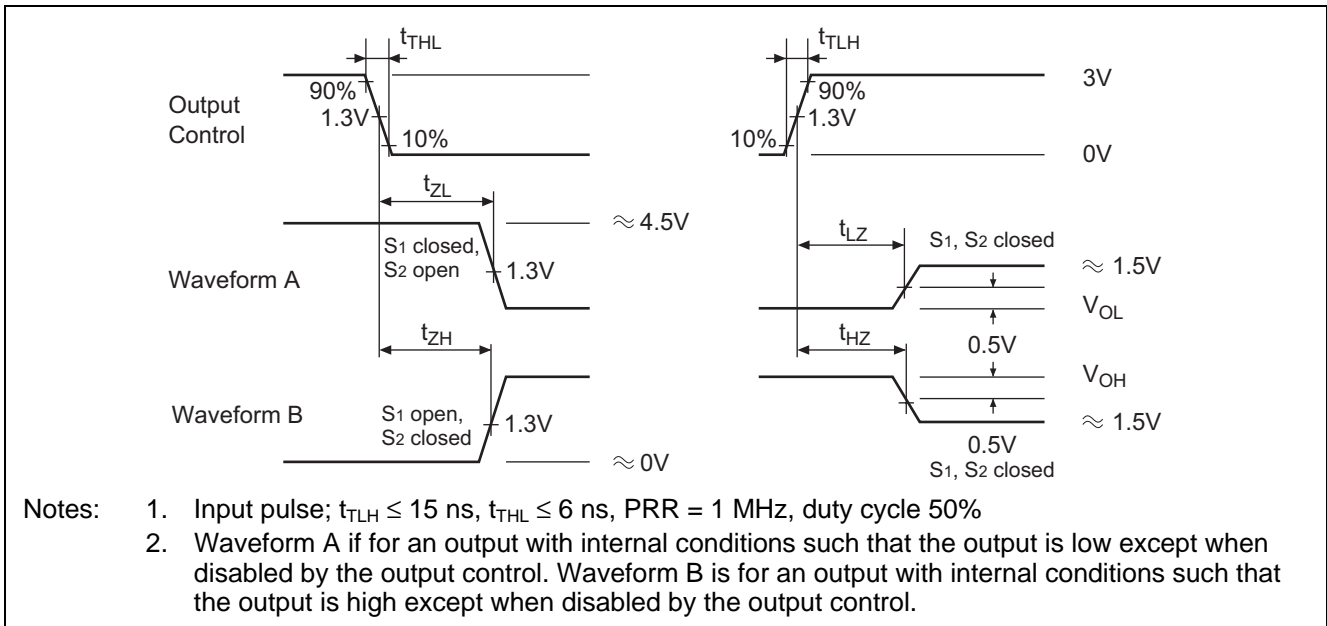
### Test Circuit



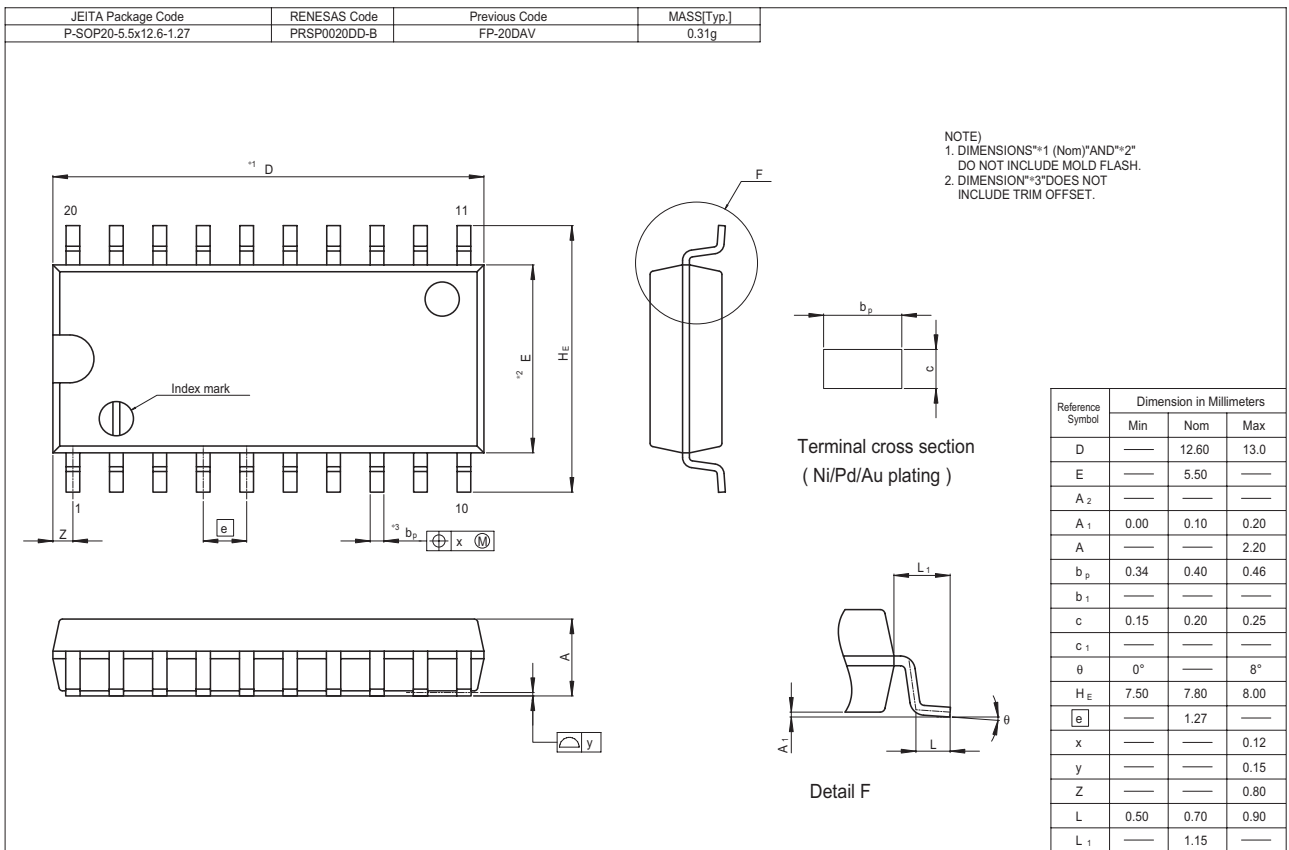
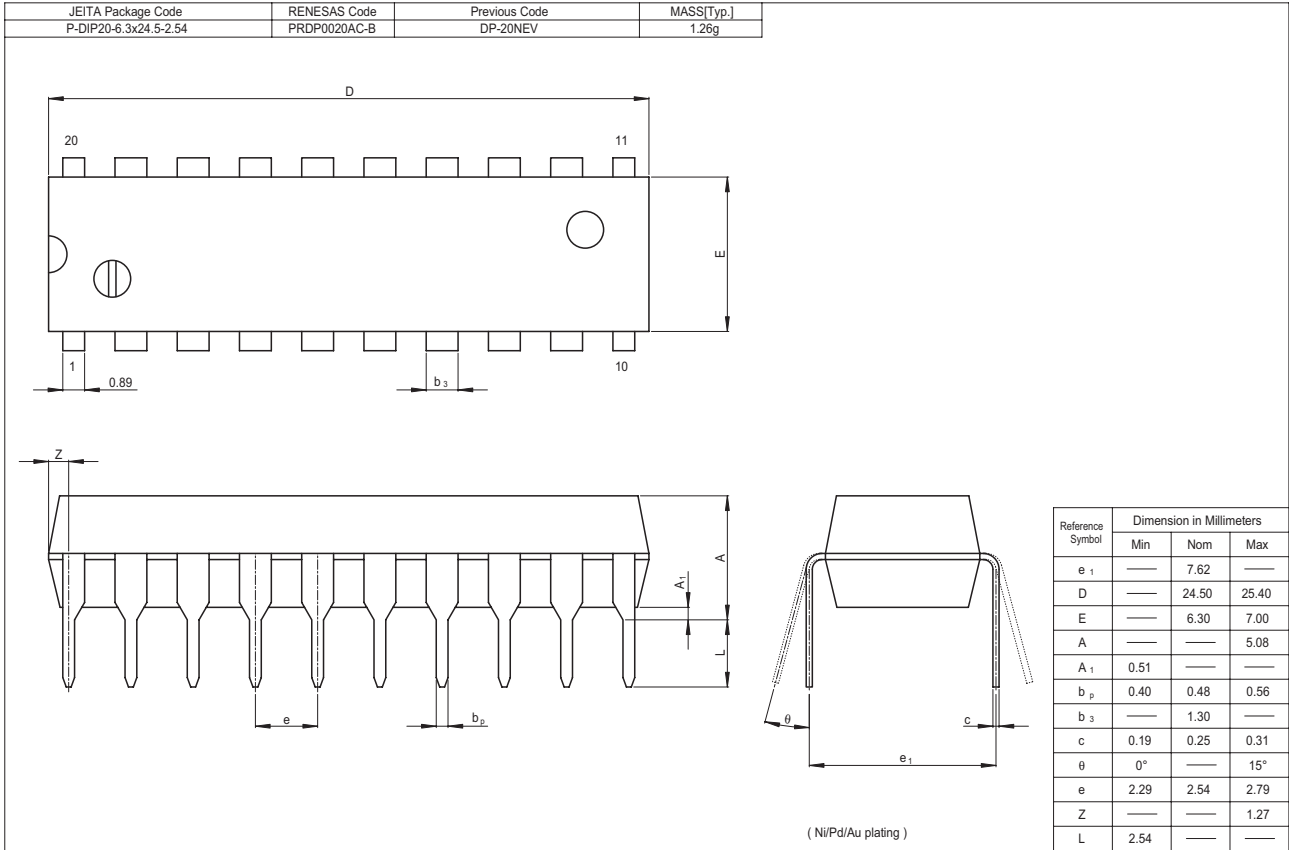
Waveforms 1



Waveforms 2



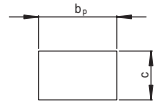
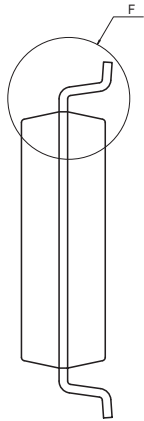
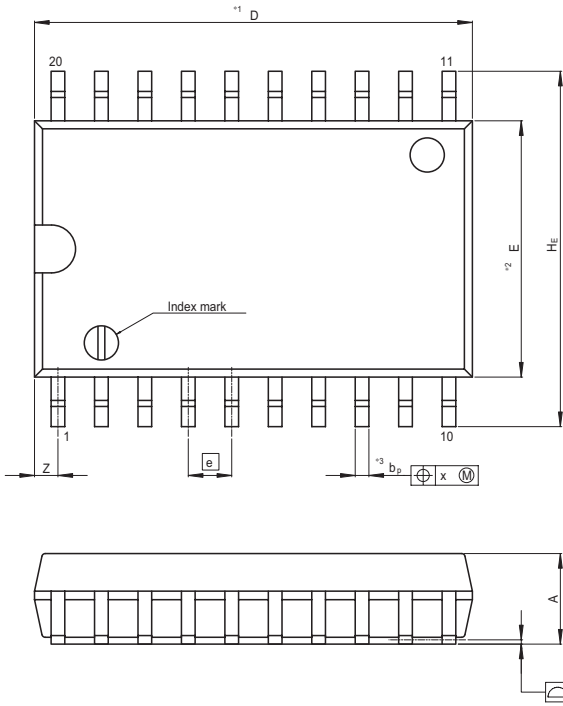
Package Dimensions



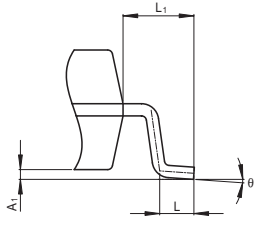


# HD74LS374

JEITA Package Code P-SOP20-7.5x12.8-1.27	RENESAS Code PRSP0020DC-A	Previous Code FP-20DBV	MASS[Typ.] 0.52g
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Terminal cross section  
( Ni/Pd/Au plating )



Detail F

NOTE)  
1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2\*  
@ DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION\*\*3\*DOES NOT  
@ INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.80	13.2
E	—	7.50	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.20	0.30
A	—	—	2.65
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.20	0.25	0.30
c <sub>1</sub>	—	—	—
θ	0°	—	8°
HE	10.00	10.40	10.65
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.935
L	0.40	0.70	1.27
L <sub>1</sub>	—	1.45	—

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