

HD74LVC16373A

16-bit D-type Transparent Latches with 3-state Outputs

REJ03D0366-0400Z
 (Previous ADE-205-121B (Z))
 Rev.4.00
 Jul. 29, 2004

Description

The HD74LVC16373A has sixteen D type latches with three state outputs in a 48 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input ($\overline{1G}$, $2\overline{G}$), all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs $V_{IH} (\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- All outputs $V_{OUT} (\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V or output off state})$
- Typical V_{OL} ground bounce $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C})$
- Typical V_{OH} undershoot $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C})$
- High output current $\pm 24\text{ mA} (@V_{CC} = 3.0\text{ V to }5.5\text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC16373ATEL	TSSOP-48 pin	TTP-48DBV	T	EL (1,000 pcs/reel)

Function Table

Inputs

\overline{G}	LE	D	Output Q
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	Q ₀

H: High level

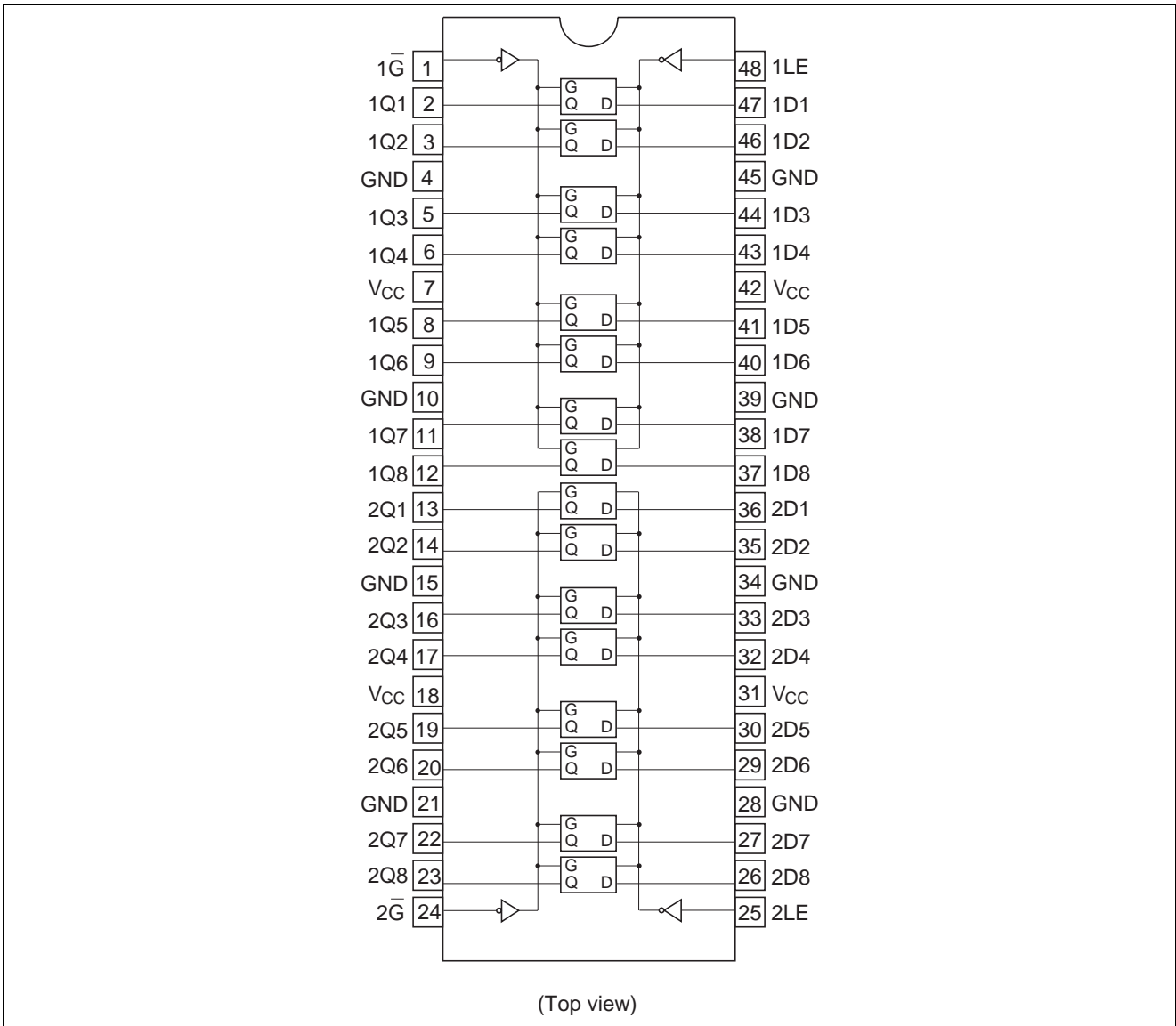
L: Low level

X: Immaterial

Z: High impedance

Q₀: Level of Q before the indicated steady input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 6.0	V	
Input diode current	I_{IK}	-50	mA	$V_I = -0.5\text{ V}$
Input voltage	V_I	-0.5 to 6.0	V	
Output diode current	I_{OK}	-50 50	mA	$V_O = -0.5\text{ V}$ $V_O = V_{CC} + 0.5\text{ V}$
Output voltage	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 6.0	V	Output "H" or "L" Output "Z" or $V_{CC}:OFF$
Output current	I_O	± 50	mA	
V_{CC} , GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5 2.0 to 5.5	V	Data hold At operation
Input / output voltage	V_I	0 to 5.5	V	\bar{G} , LE, D
	V_O	0 to V_{CC} 0 to 5.5	V	Output "H" or "L" Output "Z" or $V_{CC}:OFF$
Operating temperature	T_a	-40 to 85	$^{\circ}C$	
Output current	I_{OH}	-12 -24 ^{*2}	mA	$V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V to }5.5\text{ V}$
	I_{OL}	12 24 ^{*2}	mA	$V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V to }5.5\text{ V}$
Input rise / fall time ^{*1}	t_r, t_f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

2. Duty cycle $\leq 50\%$

Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V _{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V _{CC} ×0.7	—		
	V _{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V _{CC} ×0.3		
Output voltage	V _{OH}	2.7 to 5.5	V _{CC} -0.2	—	V	I _{OH} = -100 μA
		2.7	2.2	—		I _{OH} = -12 mA
		3.0	2.4	—		
		3.0	2.2	—		I _{OH} = -24 mA
		4.5	3.8	—		
	V _{OL}	2.7 to 5.5	—	0.2	V	I _{OL} = 100 μA
		2.7	—	0.4		I _{OL} = 12 mA
		3.0	—	0.55		I _{OL} = 24 mA
		3.0	—	0.55		
		4.5	—	0.55		
Input current	I _{IN}	0 to 5.5	—	±5.0	μA	V _{IN} = 5.5 V or GND
Off state output current	I _{OZ}	2.7 to 5.5	—	±5.0	μA	V _{IN} = V _{CC} , GND V _{OUT} = 5.5 V or GND
Output leak current	I _{OFF}	0	—	20	μA	V _{IN} / V _{OUT} = 5.5 V
Quiescent supply current	I _{CC}	2.7 to 3.6	—	±20	μA	V _{IN} / V _{OUT} = 3.6 to 5.5 V
		2.7 to 5.5	—	20		V _{IN} = V _{CC} or GND
	ΔI _{CC}	3.0 to 3.6	—	500	μA	V _{IN} = one input at (V _{CC} -0.6)V, other inputs at V _{CC} or GND

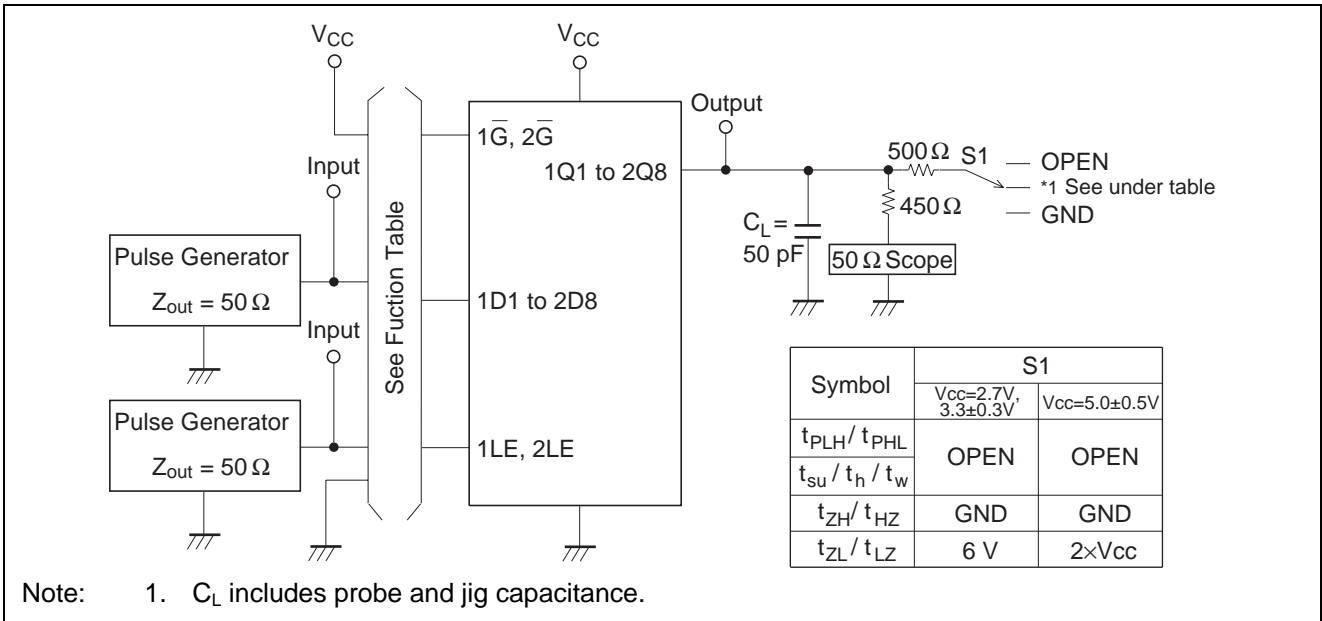
Switching Characteristics

Item	Symbol	V _{CC} (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t _{PLH}	2.7	—	—	7.7	ns	D	Q
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	—	—	5.5			
	t _{PHL}	2.7	—	—	8.0	ns	LE	Q
		3.3±0.3	2.0	—	7.0			
		5.0±0.5	—	—	5.5			
Output enable time	t _{ZH}	2.7	—	—	8.0	ns	Ḡ	Q̄
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	—	—	6.0			
Output disable time	t _{LZ}	2.7	—	—	8.0	ns	Ḡ	Q̄
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	—	—	6.0			
Setup time	t _{su}	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t _h	2.7	1.5	—	—	ns		
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t _w	2.7	3.0	—	—	ns		
		3.3±0.3	3.0	—	—			
		5.0±0.5	3.0	—	—			
Between output pins skew *1	t _{OSLH}	2.7	—	—	—	ns		
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C _{IN}	2.7	—	3.0	—	pF		
Output capacitance	C _O	2.7	—	15.0	—	pF		

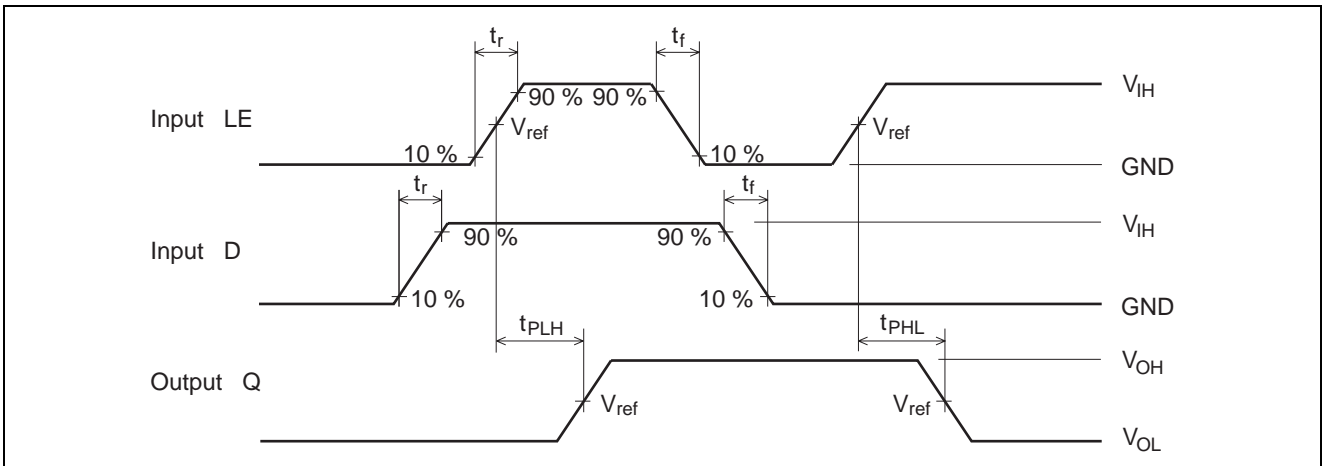
Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = | t_{PLHm} - t_{PLHn} |, t_{OSHL} = | t_{PHLm} - t_{PHLn} |$$

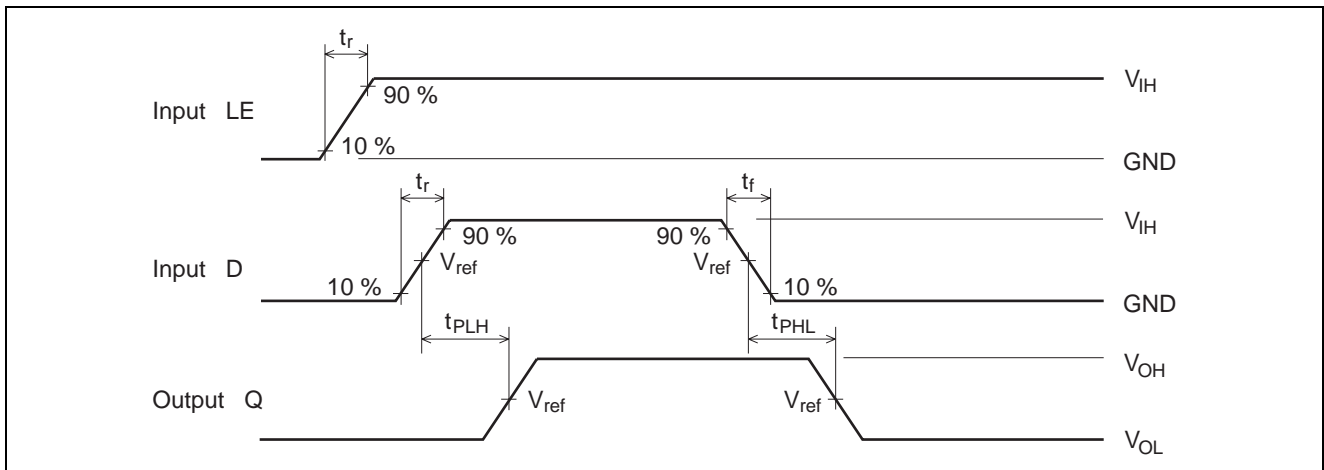
Test Circuit



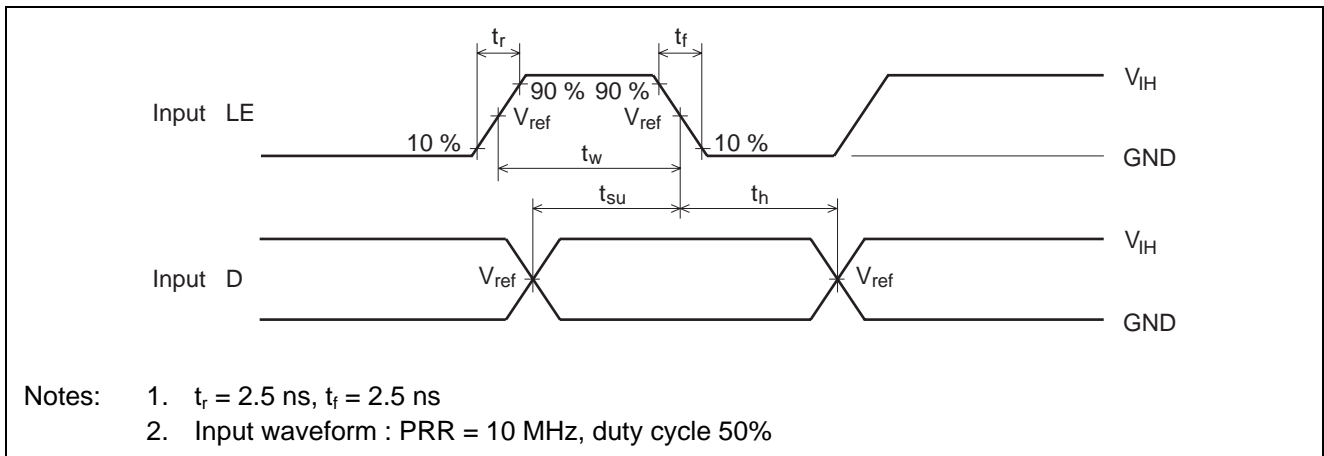
Waveforms – 1



Waveforms – 2

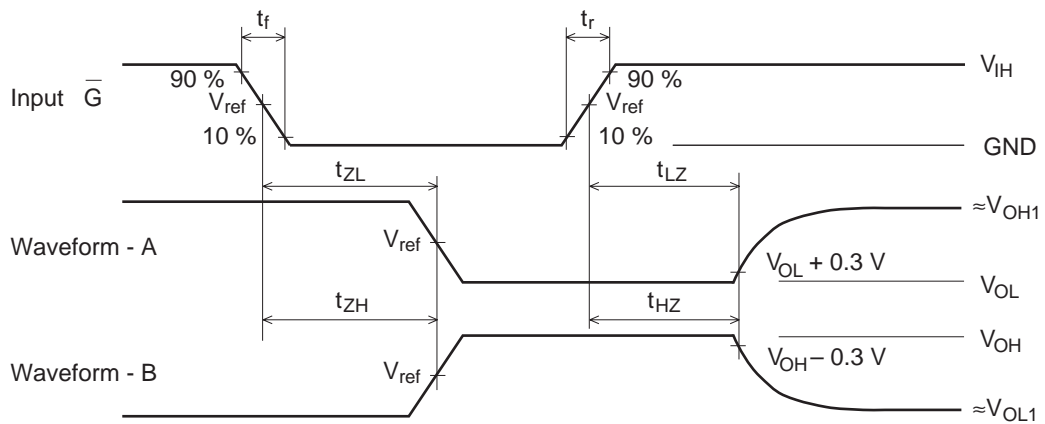


Waveforms – 3



- Notes:
1. $t_r = 2.5$ ns, $t_f = 2.5$ ns
 2. Input waveform : PRR = 10 MHz, duty cycle 50%

Waveforms – 4

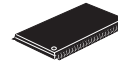
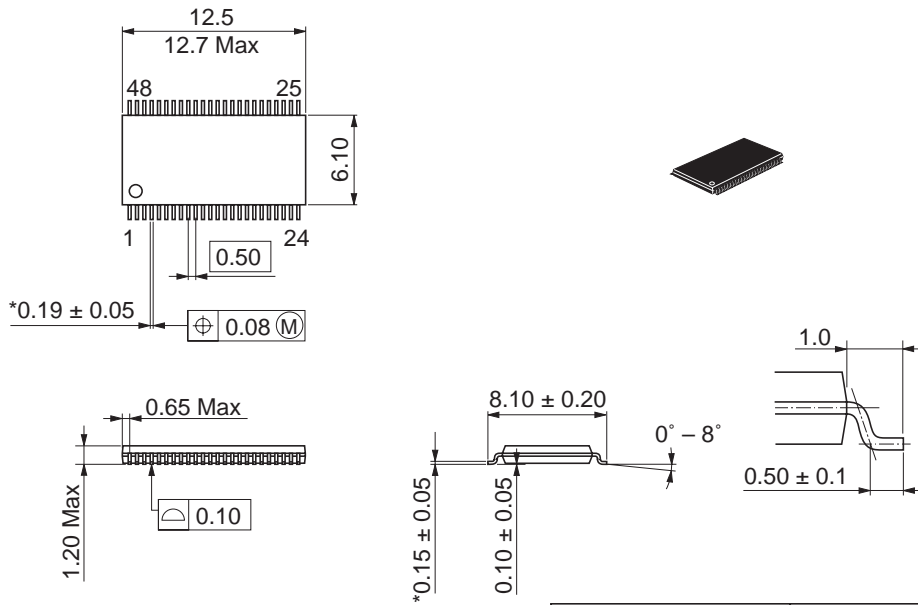


TEST	$V_{CC}=2.7V, 3.3\pm 0.3V$	$V_{CC}=5.0\pm 0.5V$
V_{IH}	2.7 V	V_{CC}
V_{ref}	1.5 V	50% V_{CC}
V_{OH1}	3 V	V_{CC}
V_{OL1}	GND	GND

- Notes:
1. $t_r = 2.5$ ns, $t_f = 2.5$ ns
 2. Input waveform : PRR = 10 MHz, duty cycle 50%
 3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
 4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

Package Dimensions

As of January, 2002
Unit: mm



*Pd plating

Package Code	TTP-48DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.20 g

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