BCD RATE MULTIPLIER

The HEF4527B is a BCD rate multiplier with two buffered rate outputs (O_1 and $\overline{O}_1$), two buffered terminal count outputs (TC and $\overline{TC}$), four BCD rate select inputs (S_A, S_B, S_C, S_D), a common clock input (CP), a preset input (PL), an overriding asynchronous clear input (CL), a strobe input (STR), a cascade input (CAS) and an active LOW count enable input ($\overline{CE}$).

The BCD rate multiplier provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD number, there will be six output pulses for every ten clock input pulses. The output is clocked on the negative-going transition of the clock.

When $\overline{CE}$, STR, CAS, CL and PL are LOW, the rate pulses are available at the outputs O_1 and $\overline{O}_1$, the terminal count pulses at TC and $\overline{TC}$.

A HIGH on CL resets the counter, independent of all other input conditions and a rate of 10 pulses is available at O_1 and $\overline{O}_1$ when S_D is HIGH. When $\overline{CE}$ is HIGH, the counter is disabled, the state of the outputs (O_1, $\overline{O}_1$) depend on the content of the counter.

A HIGH on PL sets the counter in the '9' state and TC becomes HIGH.

A HIGH on STR inhibits the outputs O_1 and $\overline{O}_1$. A HIGH on CAS forces the output O_1 to HIGH, while the state of $\overline{O}_1$ depends on the inputs S_A to S_D (see lines 1 to 16 of function table).

This device may be used to perform arithmetic operations. For the add mode and multiply mode see Figs 5 and 6.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

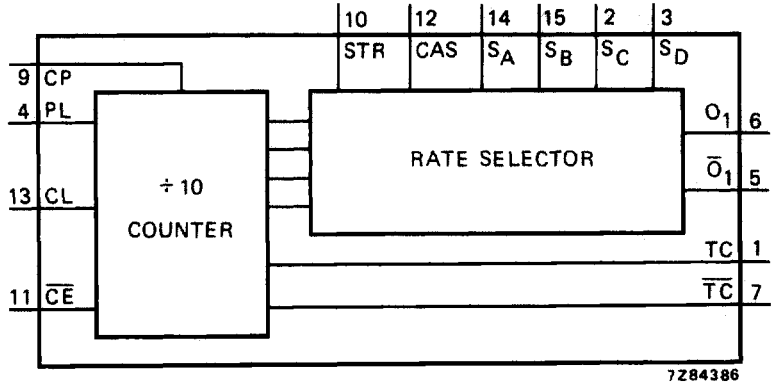
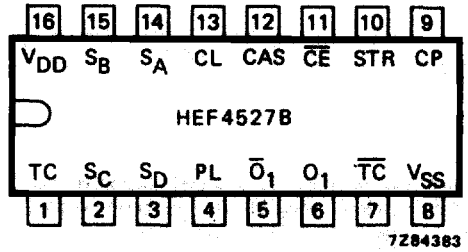


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



HEF4527BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4527BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4527BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

Fig. 2 Pinning diagram.

PINNING

CP	clock input
PL	preset to '9' input
CL	counter clear input
$\overline{CE}$	count enable input (active LOW)
STR	strobe input
CAS	cascade input
S_A to S_D	rate select inputs
O_1 to $\overline{O}_1$	rate outputs
TC	terminal count output (active HIGH)
$\overline{TC}$	terminal count output (active LOW)

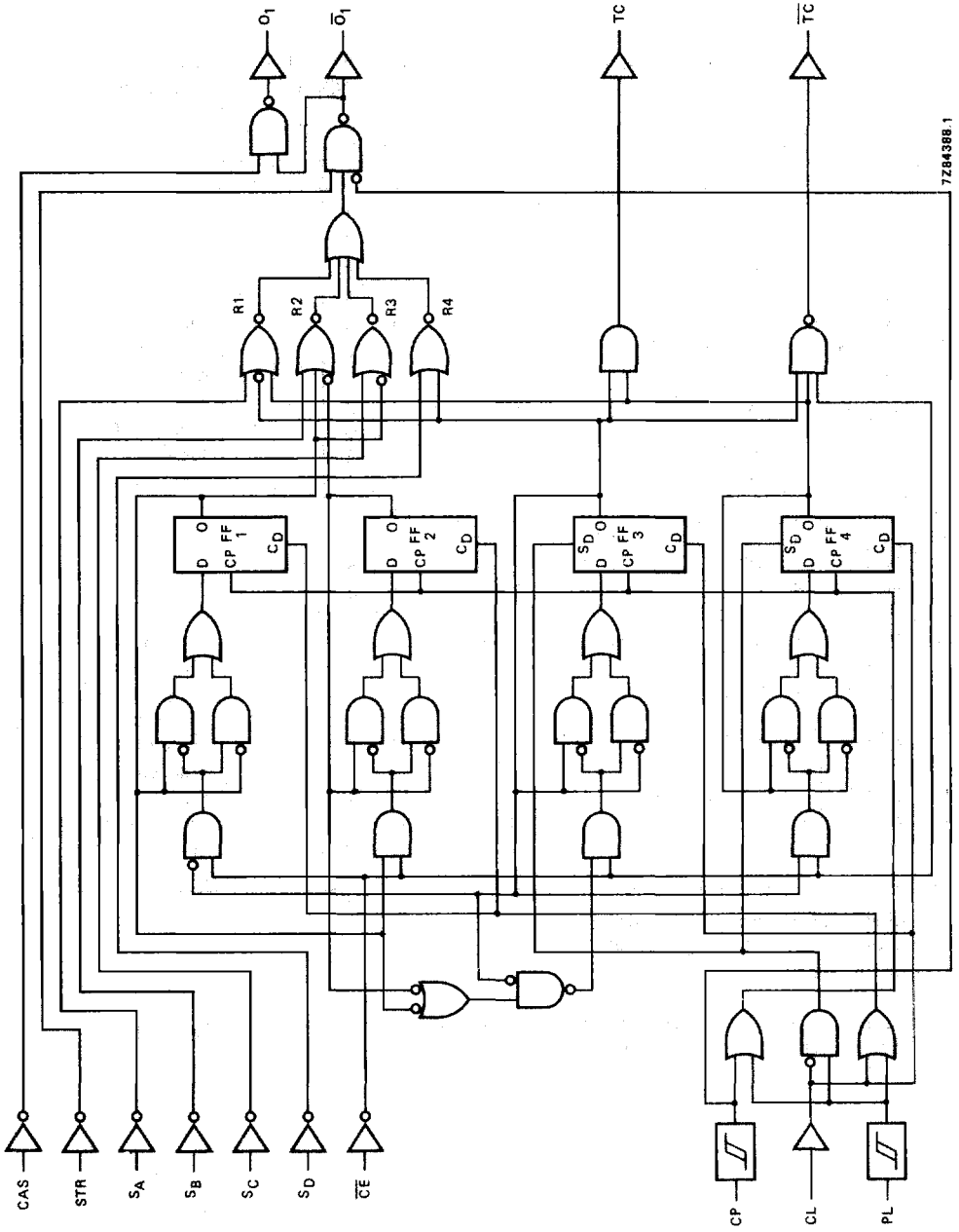


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs										outputs				mode of operation
number of pulses or logic level										number of pulses or logic level				
S_D	S_C	S_B	S_A	CP	$\overline{CE}$	STR	CAS	CL	PL	O_1	$\overline{O}_1$	$\overline{TC}$	TC	
L	L	L	L	10	L	L	L	L	L	L	H	1	1	
L	L	L	H	10	L	L	L	L	L	1	1	1	1	
L	L	H	L	10	L	L	L	L	L	2	2	1	1	
L	L	H	H	10	L	L	L	L	L	3	3	1	1	
L	H	L	L	10	L	L	L	L	L	4	4	1	1	
L	H	L	H	10	L	L	L	L	L	5	5	1	1	rate pulses at
L	H	H	L	10	L	L	L	L	L	6	6	1	1	the outputs
L	H	H	H	10	L	L	L	L	L	7	7	1	1	depend on the
H	L	L	L	10	L	L	L	L	L	8	8	1	1	BCD input
H	L	L	H	10	L	L	L	L	L	9	9	1	1	number at
H	L	H	L	10	L	L	L	L	L	8	8	1	1	S_A to S_D
H	L	H	H	10	L	L	L	L	L	9	9	1	1	
H	H	L	L	10	L	L	L	L	L	8	8	1	1	
H	H	L	H	10	L	L	L	L	L	9	9	1	1	
H	H	H	L	10	L	L	L	L	L	8	8	1	1	
H	H	H	H	10	L	L	L	L	L	9	9	1	1	
X	X	X	X	X	H	L	L	L	L	▲	▲	H	▲	$\overline{CE}$ = H; counter disabled
X	X	X	X	10	L	H	L	L	L	L	H	1	1	outputs O_1 and O_2 disabled
X	X	X	X	10	L	L	H	L	L	H	*	1	1	output O_1 disabled
H	X	X	X	10	L	L	L	H	X	10	10	H	L	CL = H
L	X	X	X	X	L	L	L	H	X	L	H	H	L	counter reset
X	X	X	X	X	L	L	L	L	H	L	H	L	H	PL = H; preset to '9'

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* Same output as the first 16 lines of this function table (depends on the values of S_A to S_D).
▲ Depends on internal state of the counter.

A.C. CHARACTERISTICS V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns.

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	typical extrapolation formula
Propagation delays							
CP → O_1, $\overline{O}_1$	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			160	320	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CP → $\overline{TC}$	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CAS → O_1	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
STR → O_1, $\overline{O}_1$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → $\overline{TC}$	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			65	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
CL → O_1	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CL → $\overline{O}_1$	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns.

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	typical extrapolation formula
Propagation delays							
PL ⟶ O_1, $\overline{O}_1$	5			260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		100	200	ns	89 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			235	470	ns	208 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Minimum clock	5			45	90	ns	
pulse width	10	t_{WCPH}		18	36	ns	
HIGH	15			12	24	ns	
Minimum CL	5			20	40	ns	
pulse width; HIGH	10	t_{WCLH}		12	24	ns	
	15			10	20	ns	
Minimum PL	5			50	100	ns	
pulse width; HIGH	10	t_{WPLH}		20	40	ns	
	15			15	30	ns	
Set-up times	5		30	15		ns	
$\overline{CE}$ ⟶ CP	10	t_{su}	20	10		ns	
	15		12	5		ns	
Recovery times	5		20	10		ns	
CL ⟶ CP	10	t_{RCL}	16	8		ns	
	15		10	5		ns	
	5		80	40		ns	
PL ⟶ CP	10	t_{RPL}	36	18		ns	
	15		25	10		ns	
Maximum clock	5		4,5	9		MHz	
pulse frequency	10	f_{max}	11	22		MHz	
	15		16	32		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 050 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4 500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	10 500 f_i + Σ($f_o C_L$) x V_{DD}^2	

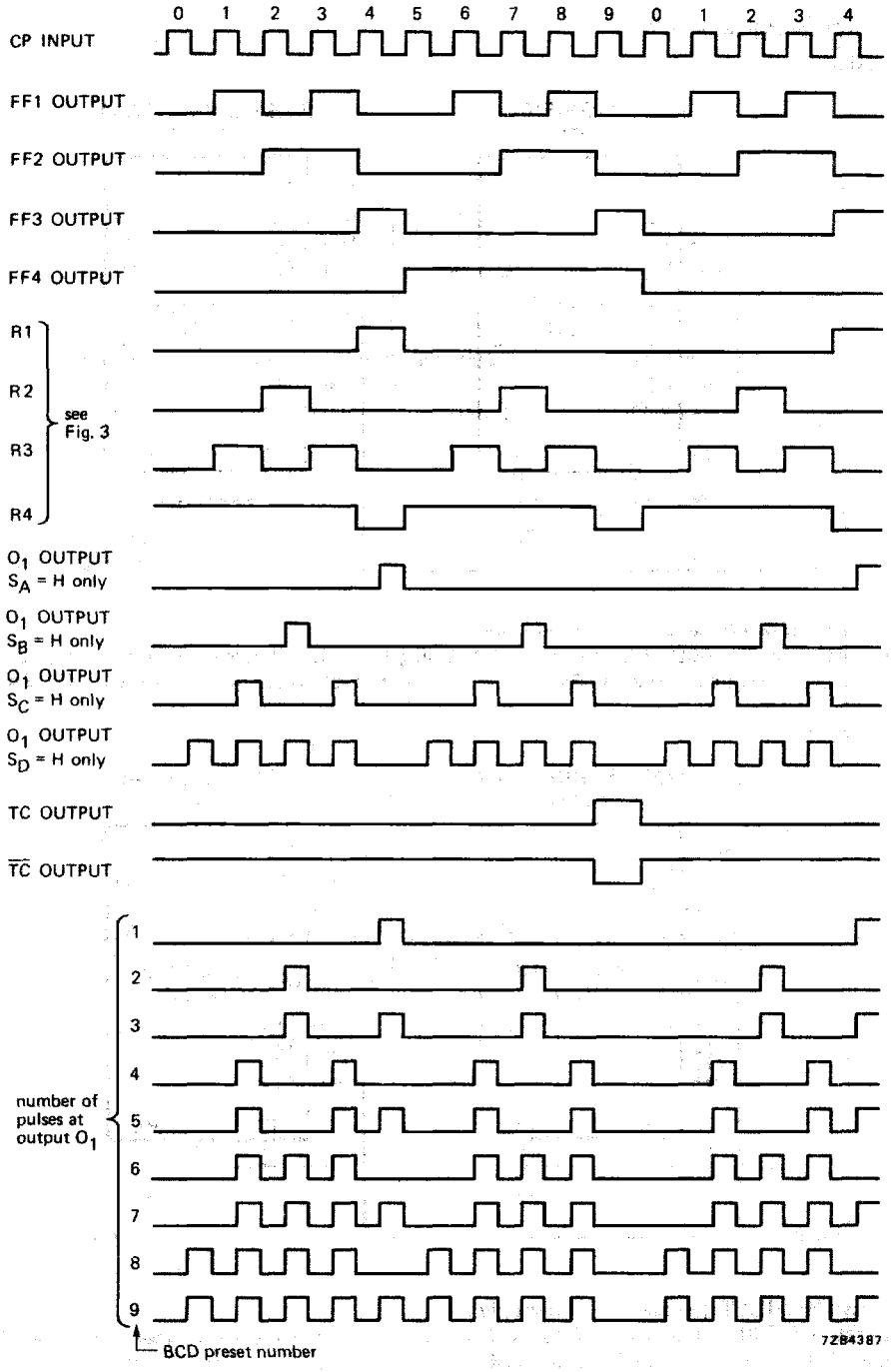


Fig. 4 Timing diagram.

APPLICATION INFORMATION

Add mode

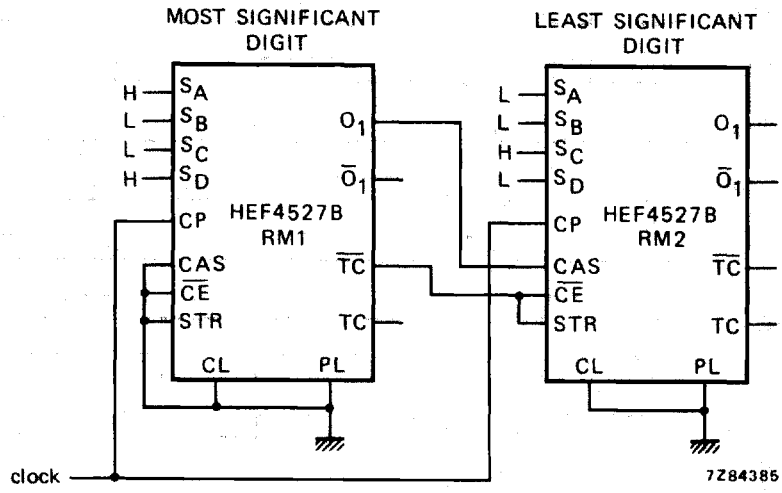


Fig. 5 Two HEF4527B cascaded in the add mode.
Output rate = 10^n (0,1 BCD_1 + 0,01 BCD_2 + 0,01 BCD_3 + ...), in where n = number of cascaded RMs. Example: RM1 preset to 9 and RM2 preset to 4, output rate is 10^2 (0,1 x 9 x 0,01 x 4) = 94.

Multiply mode

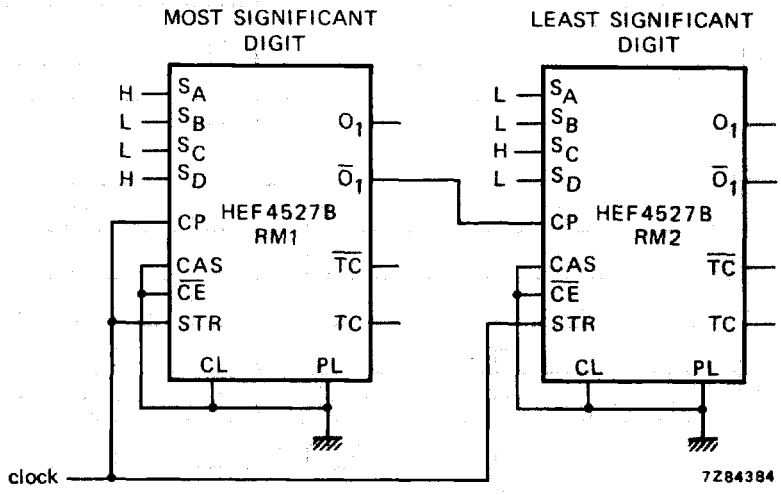


Fig. 6 Two HEF4527B cascaded in the multiply mode.
Output rate = 10^n (0,1 BCD_1 x 0,1 BCD_2 x 0,1 BCD_3 x .....), in where n = number of cascaded RMs.
Example: RM1 preset to 9 and RM2 preset to 4, output rate is 10^2 (0,1 x 9 x 0,1 x 4) = 36.