

HYB39S256[4/8/16]00FT(L)
HYB39S256[4/8/16]00FE(L)
HYB39S256[4/8/16]00FF(L)

256-MBit Synchronous DRAM

SDRAM



Memory Products



Never stop thinking

Edition 2006-03

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1 Overview

1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C Operating Temperature
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7.8 μ s)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V \pm 0.3 V Power Supply
- LVTTL Interface versions
- Plastic Packages: P-TSOPII-54 400mil width (x4, x8, x16)
- Chipsize Packages: P-TFBGA-54 (12 mm x 8 mm)

Table 1 Performance

Product Type Speed Code			-6	-7	Unit
Speed Grade			PC166-333	PC133-222	—
Max. Clock Frequency	@CL3	f_{CK3}	166	143	MHz
		t_{CK3}	6	7	ns
		t_{AC3}	5.4	5.4	ns
	@CL2	t_{CK2}	7.5	7.5	ns
		t_{AC2}	5.4	5.4	ns

1.2 Description

The HYB39S256[400/800/160]F[E/T/F](L) are four bank Synchronous DRAMs organized as 4 banks x 16 MBit x4, 4 banks x 8 MBit x8 and 4 banks x 4 Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with INFINEON's advanced 0.11- μ m 256-MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V \pm 0.3 V power supply. All 256-Mbit components are available in P-TSOPII-54 and P-TFBGA-54 packages.

Table 2 Ordering Information

Product Type	Speed Grade	Package	Description
HYB39S256400FT-7	PC133-222-520	P-TSOPII-54	143MHz 64M x 4 SDRAM
HYB39S256400FTL-7	PC133-222-520	P-TSOPII-54	143MHz 64M x 4 SDRAM
HYB39S256800FT-7	PC133-222-520	P-TSOPII-54	143MHz 32M x 8 SDRAM
HYB39S256800FTL-7	PC133-222-520	P-TSOPII-54	143MHz 32M x 8 SDRAM
HYB39S256160FT-7	PC133-222-520	P-TSOPII-54	143MHz 16M x 16 SDRAM
HYB39S256160FTL-7	PC133-222-520	P-TSOPII-54	143MHz 16M x 16 SDRAM


Table 3 Ordering Information for RoHS Compliant Products

Product Type ¹⁾	Speed Grade	Package	Description
HYB39S256400FF-7	PC133-222-520	P-TFBGA-54	143MHz 64M x 4 SDRAM
HYB39S256400FE-7	PC133-222-520	P-TSOPII-54	143MHz 64M x 4 SDRAM
HYB39S256400FFL-7	PC133-222-520	P-TFBGA-54	143MHz 64M x 4 SDRAM
HYB39S256400FEL-7	PC133-222-520	P-TSOPII-54	143MHz 64M x 4 SDRAM
HYB39S256800FF-7	PC133-222-520	P-TFBGA-54	143MHz 32M x 8 SDRAM
HYB39S256800FE-7	PC133-222-520	P-TSOPII-54	143MHz 32M x 8 SDRAM
HYB39S256800FFL-7	PC133-222-520	P-TFBGA-54	143MHz 32M x 8 SDRAM
HYB39S256800FEL-7	PC133-222-520	P-TSOPII-54	143MHz 32M x 8 SDRAM
HYB39S256160FF-7	PC133-222-520	P-TFBGA-54	143MHz 16M x 16 SDRAM
HYB39S256160FE-7	PC133-222-520	P-TSOPII-54	143MHz 16M x 16 SDRAM
HYB39S256160FFL-7	PC133-222-520	P-TFBGA-54	143MHz 16M x 16 SDRAM
HYB39S256160FEL-7	PC133-222-520	P-TSOPII-54	143MHz 16M x 16 SDRAM
HYB39S256160FF-6	PC166-333-520	P-TFBGA-54	166MHz 16M x 16 SDRAM
HYB39S256160FE-6	PC166-333-520	P-TSOPII-54	166MHz 16M x 16 SDRAM
HB39S256160FFL-6	PC166-333-520	P-TFBGA-54	166MHz 16M x 16 SDRAM
HB39S256160FEL-6	PC166-333-520	P-TSOPII-54	166MHz 16M x 16 SDRAM

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

2 Pin Configuration and Block Diagrams

This chapter contains the pin configuration table, the TSOP and FBGA package drawing, and the block diagrams for the $\times 4$, $\times 8$, $\times 16$ organization of the SDRAM.

2.1 Pin Description

Listed below are the pin configurations sections for the various signals of the SDRAM

- **Clock Signals $\times 4/\times 8/\times 16$ Organization**
- **Control Signals $\times 4/\times 8/\times 16$ Organization**
- **Address Signals $\times 4/\times 8/\times 16$ Organization**
- **Data Signals $\times 4$ Organization**
- **Data Signals $\times 8$ Organization**
- **Data Signals $\times 16$ Organization**
- **Data Mask $\times 4/\times 8$ Organization**
- **Data Mask $\times 16$ Organization**
- **Power Supplies $\times 4/\times 8/\times 16$ Organization**
- **Not connected $\times 4$ Organization**
- **Not connected $\times 8$ Organization**
- **Not connected $\times 16$ Organization**

Table 4 Pin Configuration of the SDRAM

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals $\times 4/\times 8/\times 16$ Organization				
38,2F	CLK	I	LVTTTL	Clock Signal CK <i>Note: The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.</i>
37,3F	CKE	I	LVTTTL	Clock Enable <i>Note: Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiating either the Power Down mode, Suspend mode, or the Self Refresh mode.</i>
Control Signals $\times 4/\times 8/\times 16$ Organization				
18, 8F	RAS	I	LVTTTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE) <i>Note: When sampled at the positive rising edge of the clock, CAS, RAS, and WE define the command to be executed by the SDRAM.</i>
17, 7F	CAS	I	LVTTTL	
16, 9F	WE	I	LVTTTL	
19, 9G	CS	I	LVTTTL	Chip Select <i>Note: Enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.</i>
Address Signals $\times 4/\times 8/\times 16$ Organization				
20, 7G	BA0	I	LVTTTL	Bank Address Signals 1:0 <i>Note: Bank Select Inputs. Bank address inputs selects which of the four banks a command applies to.</i>
21, 8G	BA1	I	LVTTTL	

Table 4 Pin Configuration of the SDRAM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
23, 7H	A0	I	LVTTTL	Address Signal 9:0, Address Signal 10/Auto precharge <i>Note: During a Bank Activate command cycle, A0-A12 define the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An define the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends upon the SDRAM organization: 64M x4SDRAM CAn = CA9, CA11 (Page Length = 2048 bits) 32M x8SDRAM CAn = CA9 (Page Length = 1024 bits) 16M x16SDRAM CAn = CA8 (Page Length = 512 bits) In addition to the column address, A10 (= AP) is used to invoke the auto pre charge operation at the end of the burst read or write cycle. If A10 is high, auto pre charge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, auto pre charge is disabled. During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.</i>
24, 8H	A1	I	LVTTTL	
25, 8J	A2	I	LVTTTL	
26, 7J	A3	I	LVTTTL	
29, 3J	A4	I	LVTTTL	
30, 2J	A5	I	LVTTTL	
31, H	A6	I	LVTTTL	
32, 2H	A7	I	LVTTTL	
33, 1H	A8	I	LVTTTL	
34, 3G	A9	I	LVTTTL	
22, 9H	A10	I	LVTTTL	
35, 2G	A11	I	LVTTTL	
36, 1G	A12	I	LVTTTL	

Data Signals ×4 Organization

5, 8B	DQ0	I/O	LVTTTL	Data Signal Bus [15:0] <i>Note: Data Input/Output pins operate in the same manner as on EDO or FPM DRAMs.</i>
11, 8D	DQ1	I/O	LVTTTL	
44, 2D	DQ2	I/O	LVTTTL	
50, 2B	DQ3	I/O	LVTTTL	

Data Signals ×8 Organization

2, 8A	DQ0	I/O	LVTTTL	Data Signal Bus [15:0] <i>Note: Data Input/Output pins operate in the same manner as on EDO or FPM DRAMs.</i>
5, 8B	DQ1	I/O	LVTTTL	
8, 8C	DQ2	I/O	LVTTTL	
11, 8D	DQ3	I/O	LVTTTL	
44, 2D	DQ4	I/O	LVTTTL	
47, 2C	DQ5	I/O	LVTTTL	
50, 2B	DQ6	I/O	LVTTTL	
53, 2A	DQ7	I/O	LVTTTL	

Table 4 Pin Configuration of the SDRAM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals ×16 Organization				
2, 9A	DQ0	I/O	LVTTL	Data Signal Bus [15:0] <i>Note: Data Input/Output pins operate in the same manner as on EDO or FPM DRAMs.</i>
4, 9B	DQ1	I/O	LVTTL	
5, 8B	DQ2	I/O	LVTTL	
7, 9C	DQ3	I/O	LVTTL	
8, 8C	DQ4	I/O	LVTTL	
10, 9D	DQ5	I/O	LVTTL	
11, 8D	DQ6	I/O	LVTTL	
13, 9E	DQ7	I/O	LVTTL	
42, 1E	DQ8	I/O	LVTTL	
44, 2D	DQ9	I/O	LVTTL	
45, 1D	DQ10	I/O	LVTTL	
47, 2C	DQ11	I/O	LVTTL	
48, 1C	DQ12	I/O	LVTTL	
50, 2B	DQ13	I/O	LVTTL	
51, 1B	DQ14	I/O	LVTTL	
53, 2A	DQ15	I/O	LVTTL	
Data Mask ×4/×8 Organization				
39, 1F	DQM	I/O	LVTTL	Data Mask <i>Note: The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. One DQM input is present in x4 and x8 SDRAMs.</i>
Data Mask ×16 Organization				
39, 1F	UDQM	I/O	LVTTL	Data Mask Upper Byte <i>Note: LDQM and UDQM controls the lower and upper bytes in x16 SDRAMs.</i>
15, 8E	LDQM	I/O	LVTTL	Data Mask Lower Byte
Power Supplies ×4/×8/×16 Organization				
3B, 3D, 7A, 7C	V_{DDQ}	PWR	–	Power Supply
7E, 9A, 9J	V_{DD}	PWR	–	Power Supply <i>Note: Power for the input buffers and the core logic (3.3 V)</i>
3A, 3C, 7B, 7D	V_{SSQ}	PWR	–	Power Supply Ground for DQs <i>Note: Isolated power supply and ground for the output buffers to provide improved noise immunity.</i>
1J, 1A, 3E	V_{SS}	PWR	–	Power Supply Ground

Table 4 Pin Configuration of the SDRAM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Not connected ×4 Organization				
2, 4, 7, 8, 10, 13, 15, 40, 42, 45, 47, 48, 51, 53, 1B, 1C, 1D, 1E, 2A, 2C, 2E, 8A, 8C, 8E, 9B, 9C, 9D, 9E	NC	NC	–	Not connected <i>Note: No internal electrical connection is present.</i>
Not connected ×8 Organization				
7, 10, 13, 15, 40, 42, 45, 48, 51, 1B, 1C, 1D, 1E, 2E, 8E, 9B, 9C, 9D, 9E	NC	NC	–	Not connected <i>Note: No internal electrical connection is present.</i>
Not connected ×16 Organization				
40, 2E	NC	NC	–	Not connected <i>Note: No internal electrical connection is present.</i>

2.2 Package P-TSOPII-54

Listed below are the pin outs of the TSOP package.

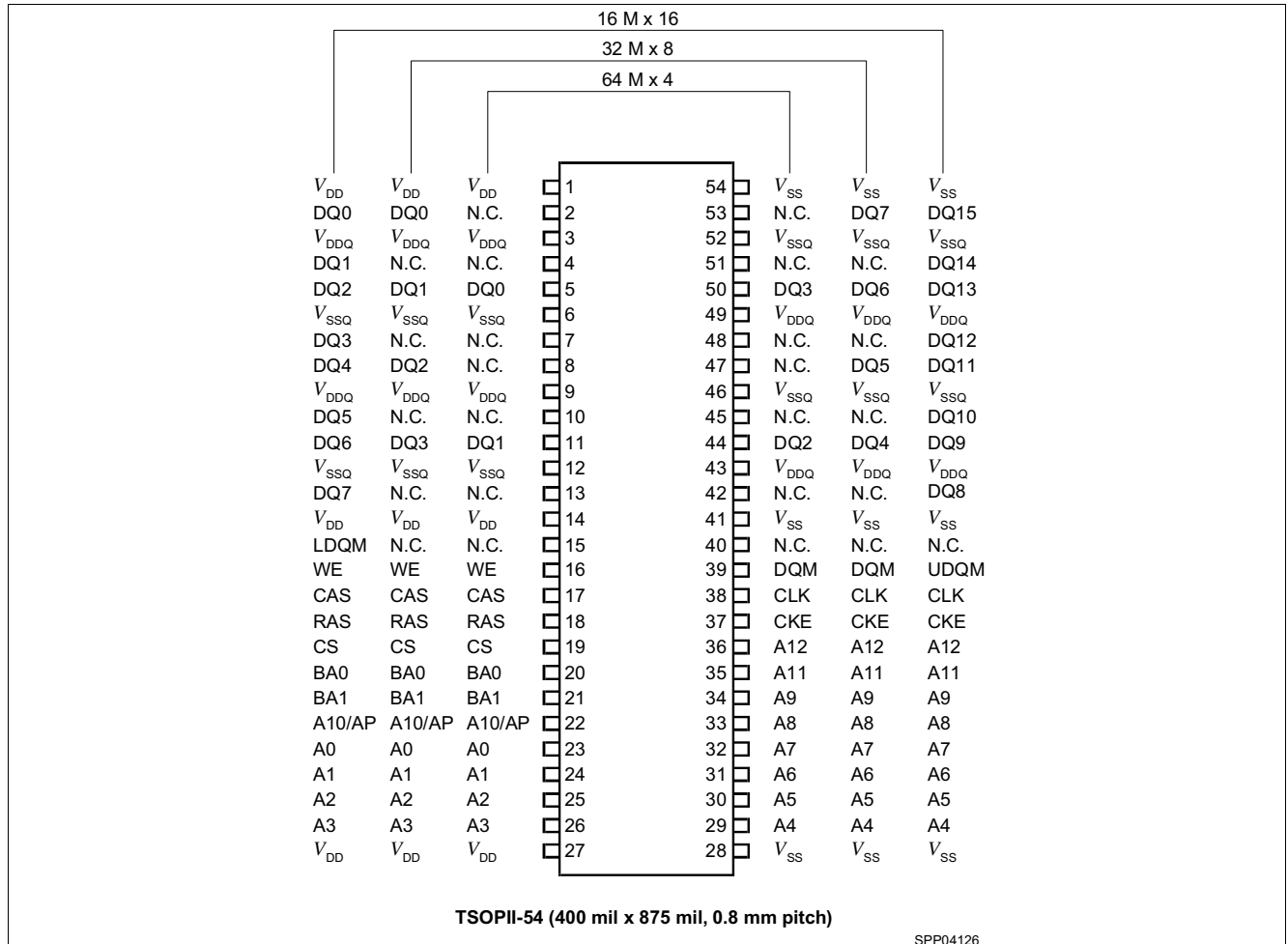


Figure 1 Pinouts P-TSOPII-54

2.3 Package P-TFBGA-54

Listed below are the ball outs of the TFBGA package.

- Ball out for ×16 components, PG-TFBGA-54 (top view)
- Ball out for ×8 components, PG-TFBGA-54 (top view)
- Ball out for ×4 components, PG-TFBGA-54 (top view)

1	2	3	4	5	6	7	8	9
V_{SS}	DQ15	V_{SSQ}		A		V_{DDQ}	DQ0	V_{DD}
DQ14	DQ13	V_{DDQ}		B		V_{SSQ}	DQ2	DQ1
DQ12	DQ11	V_{SSQ}		C		V_{DDQ}	DQ4	DQ3
DQ10	DQ9	V_{DDQ}		D		V_{SSQ}	DQ6	DQ5
DQ8	NC	V_{SS}		E		V_{DD}	LDQM	DQ7
UDQM	CLK	CKE		F		$\overline{\text{CAS}}$	$\overline{\text{RAS}}$	$\overline{\text{WE}}$
A12	A11	A9		G		BA0	BA1	$\overline{\text{CS}}$
A8	A7	A6		H		A0	A1	A10
V_{SS}	A5	A4		J		A3	A2	V_{DD}

MPPD0391

Figure 2 Ball out for ×16 components, PG-TFBGA-54 (top view)

Pin Configuration and Block Diagrams

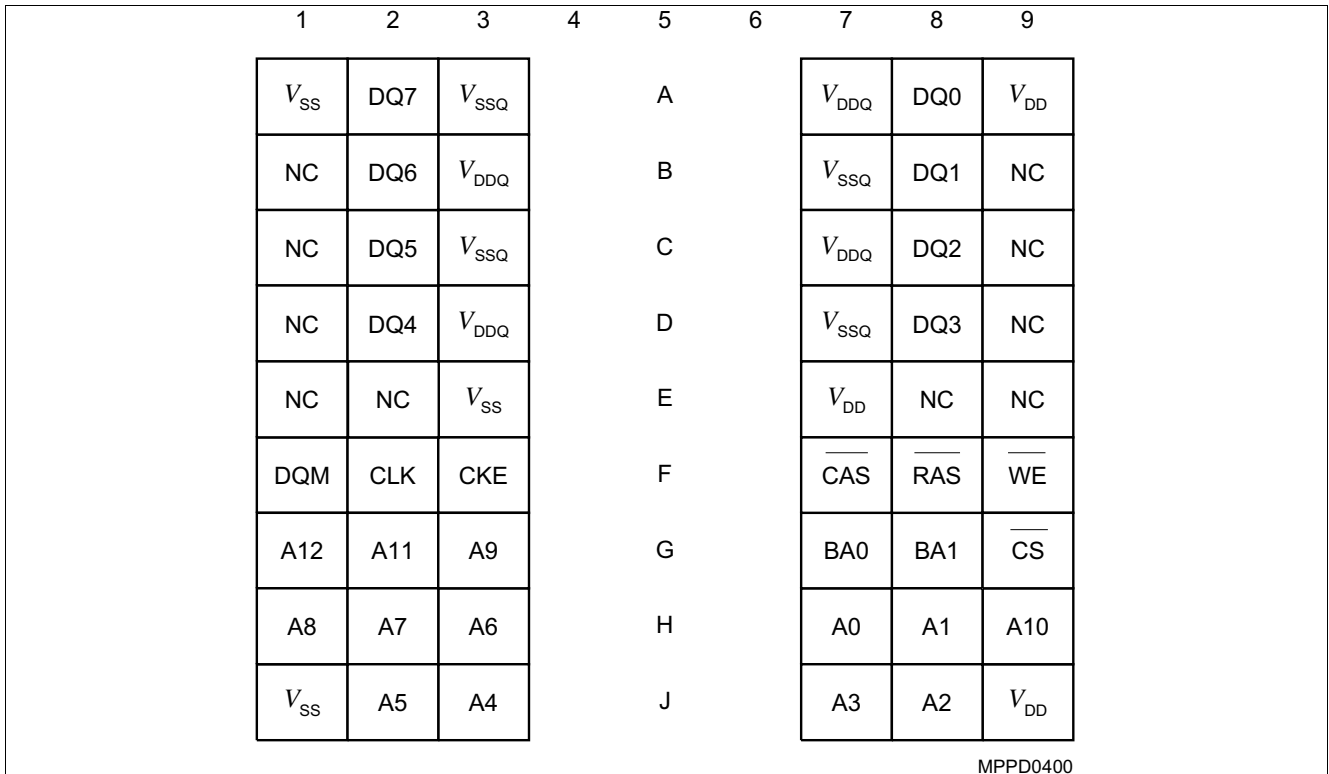


Figure 3 Ball out for ×8 components, PG-TFBGA-54 (top view)

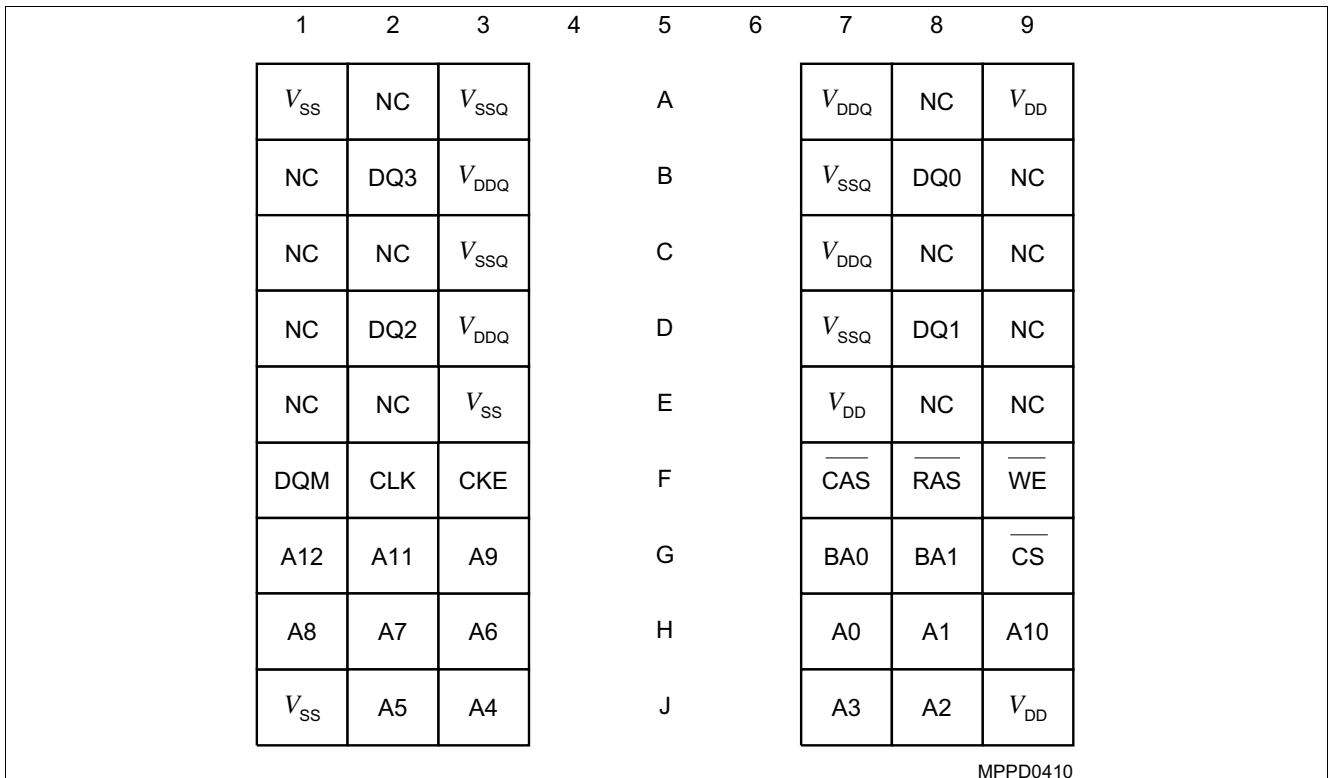


Figure 4 Ball out for ×4 components, PG-TFBGA-54 (top view)

2.4 Block Diagrams

The Block diagrams for 64M x 4, 32M x 8 and 16M x 16 are shown below.

- [Block Diagram for 64M x 4 SDRAM \(13/11/2 Addressing\)](#)
- [Block Diagram for 32M x 8 SDRAM \(13/10/2 Addressing\)](#)
- [Block Diagram for 16M x 16 SDRAM \(13/9/2 Addressing\)](#)

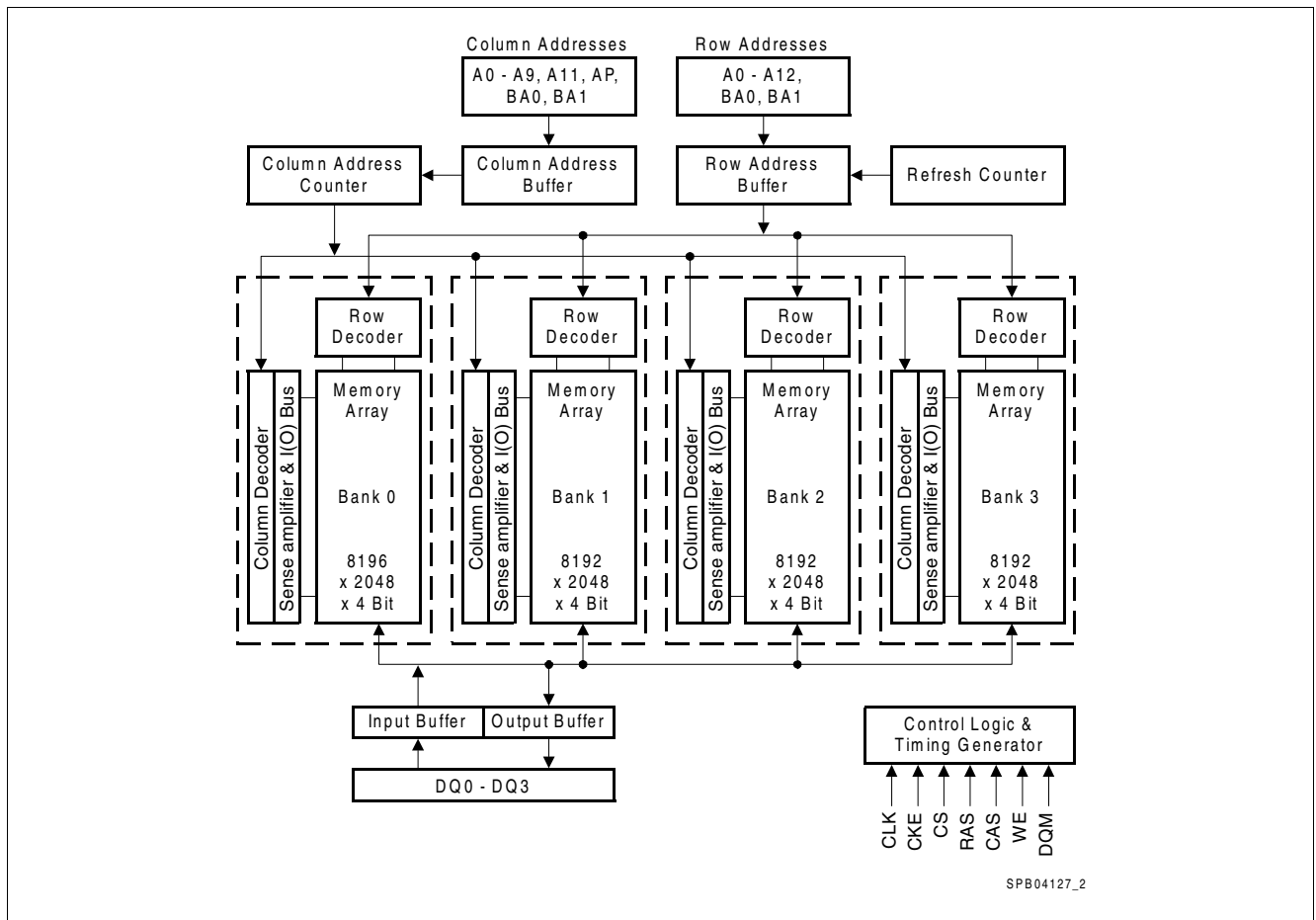


Figure 5 Block Diagram for 64M x 4 SDRAM (13/11/2 Addressing)

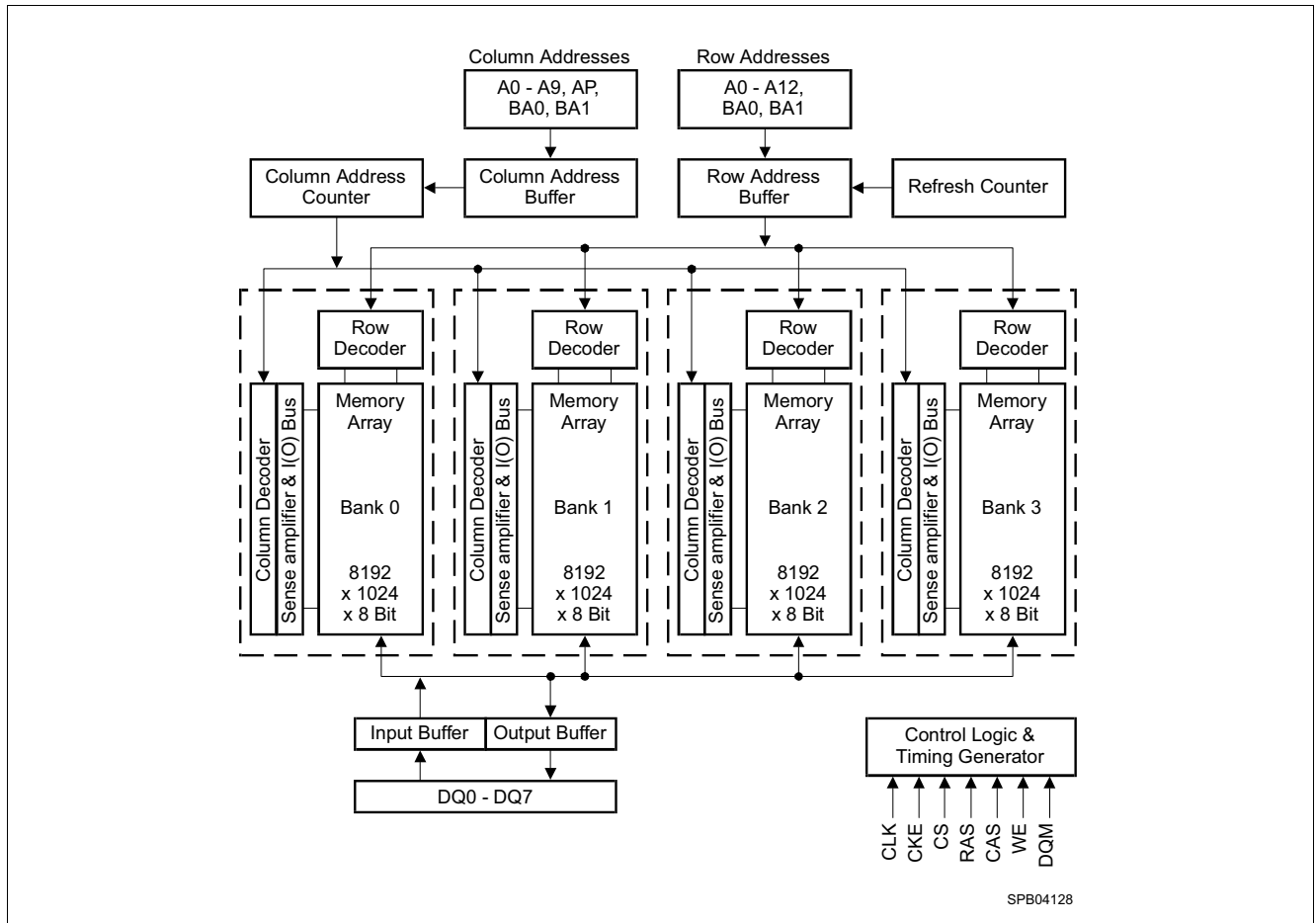


Figure 6 Block Diagram for 32M x 8 SDRAM (13/10/2 Addressing)

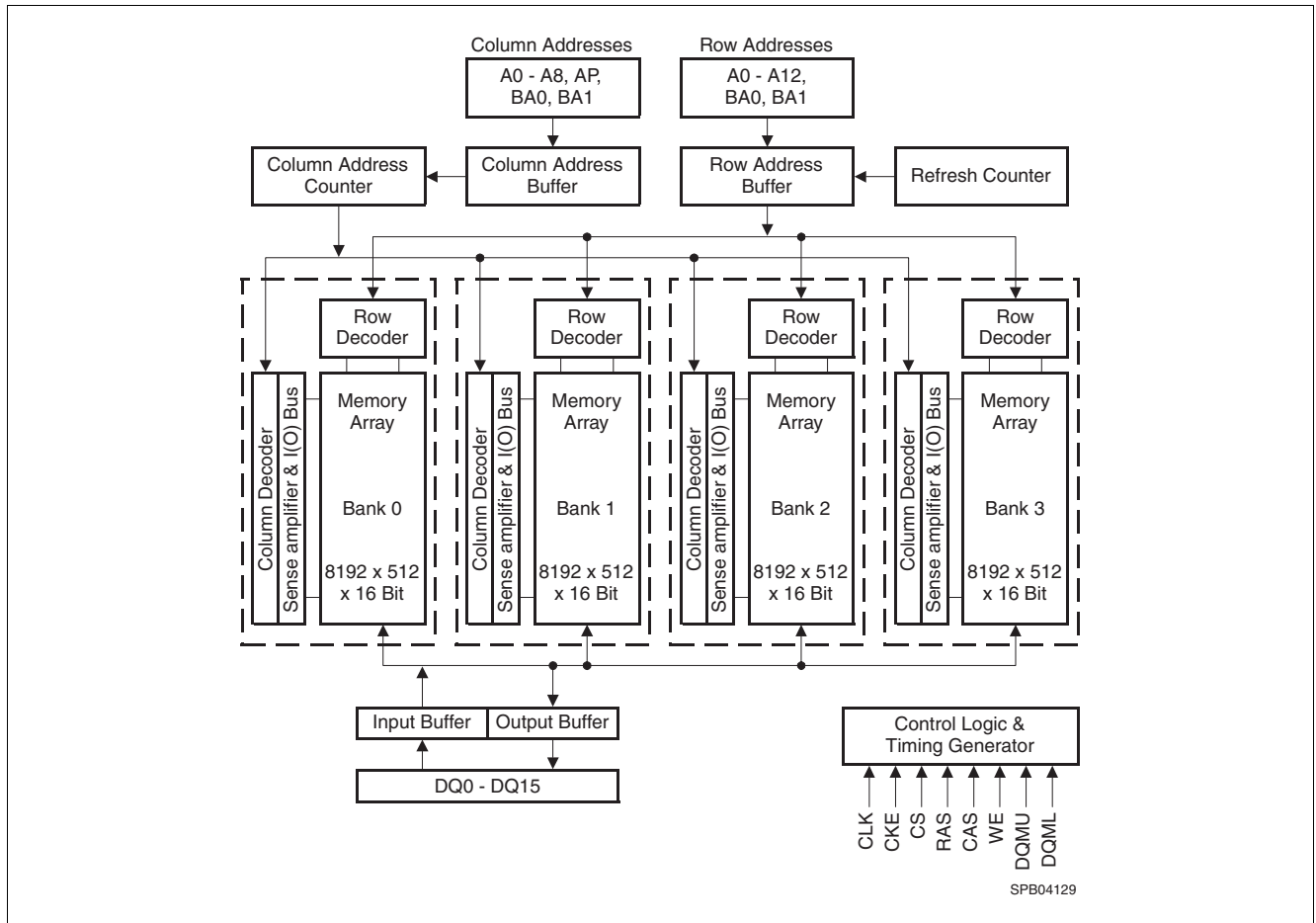


Figure 7 Block Diagram for 16M x 16 SDRAM (13/9/2 Addressing)

3 Functional Description

3.1 Operation Definition

All of SDRAM operations are defined by states of control signals \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Table 5 Truth Table: Operation Command

Operation	Device State	CKE n-1 ¹⁾²⁾	CKE n ¹⁾²⁾	DQM 1)2)	BA0 BA1 ¹⁾²⁾	AP= A10 ¹⁾²⁾	Addr. 1)2)	CS 1)2)	RAS 1)2)	CAS 1)2)	WE 1)2)
Bank Active	Idle ³⁾	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active ³⁾	H	X	X	V	L	V	L	H	L	L
Write with Auto pre charge	Active ³⁾	H	X	X	V	H	V	L	H	L	L
Read	Active ³⁾	H	X	X	V	L	V	L	H	L	H
Read with Auto pre charge	Active ³⁾	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Entry (Precharge or active standby)	Idle	H	L	X	X	X	X	H	X	X	X
	Active							L	H	H	H
Clock Suspend Exit	Active ⁴⁾	L	H	X	X	X	X	X	X	X	X
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

1) V = Valid, x = Don't Care, L = Low Level, H = High Level

2) CKE_n signal is input level when commands are provided, CKE_{n-1} signal is input level one clock before the commands are provided.

3) This is the state of the banks designated by BA0, BA1 signals.

4) Power Down Mode can not be entered in a burst cycle. When this command asserted in the burst mode cycle device is in clock suspend mode.

3.2 Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed $V_{DD} + 0.3$ V on any of the input pins or V_{DD} supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 μ s is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

3.3 Mode Register Definition

The Mode register designates the operation mode at the read or write cycle. This register is divided into four fields. First, a Burst Length field which sets the length of the burst. Second, an Addressing Selection bit which programs the column access sequence in a burst cycle (interleaved or sequential). Third, a CAS Latency field to set the access time at clock cycle. Fourth, an Operation mode field to differentiate between normal operation (Burst read and burst Write) and special Burst Read and Single Write mode. After the initial power up, the mode set operation must be done before any activate command. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of RAS, CAS, and WE at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

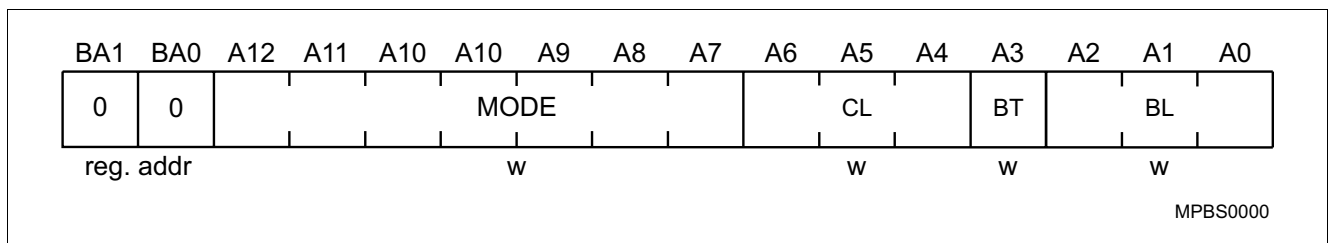


Table 6 Mode Register Definition (BA[1:0] = 00_B)

Field	Bits	Type	Description
BL	[2:0]	w	Burst Length Number of sequential bits per DQ related to one read/write command, see Chapter 3.3.1 All other bit combinations are RESERVED 000 _B 1, 001 _B 2, 010 _B 4, 011 _B 8, 111 _B Full Page (Sequential burst type only),
BT	3	w	Burst Type See Table 8 for internal address sequence of low order address bits. 0 _B Sequential, 1 _B Interleaved,
CL	[6:4]	w	CAS Latency Number of full clocks from read command to first data valid window. All other bit combinations are RESERVED. 010 _B 2, 011 _B 3,
Mode	[12:7]	w	Operation Mode All other bit combinations are RESERVED. 0 _B Burst read/burst write, 1 _B Burst read/single write,

3.3.1 Burst Length

Table 7 Burst Length and Sequence

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type=Sequential	Type=Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
FullPage	n			Cn, Cn+1, Cn+2	not supported

Notes

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access with in the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

3.4 Commands

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the CAS -before-RAS refresh of conventional DRAMs. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are held low and CKE and $\overline{\text{WE}}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. The mode restores the word lines after $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and CKE are low and $\overline{\text{WE}}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} ("write recovery time") after the last data in. A burst operation with Auto-Precharge may only be interrupted by a burst start to another bank. It must not be interrupted by a precharge or a burst stop command.

Precharge Command

There is also a separate precharge command available. When $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ are low and $\overline{\text{CAS}}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2 and two clocks before the last data out for CAS latency = 3. Writes require a time delay t_{WR} ("write recovery time") of 2 clocks minimum from the last data out to apply the precharge command.

Table 8 Bank Selection by Address Bits

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	All Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

3.5 Operations

3.5.1 Read and Write

When $\overline{\text{RAS}}$ is low and both $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high at the positive edge of the clock, a $\overline{\text{RAS}}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A CAS cycle is triggered by setting $\overline{\text{RAS}}$ high and $\overline{\text{CAS}}$ low at a clock timing after a necessary delay, t_{RCD} from the RAS timing. $\overline{\text{WE}}$ is used to define either a read ($\overline{\text{WE}} = \text{H}$) or a write ($\overline{\text{WE}} = \text{L}$) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4 and 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organization and column addressing. Full page burst operation does not self terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAMs, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

3.5.2 DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

3.5.3 Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

3.5.4 Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for Power Down mode entry and exit.

4 Electrical Characteristics

4.1 Operating Conditions

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/ Test Condition
		Min.	Max.		
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	- 1.0	+4.6	V	-
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	- 1.0	+4.6	V	-
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	- 1.0	+4.6	V	-
Operating Temperature	T_A	0	+70	°C	-
Storage temperature range	T_{STG}	-55	+150	°C	-
Power dissipation per SDRAM component	P_D	-	1	W	-
Data out current (short circuit)	I_{OUT}	-	50	mA	-

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 10 DC Characteristics¹⁾

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Supply Voltage	V_{DD}	3.0	3.6	V	2)
I/O Supply Voltage	V_{DDQ}	3.0	3.6	V	2)
Input high voltage	V_{IH}	2.0	$V_{DDQ}+0.3$	V	2)3)
Input low voltage	V_{IL}	- 0.3	+0.8	V	2)3)
Output high voltage ($I_{OUT} = - 4.0$ mA)	V_{OH}	2.4	-	V	2)
Output low voltage ($I_{OUT} = 4.0$ mA)	V_{OL}	-	0.4	V	2)
Input leakage current, any input ($0\text{ V} < V_{IN} < V_{DD}$, all other inputs = 0 V)	I_{IL}	- 5	+5	μA	-
Output leakage current (DQs are disabled, $0\text{ V} < V_{OUT} < V_{DDQ}$)	I_{OL}	- 5	+5	μA	-

1) $T_A = 0$ to 70 °C

2) All voltages are referenced to V_{SS}

3) V_{IH} may overshoot to $V_{DDQ} + 2.0$ V for pulse width of < 4ns with 3.3 V. V_{IL} may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Table 11 Input and Output Capacitances¹⁾

Parameter	Symbol	Values ²⁾		Unit
		Min.	Max.	
Input Capacitances: CK, $\overline{\text{CK}}$	C_{I1}	2.5	3.5	pF
Input Capacitance (A0-A12, BA0, BA1, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, DQM)	C_{I2}	2.5	3.8	pF
Input/Output Capacitance (DQ)	C_{I0}	4.0	6.0	pF

1) $T_A = 0$ to 70 °C; $V_{DD}, V_{DDQ} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $f = 1 \text{ MHz}$

2) Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF

Table 12 I_{DD} Conditions

Parameter	Symbol
Operating Current One bank active, Burst length = 1	I_{DD1}
Precharge Standby Current in Power Down Mode	I_{DD2P}
Recharge Standby Current in Non-Power Down Mode	I_{DD2N}
No Operating Current Active state (max. 4 banks)	I_{DD3N}
	I_{DD3P}
Burst Operating Current Read command cycling	I_{DD4}
Auto Refresh Current Auto Refresh command cycling	I_{DD5}
Self Refresh Current (standard components) Self Refresh Mode, $\text{CKE}=0.2\text{V}$, $t_{\text{CK}}=\text{infinity}$	I_{DD6}

Table 13 I_{DD} Specifications and Conditions¹⁾²⁾

Symbol	-6	-7	Unit	Note/ Test Condition
	Max.			
I_{DD1}	100	80	mA	$t_{RC} = t_{RC(min)}$, $I_O = 0$ mA ³⁾⁴⁾
I_{DD2P}	2	2	mA	$\overline{CS} = V_{IH(min)}$, $CKE \leq V_{IL(max)}$ ²⁾
I_{DD2N}	26	22	mA	$\overline{CS} = V_{IH(min)}$, $CKE \geq V_{IH(min)}$ ²⁾
I_{DD3N}	40	35	mA	$CS = V_{IH(min)}$, $CKE \geq V_{IH(min)}$ ²⁾
I_{DD3P}	5	5	mA	$CS = V_{IH(min)}$, $CKE \leq V_{IL(max)}$ ²⁾
I_{DD4}	65	57	mA	²⁾³⁾
I_{DD5}	168	142	mA	$t_{RFC} = t_{RFC(min)}$ ⁵⁾
	25	25	mA	$t_{RFC} = 7.8 \mu s$
I_{DD6}	3	3	mA	Standard components
	0.85	0.85	mA	Low power components

1) Currents values will be added when available.

2) $T_A = 0$ to 70 °C; $V_{SS} = 0$ V; V_{DD} , $V_{DDQ} = 3.3$ V \pm 0.3 V

3) These parameters depend on the cycle rate. All values are measured at 166 MHz for -6, at 133 MHz for -7 and -7.5 and at 100 MHz for -8 components with the outputs open. Input signals are changed once during t_{CK} .

4) These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the V_{DDQ} current is excluded.

5) $t_{RFC} = t_{RFC(min)}$ "burst refresh", $t_{RFC} = 7.8 \mu s$ "distributed refresh"

4.2 AC Characteristics
Table 14 AC Timing - Absolute Specifications –7/-6 ¹⁾²⁾³⁾

Parameter	Symbol	–7		–6		Unit	Notes
		PC133 - 222		PC166 - 333			
		Min.	Max.	Min.	Max.		
Clock and Clock Enable							
Clock Frequency	t_{CK}	—	–7	—	–6	ns	CL3
		—	–7.5	—	–7.5	ns	CL2
Access Time from Clock	t_{AC}	—	5.4	—	5.4	ns	CL3
		—	5.4	—	5.4	ns	CL2 3)4)5)
Clock High Pulse Width	t_{CH}	2.5	—	2	—	ns	
Clock Low Pulse Width	t_{CL}	2.5	—	2	—	ns	
Transition time	t_T	0.3	1.2	0.3	1.2	ns	
Setup and Hold Times							
Input Setup Time	t_{IS}	1.5	—	1.5	—	ns	6)
Input Hold Time	t_{IH}	0.8	—	0.8	—	ns	6)
CKE Setup Time	t_{CK}	1.5	—	1.5	—	ns	6)
CKE Hold Time	t_{CKH}	0.8	—	0.8	—	ns	6)
Mode Register Set-up to Active delay	t_{RSC}	2	—	2	—	t_{CK}	
Power Down Mode Entry Time	t_{SB}	0	7	0	6	ns	
Common Parameters							
Row to Column Delay Time	t_{RCD}	15	—	15	—	ns	7)
Row Precharge Time	t_{RP}	15	—	15	—	ns	7)
Row Active Time	t_{RAS}	37	100k	36	100k	ns	7)
Row Cycle Time	t_{RC}	60	—	60	—	ns	7)
Row Cycle Time during Auto Refresh	t_{RFC}	63	—	60	—	ns	
Activate(a) to Activate(b) Command period	t_{RRD}	14	—	12	—	ns	7)
CAS(a) to CAS(b) Command period	t_{CCD}	1	—	1	—	t_{CK}	
Refresh Cycle							
Refresh Period (8192 cycles)	t_{REF}	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	1	—	1	—	t_{CK}	
Data Out Hold Time	t_{OH}	3	—	2.5	—	ns	3)5)
Read Cycle							
Data Out to Low Impedance Time	t_{LZ}	0	—	0	—	ns	
Data Out to High Impedance Time	t_{HZ}	3	7	3	6	ns	
DQM Data Out Disable Latency	t_{DQZ}	—	2	—	2	t_{CK}	
Write Cycle							
Last Data Input to Precharge (Write without Auto Precharge)	t_{WR}	14	—	12	—	ns	8)

Table 14 AC Timing - Absolute Specifications -7/-6 (cont'd)¹⁾²⁾³⁾

Parameter	Symbol	-7		-6		Unit	Notes
		PC133 - 222		PC166 - 333			
		Min.	Max.	Min.	Max.		
Last Data Input to Activate (Write with Auto Precharge)	$t_{DAL(min.)}$					t_{CK}	⁹⁾
DQM Write Mask Latency	t_{DQW}	0	—	0	—	t_{CK}	

- $T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD}, V_{DDQ} = 3.3$ V \pm 0.3 V, $t_T = 1$ ns
- For proper power-up see the operation section of this data sheet.
- AC timing tests for LV-TTL versions have $V_{IL} = 0.4$ V and $V_{IH} = 2.4$ V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL} . All AC measurements assume $t_T = 1$ ns with the AC output load circuit shown in figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.
- If clock rising time is longer than 1 ns, a time $(t_T/2 - 0.5)$ ns has to be added to this parameter.
- Access time from clock t_{ac} is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time t_{oh} is 1.8 ns for PC133 components with no termination and 0 pF load.
- If t_T is longer than 1 ns, a time $(t_T - 1)$ ns has to be added to this parameter.
- These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
- It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times t_{CK} greater or equal the specified t_{WR} value, where t_{ck} is equal to the actual system clock time.
- When a Write command with Auto Precharge has been issued, a time of $t_{DAL(min)}$ has to be fulfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. t_{CK} is equal to the actual system clock time.

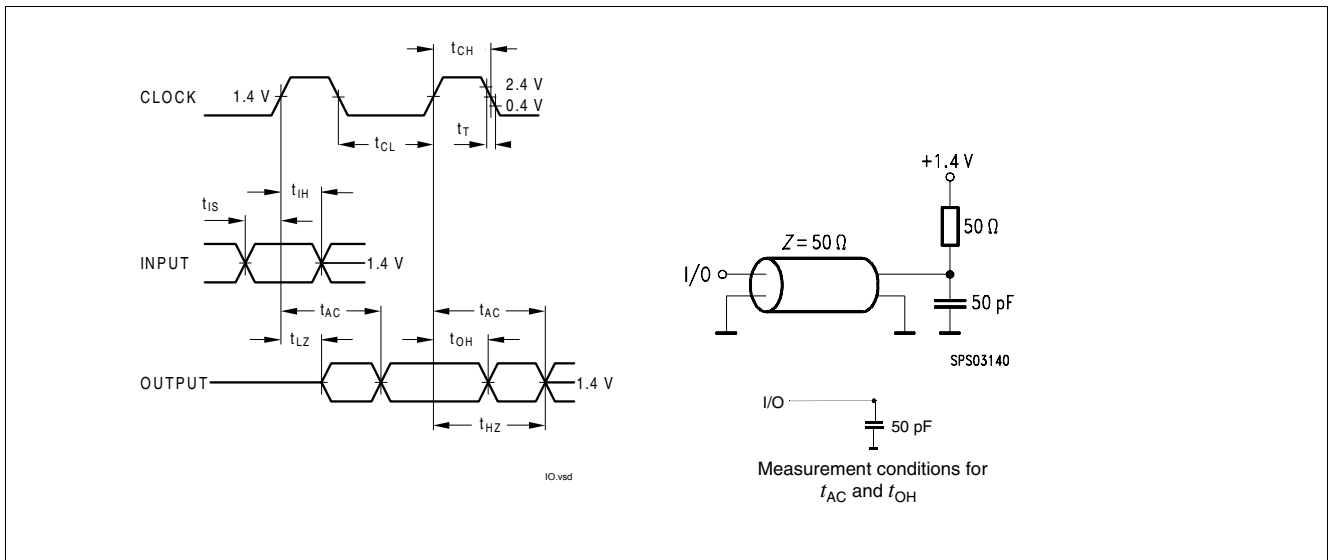


Figure 8 Measurement conditions for t_{AC} and t_{OH}

5 Timing Diagrams

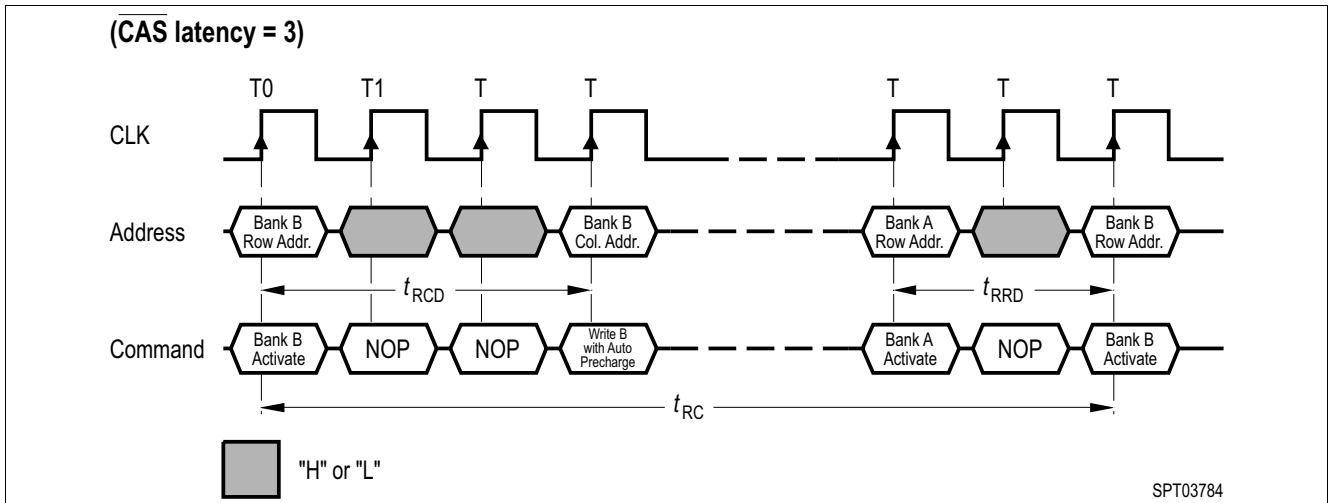


Figure 9 Bank Activate Command Cycle

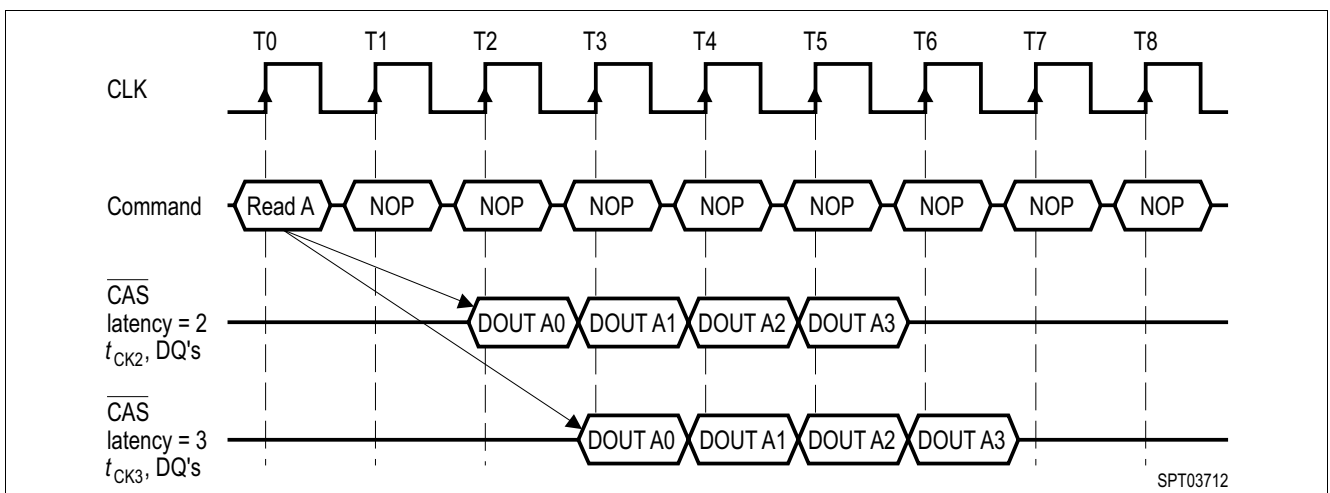


Figure 10 Burst Read Operation

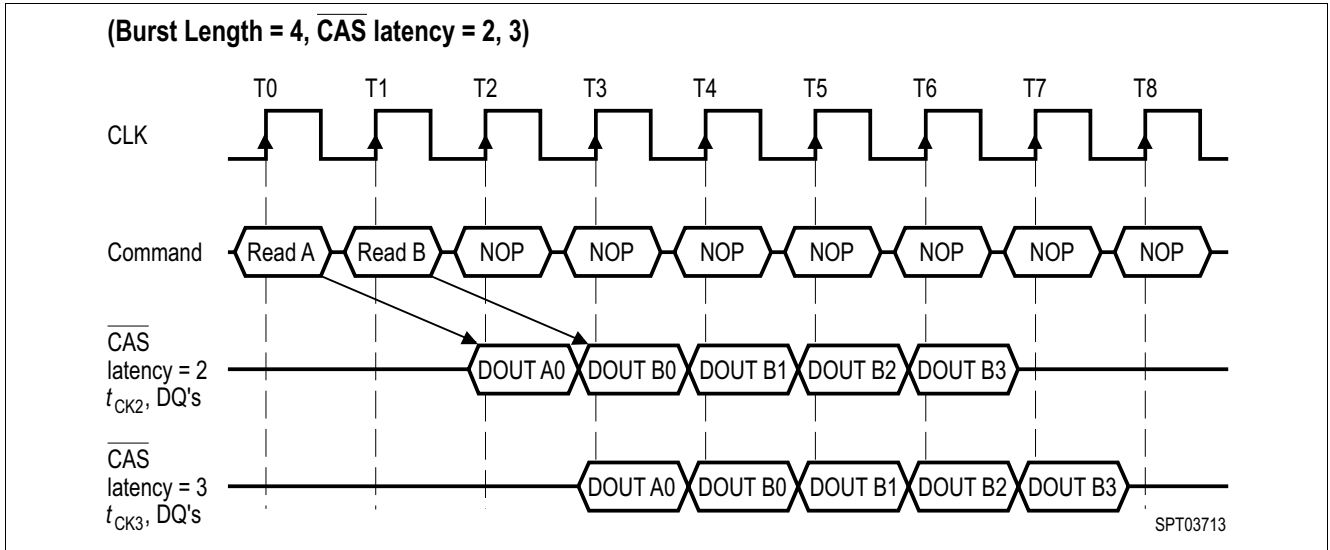


Figure 11 Read Interrupted by a Read

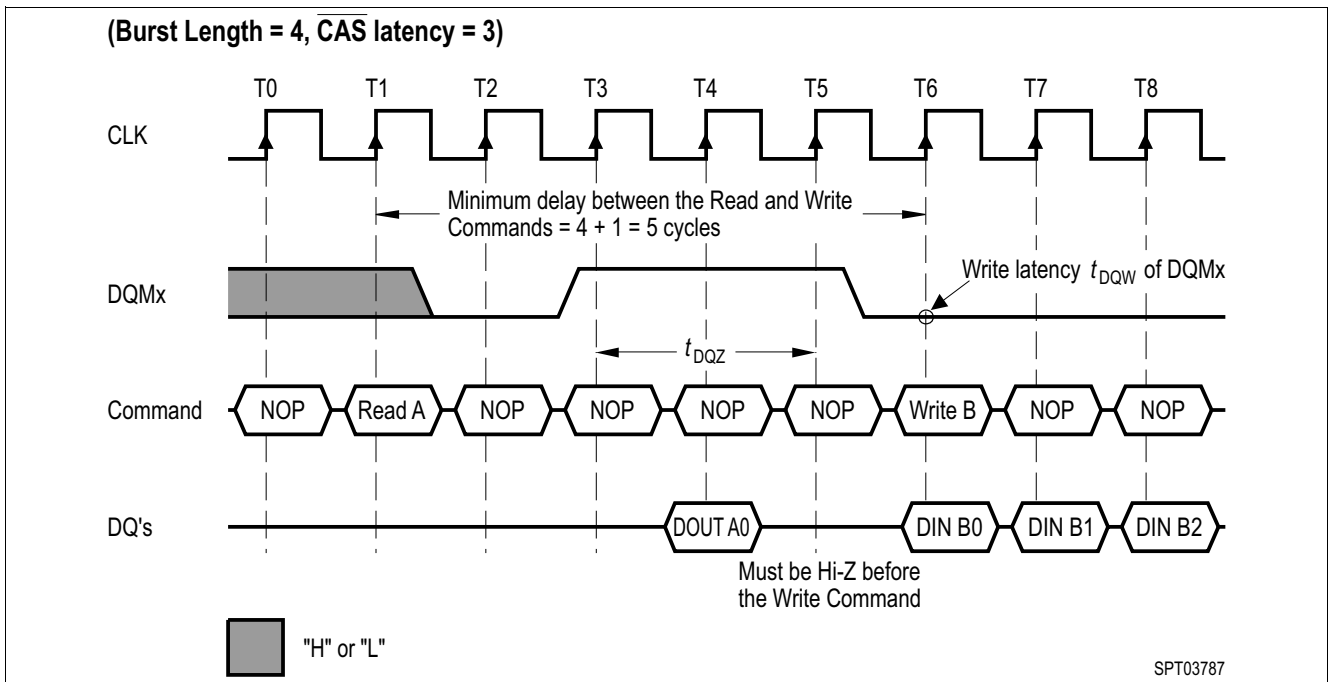


Figure 12 Read to Write Interval

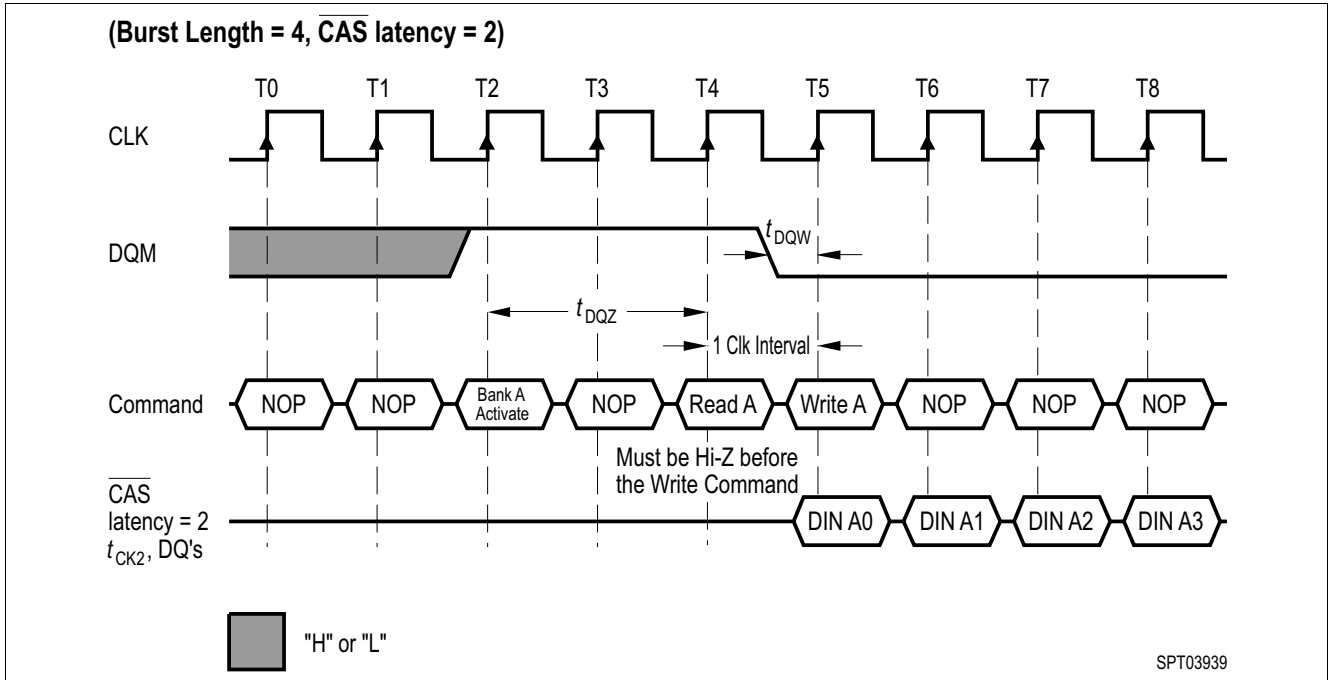


Figure 13 Minimum Read to Write Interval

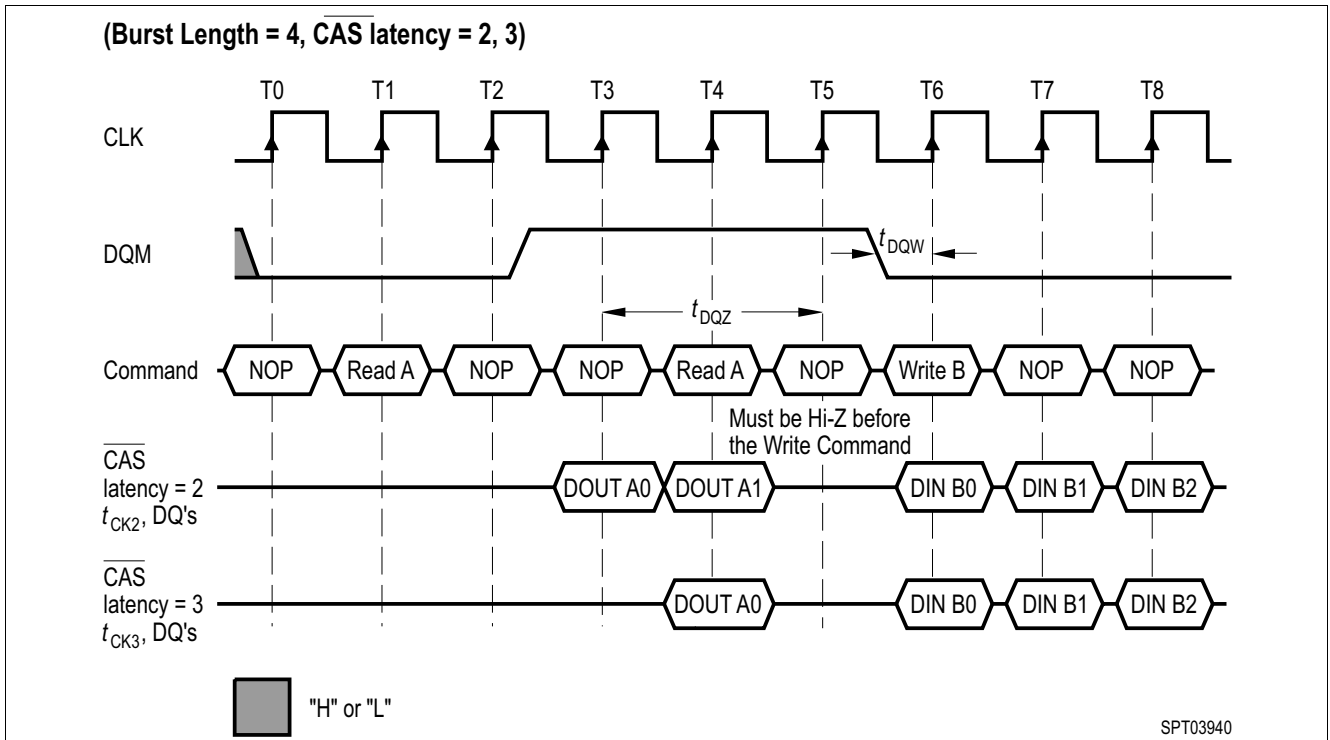


Figure 14 Non-Minimum Read to Write Interval

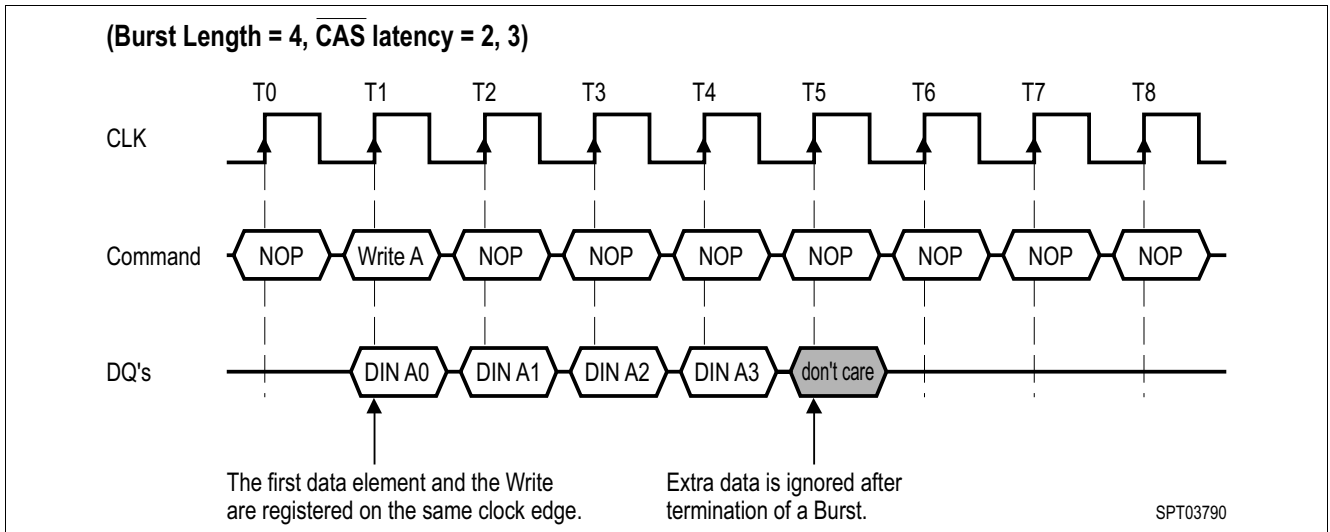


Figure 15 Burst Write Operation

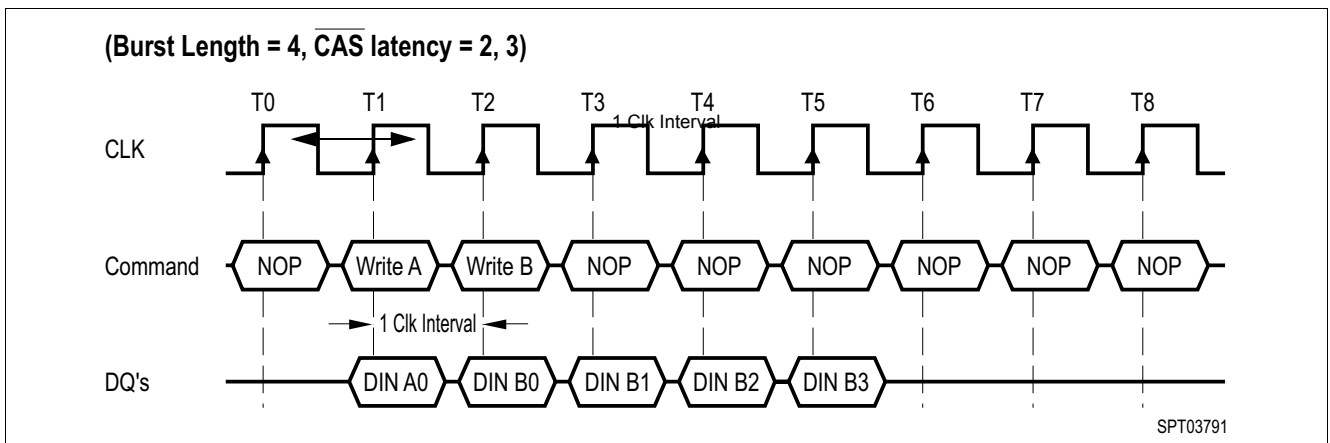


Figure 16 Write Interrupted by a Write

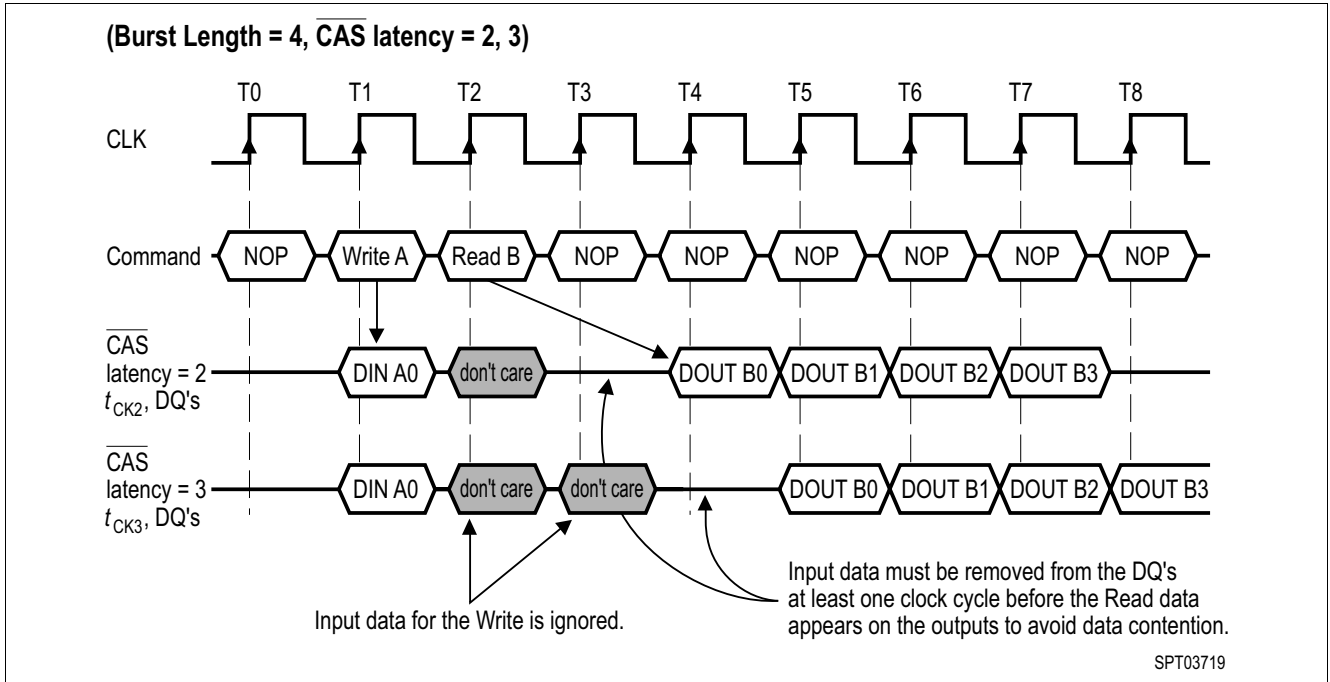


Figure 17 Write Interrupted by a Read

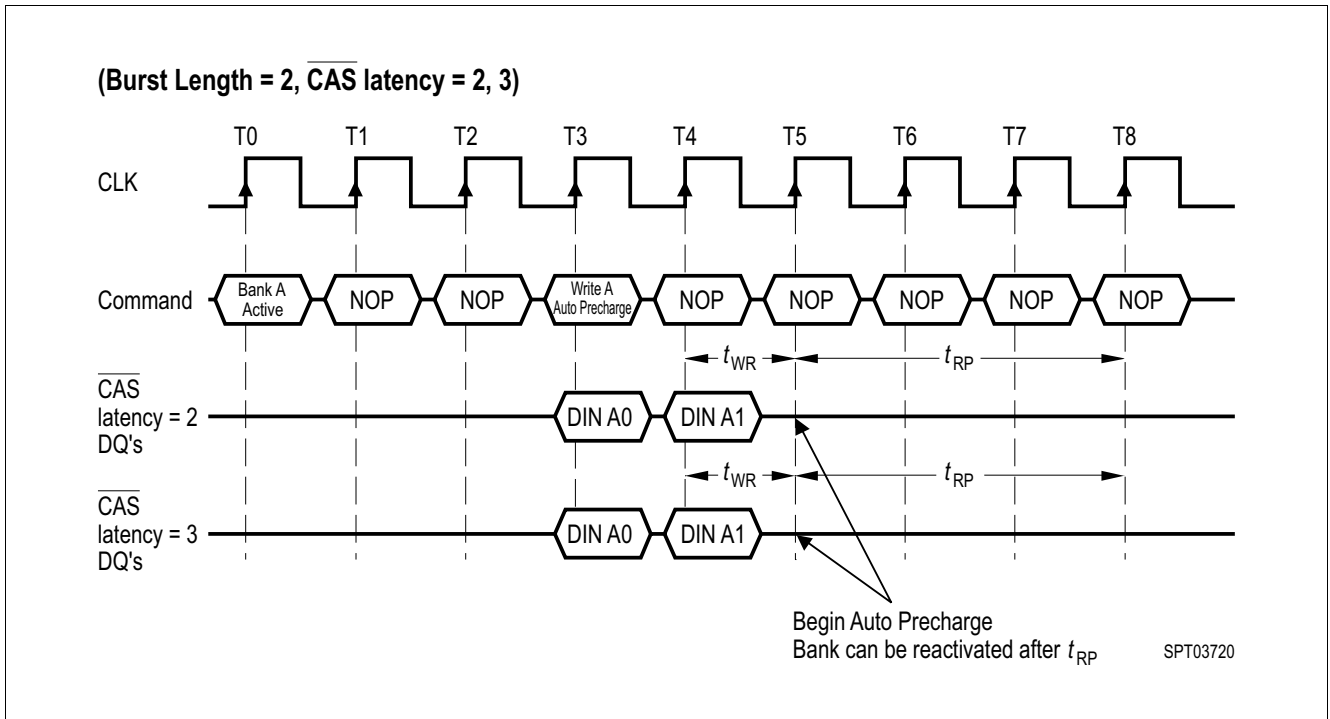


Figure 18 Burst Write with Auto-Precharge

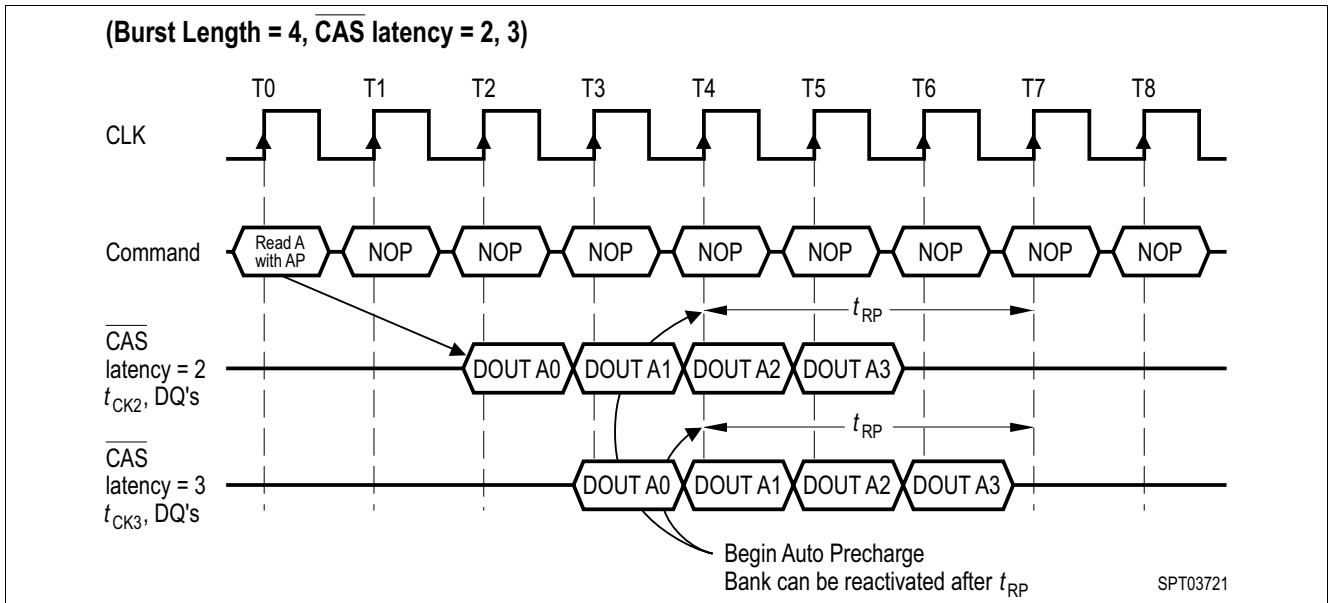


Figure 19 Burst Read with Auto-Precharge

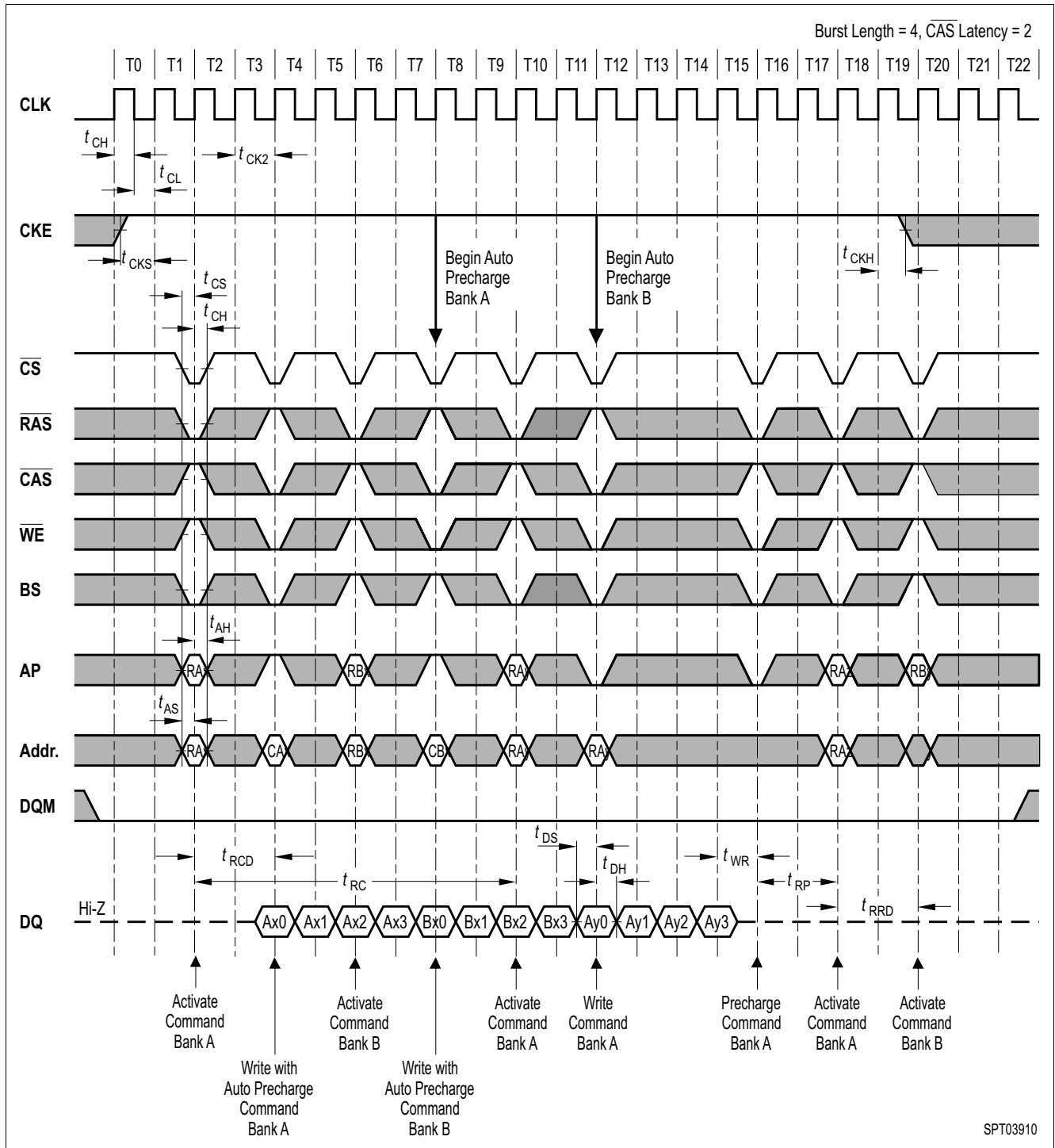


Figure 20 AC Parameters for a Write Timing

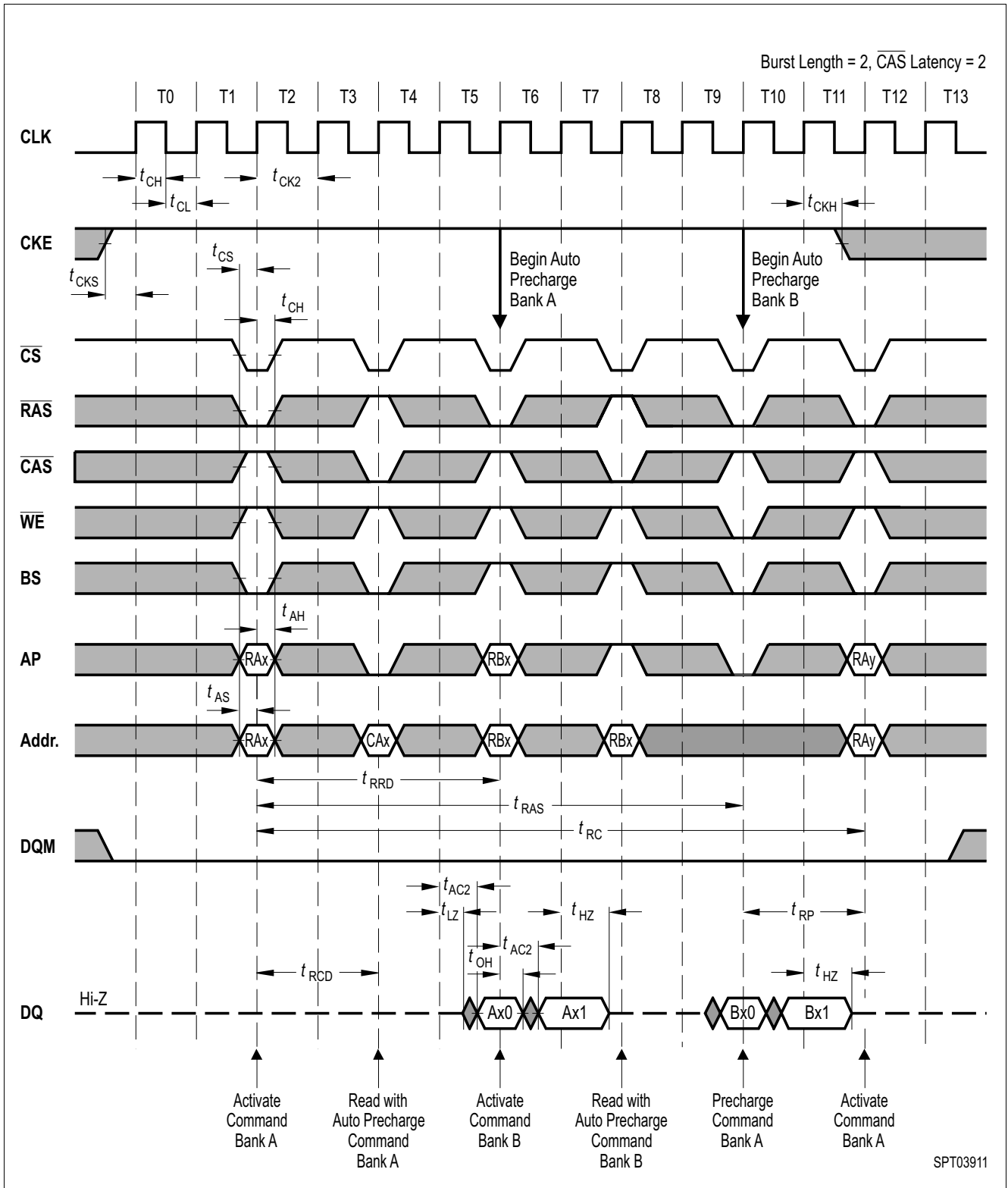


Figure 21 AC Parameters for a Read Timing

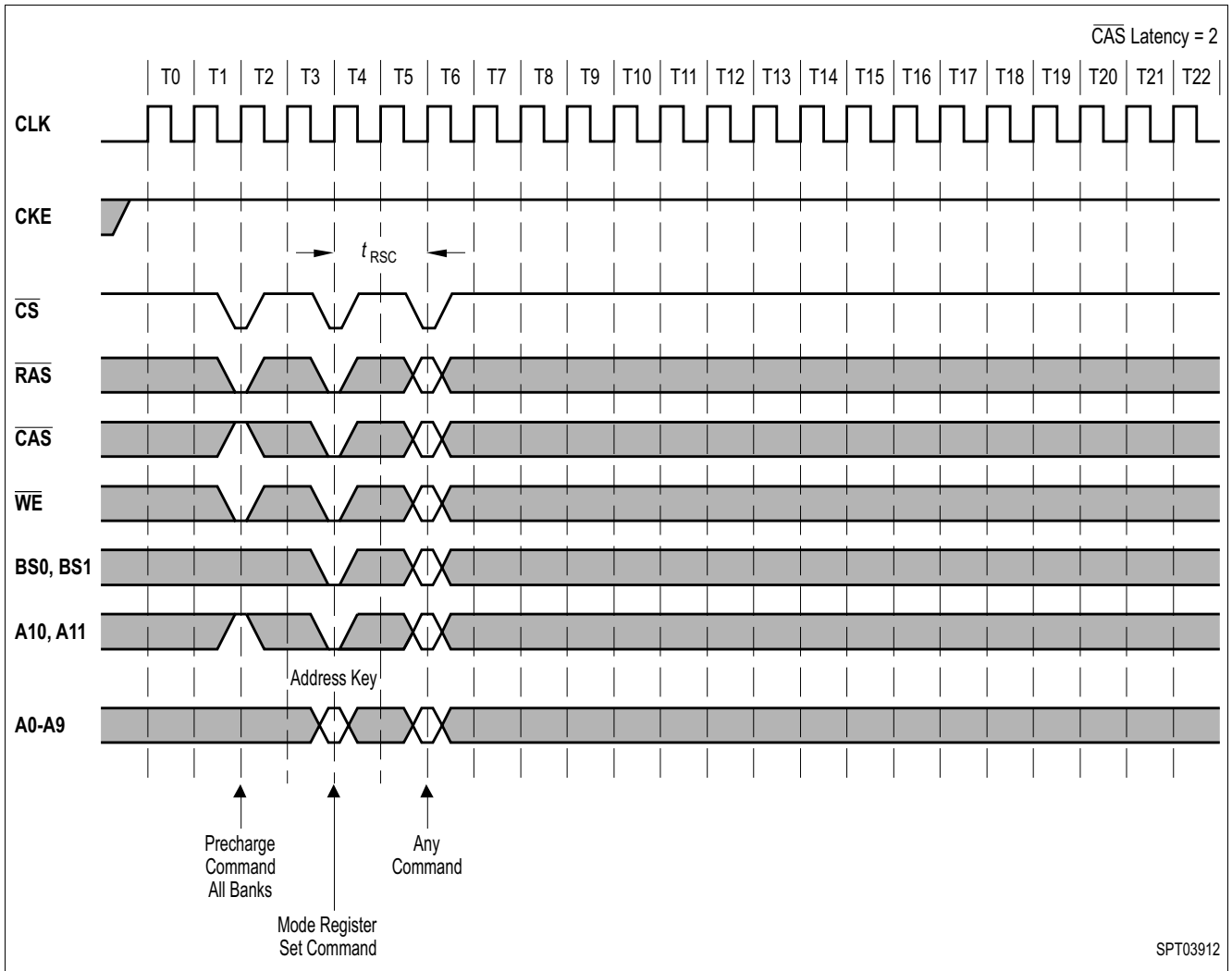


Figure 22 Mode Register Set

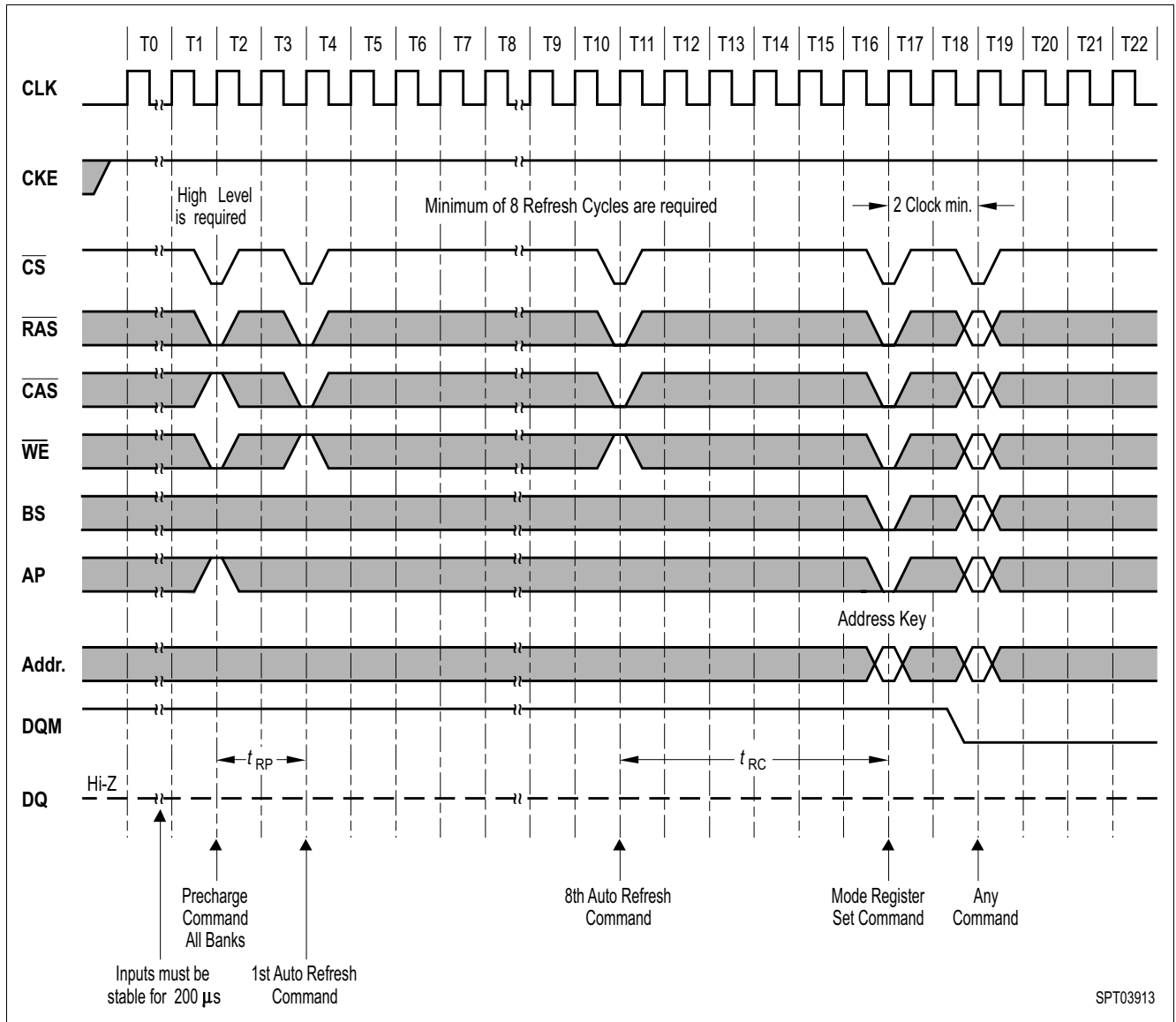


Figure 23 Power on Sequence and Auto Refresh (CBR)

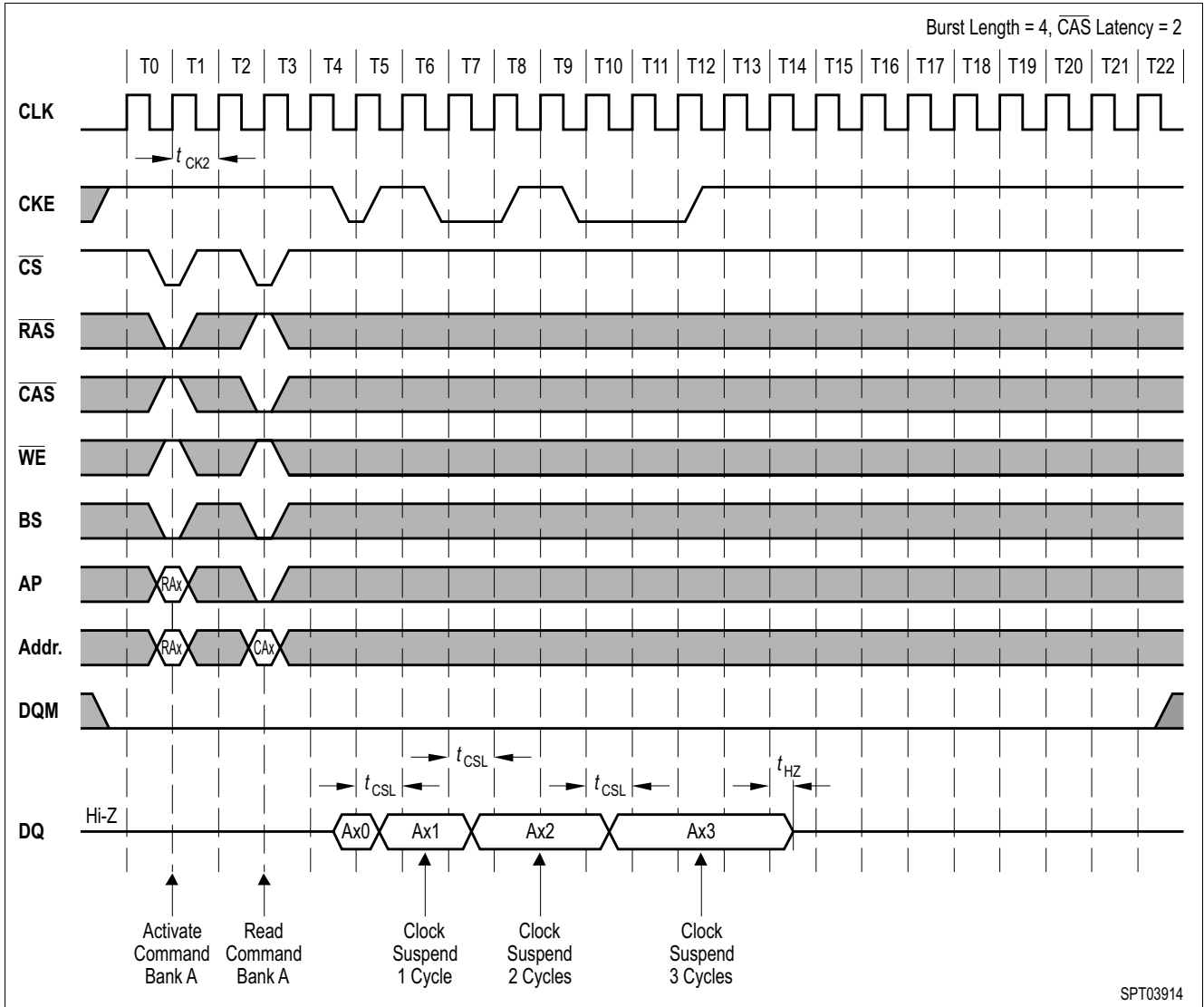
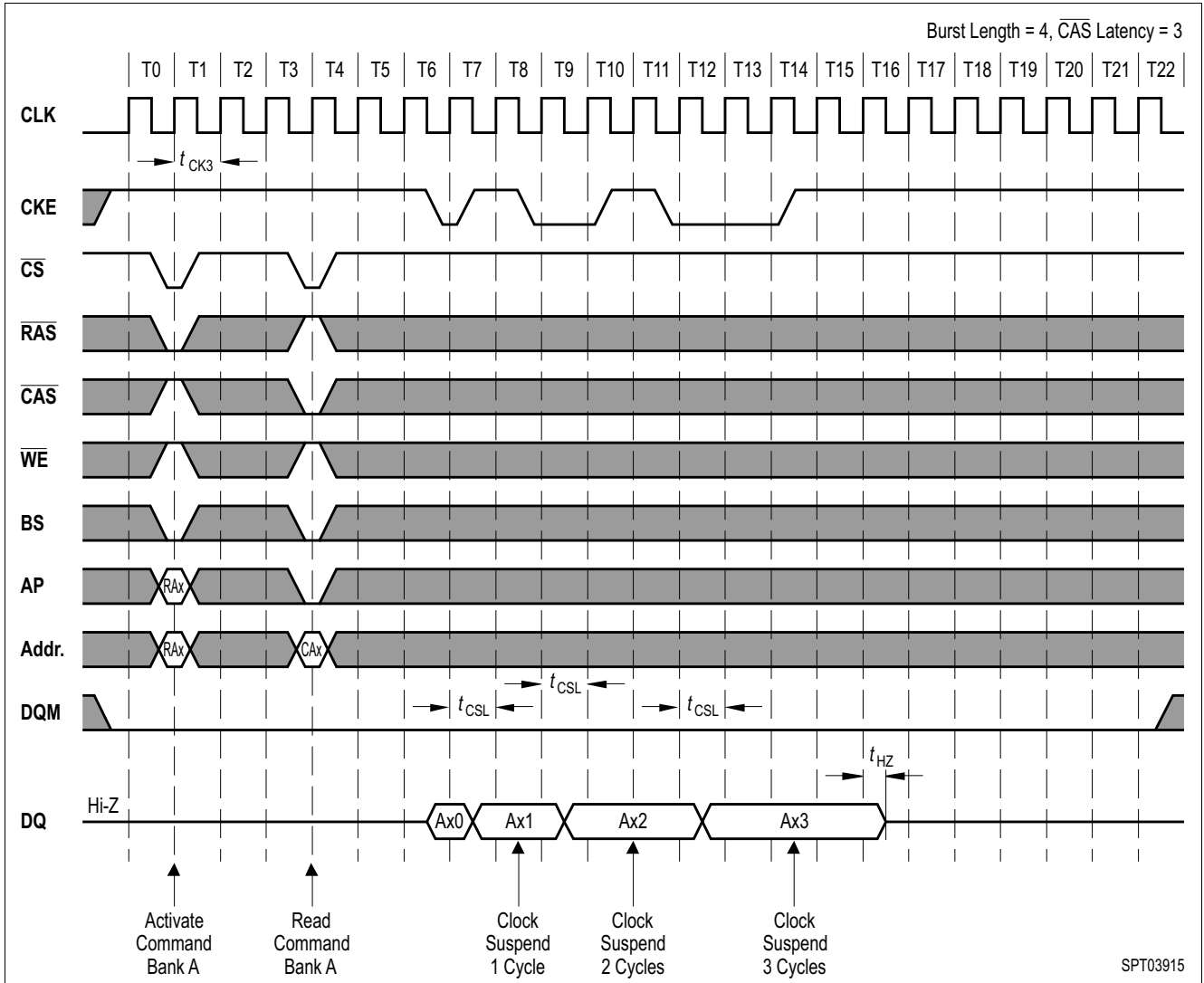


Figure 24 Clock Suspension During Burst Read CAS Latency = 2



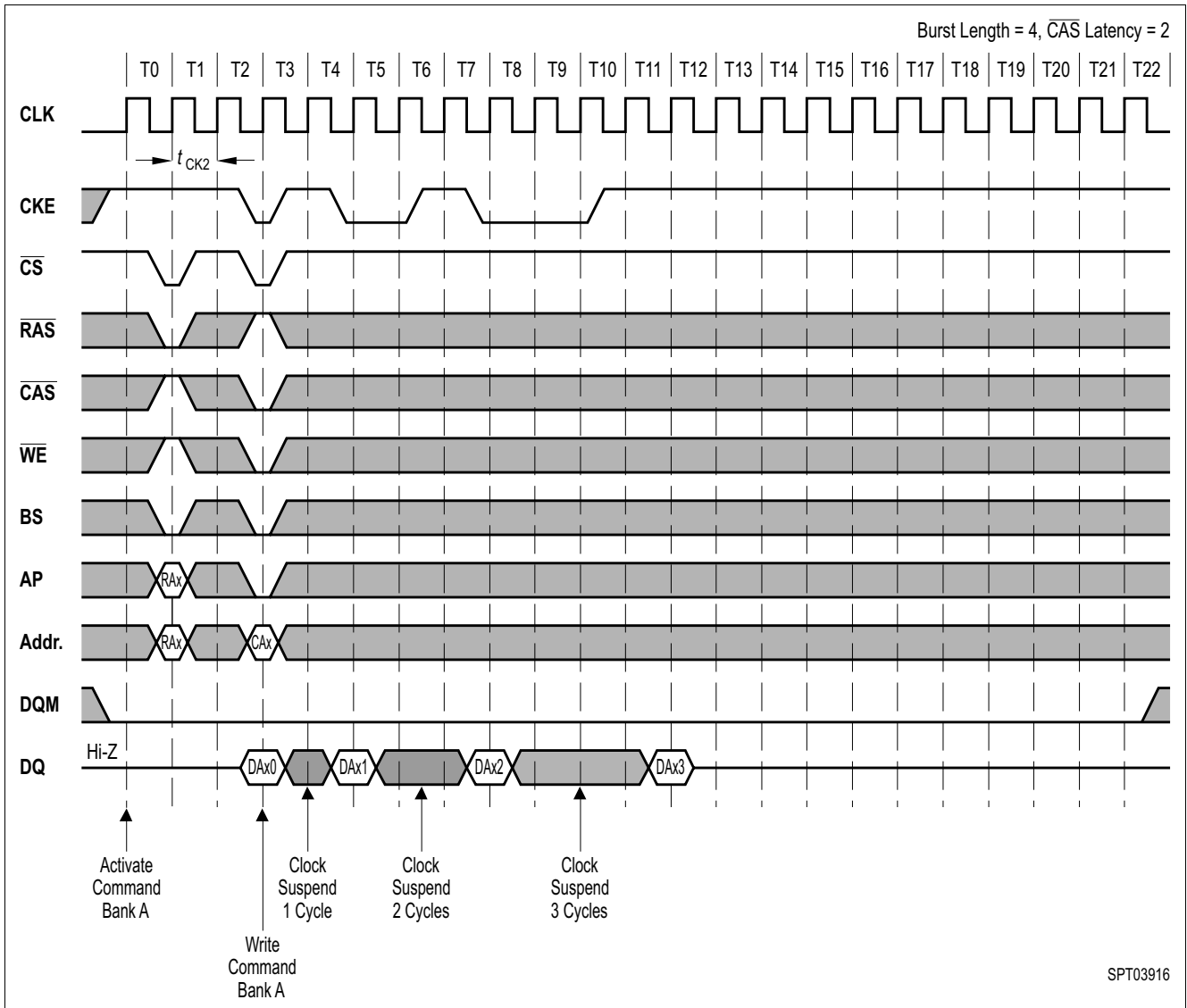


Figure 26 Clock Suspension During Burst Write CAS Latency = 2

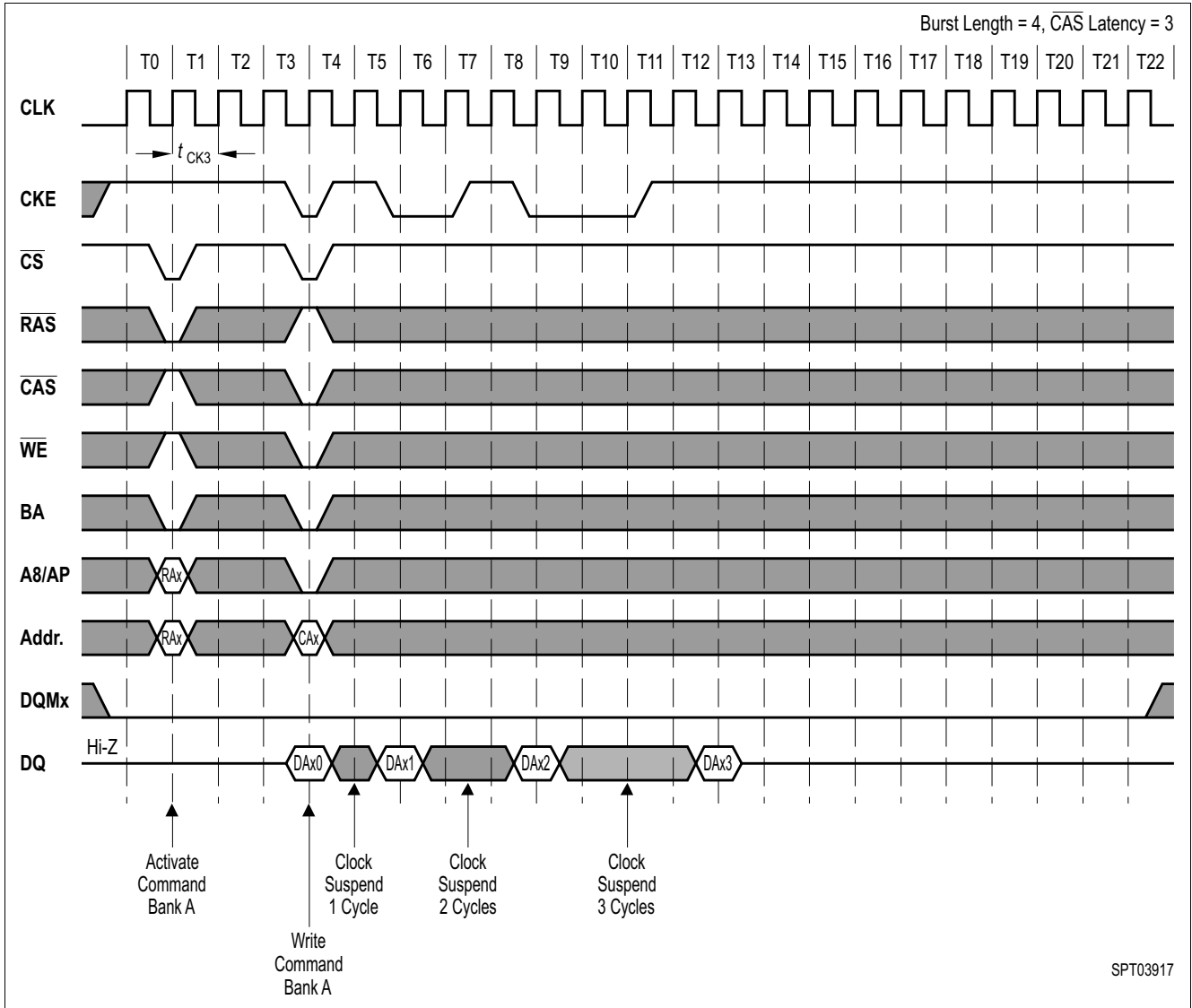


Figure 27 Clock Suspension During Burst Write CAS Latency = 3

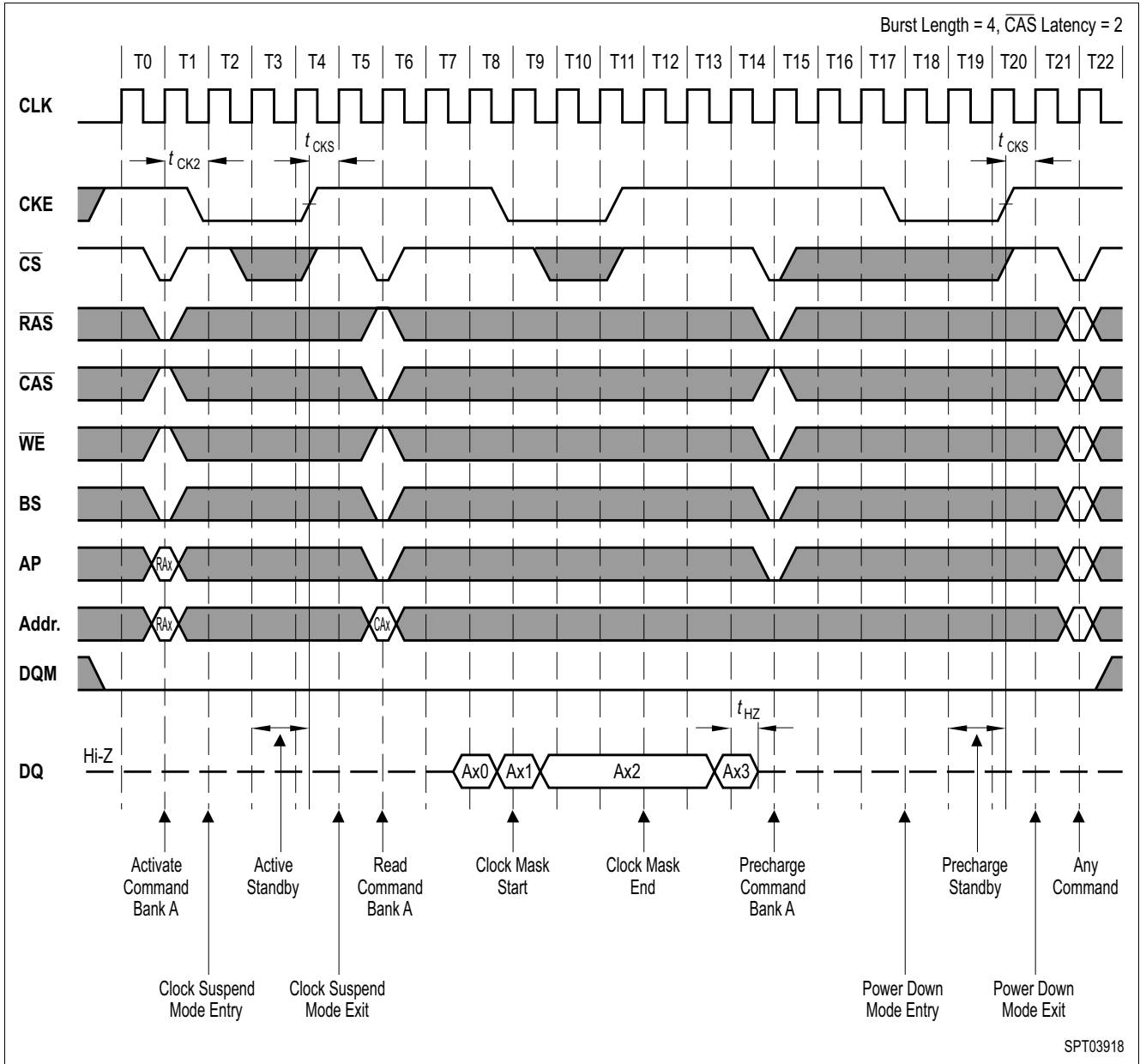


Figure 28 Power Down Mode and Clock Suspend

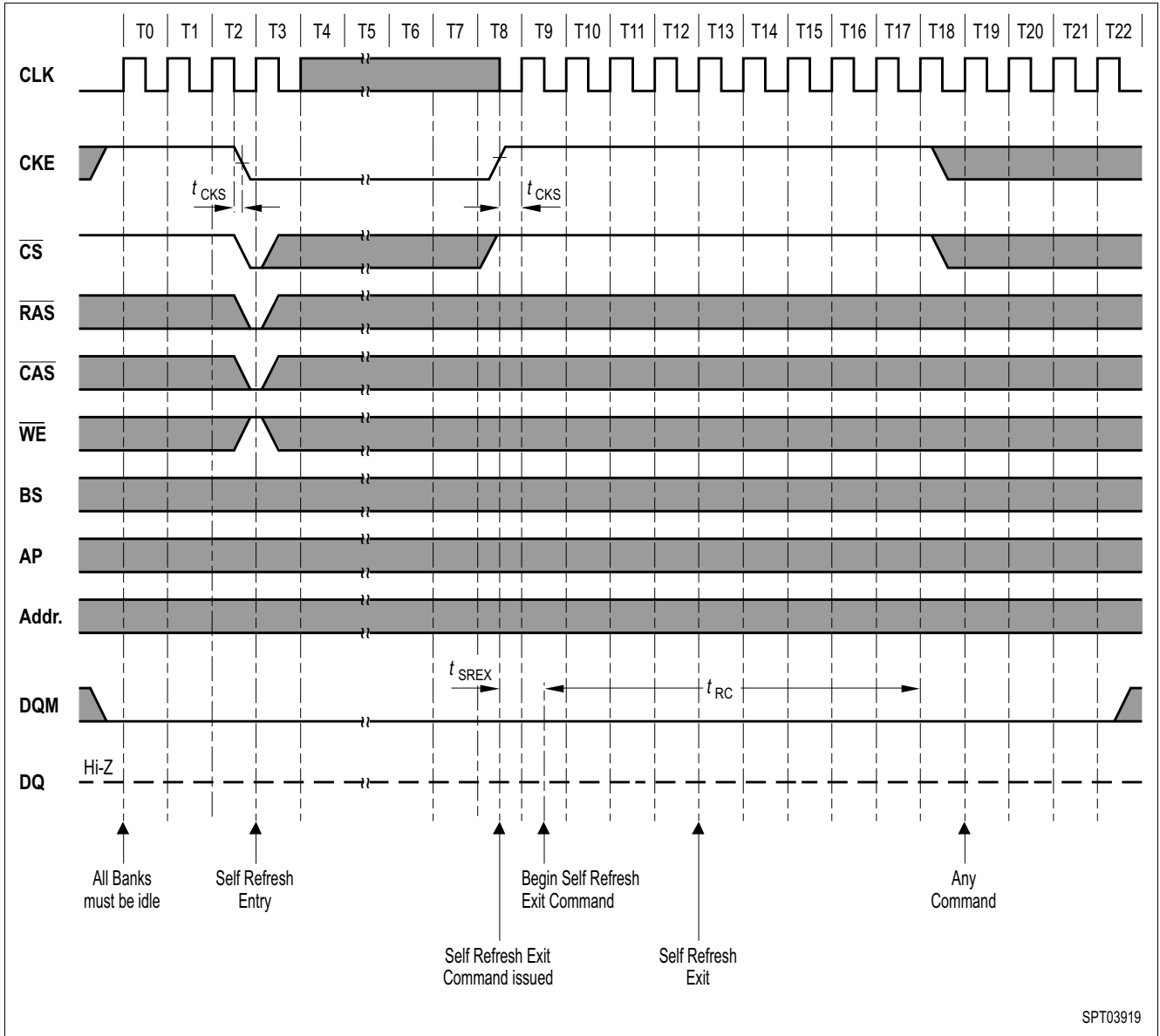


Figure 29 Self Refresh (Entry and Exit)

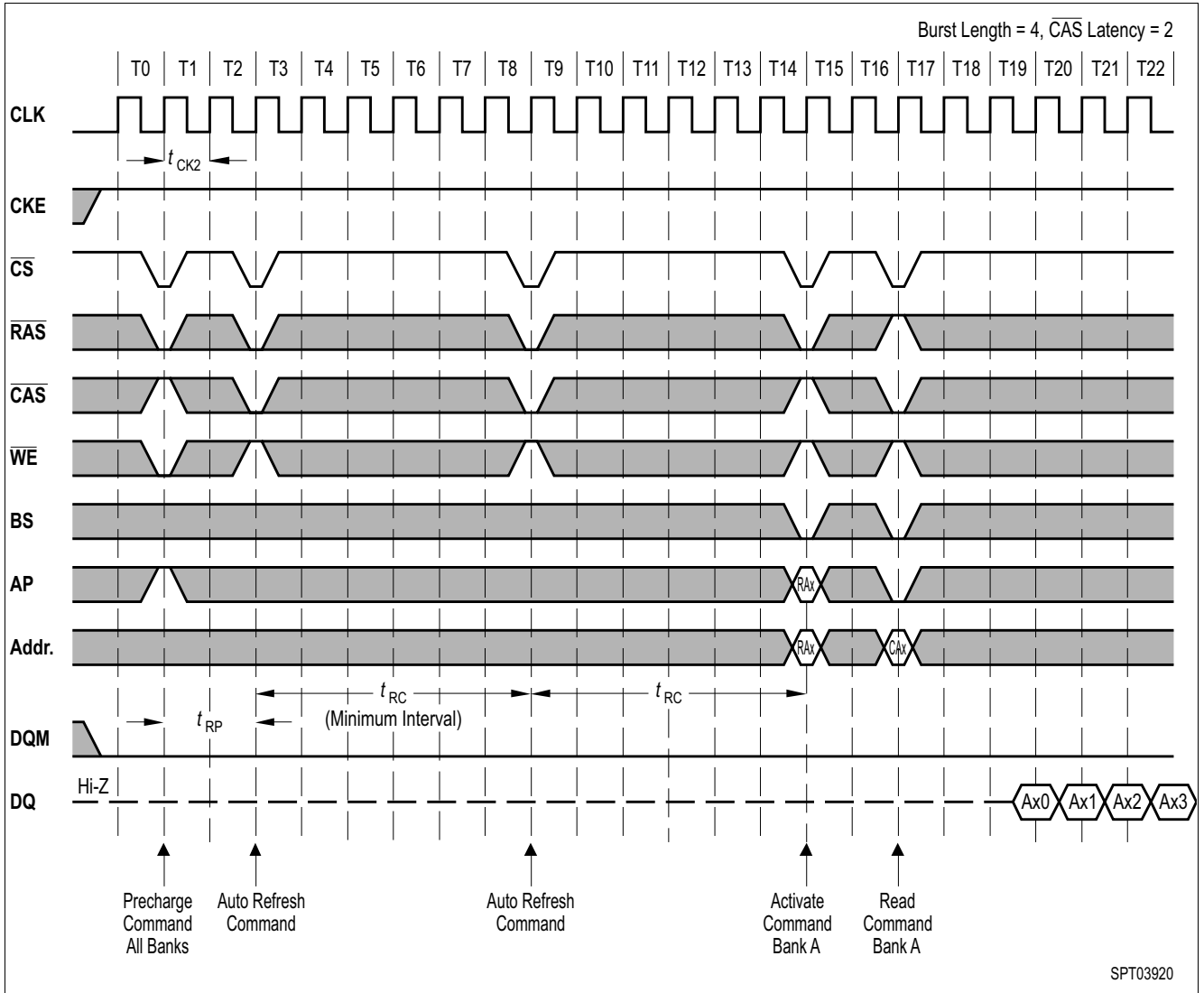


Figure 30 Auto Refresh (CBR)

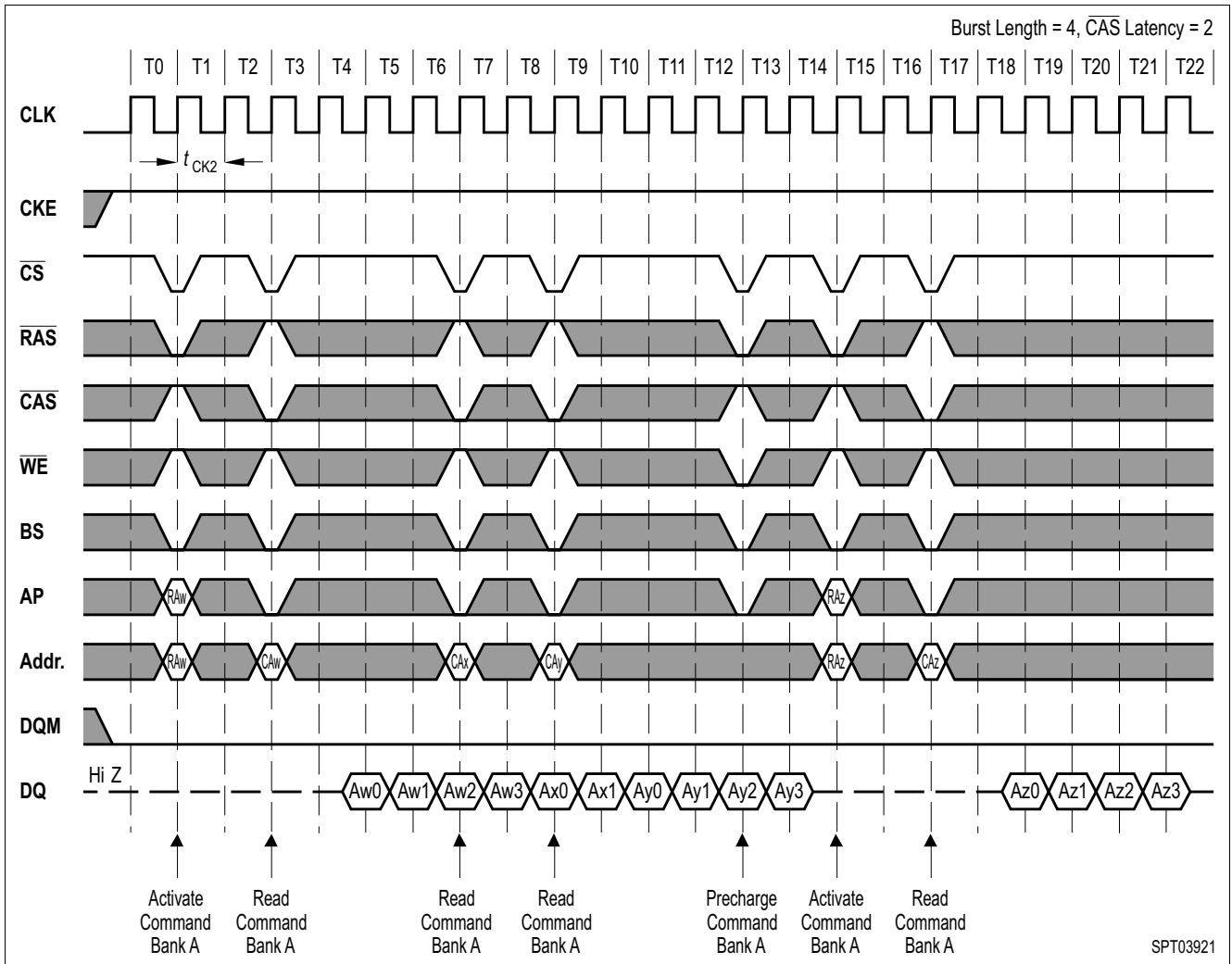


Figure 31 CAS Latency = 2

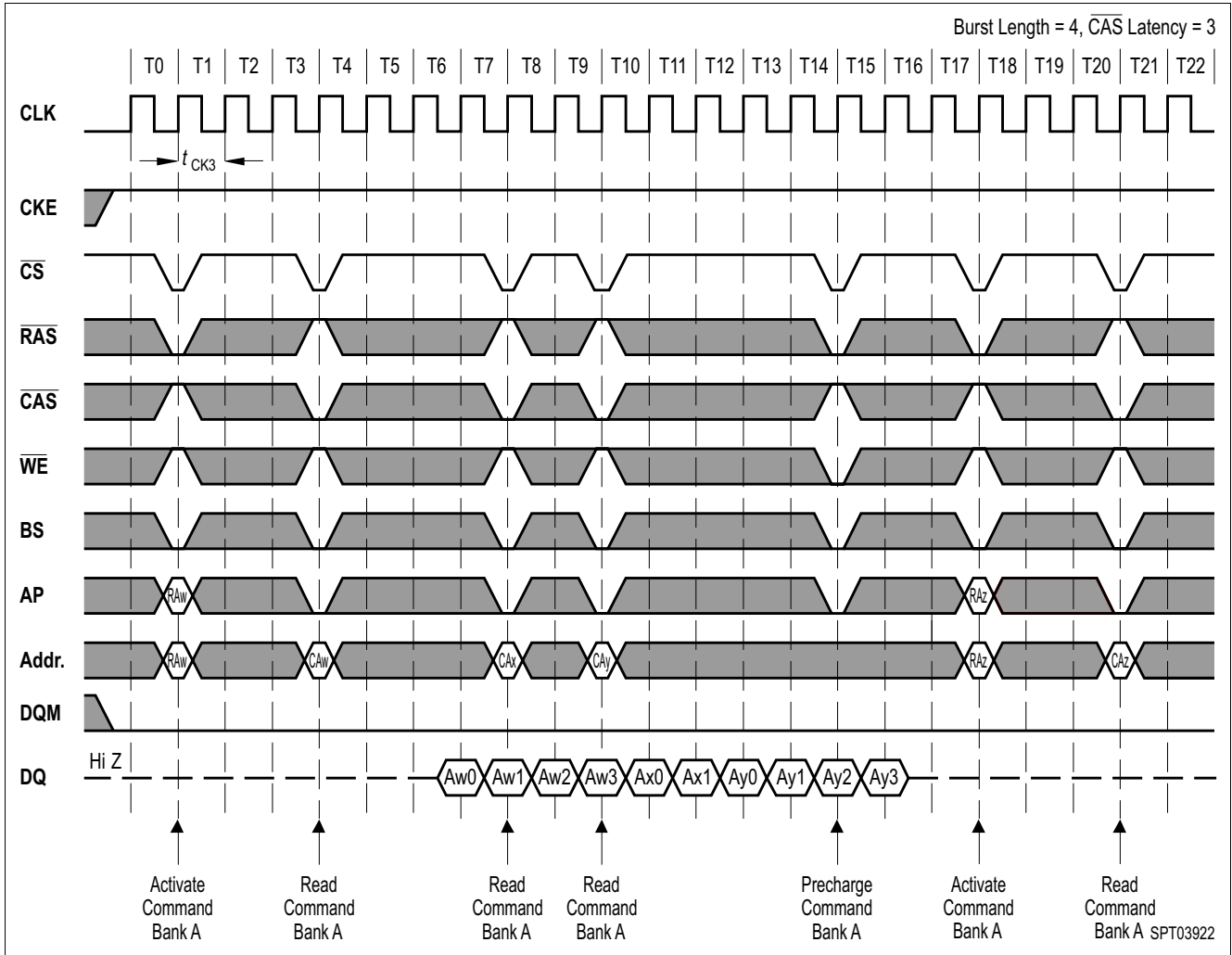


Figure 32 CAS Latency = 3

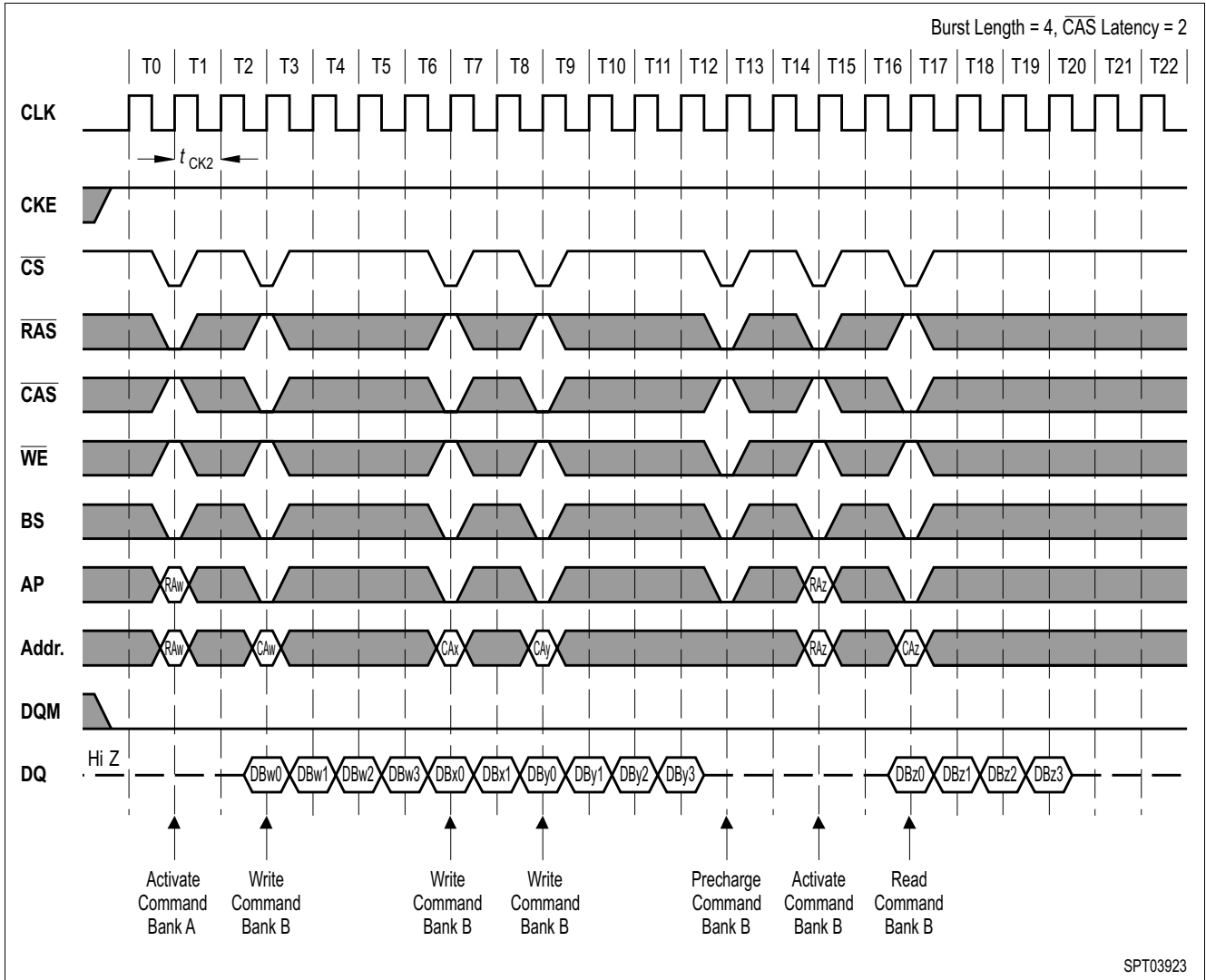


Figure 33 CAS Latency = 2

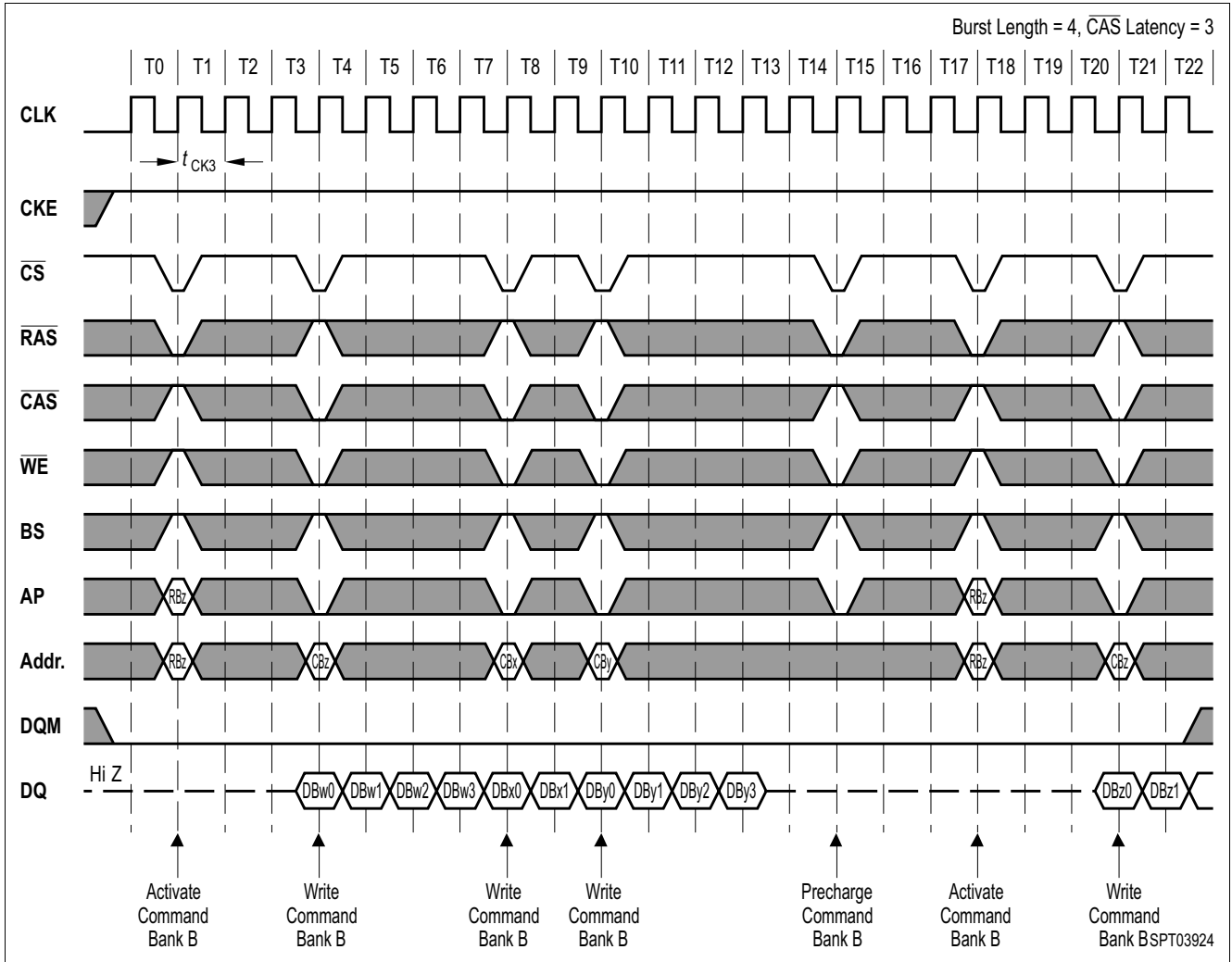


Figure 34 CAS Latency = 3

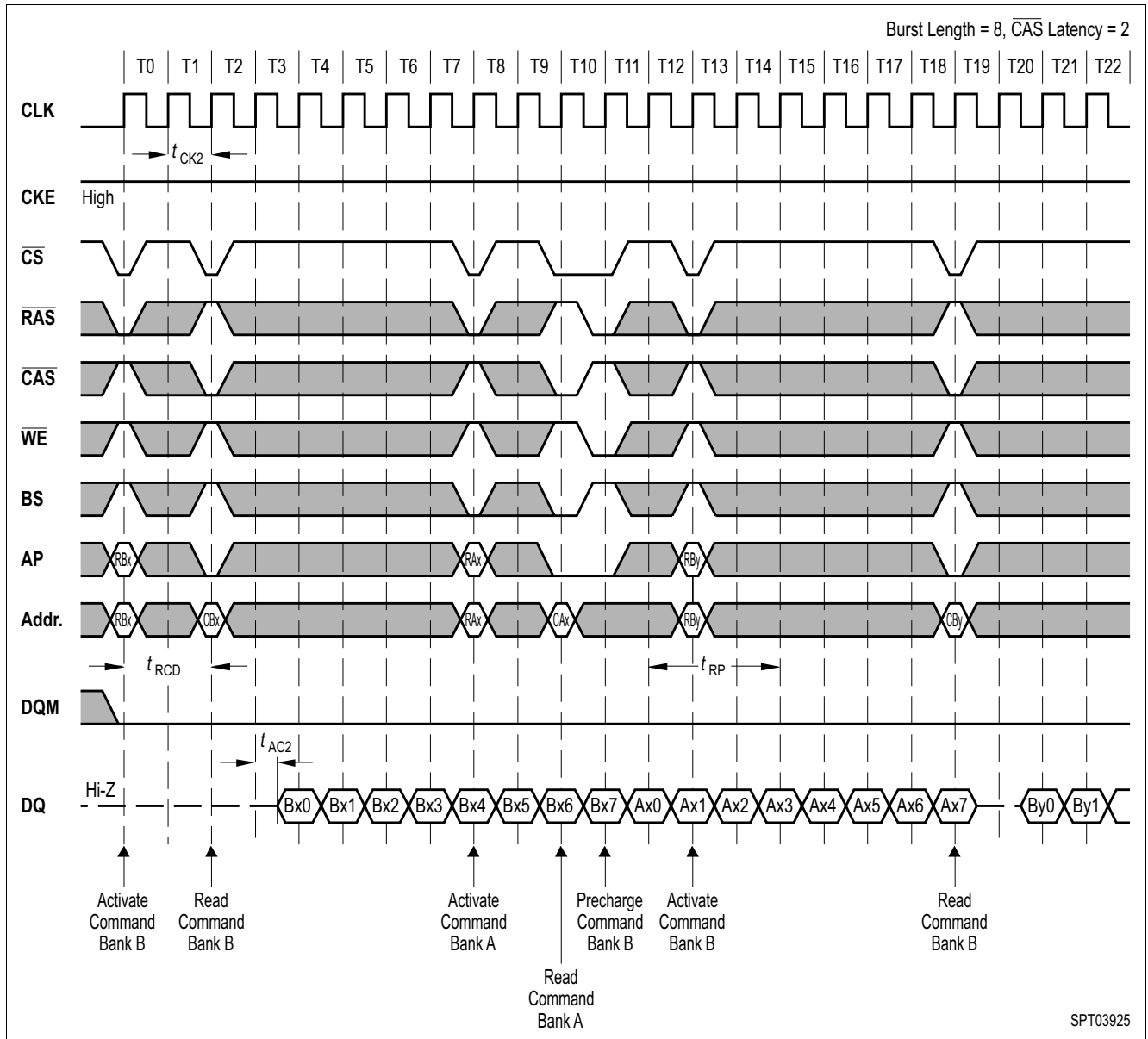


Figure 35 CAS Latency = 2

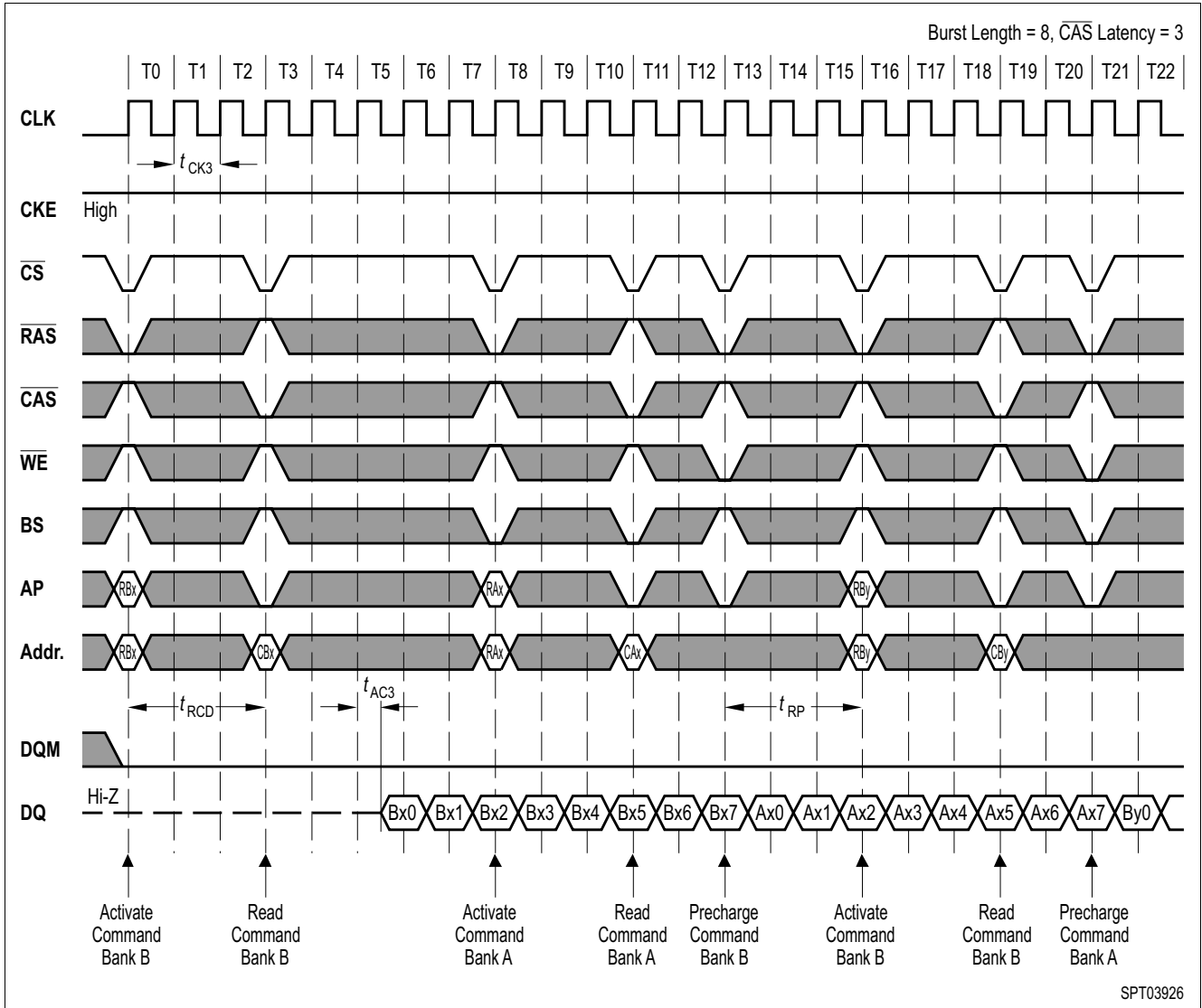


Figure 36 CAS Latency = 3

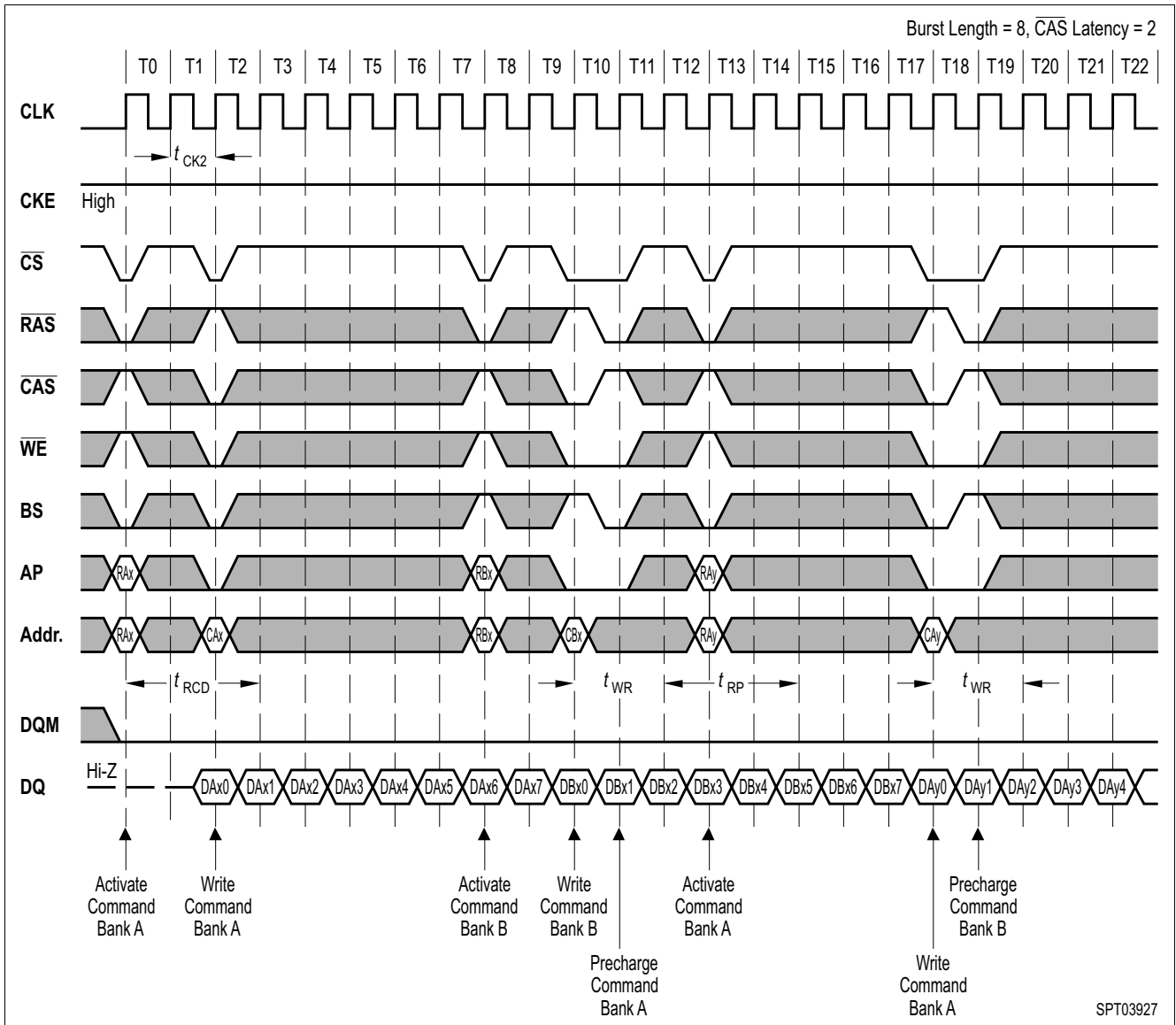


Figure 37 CAS Latency = 2

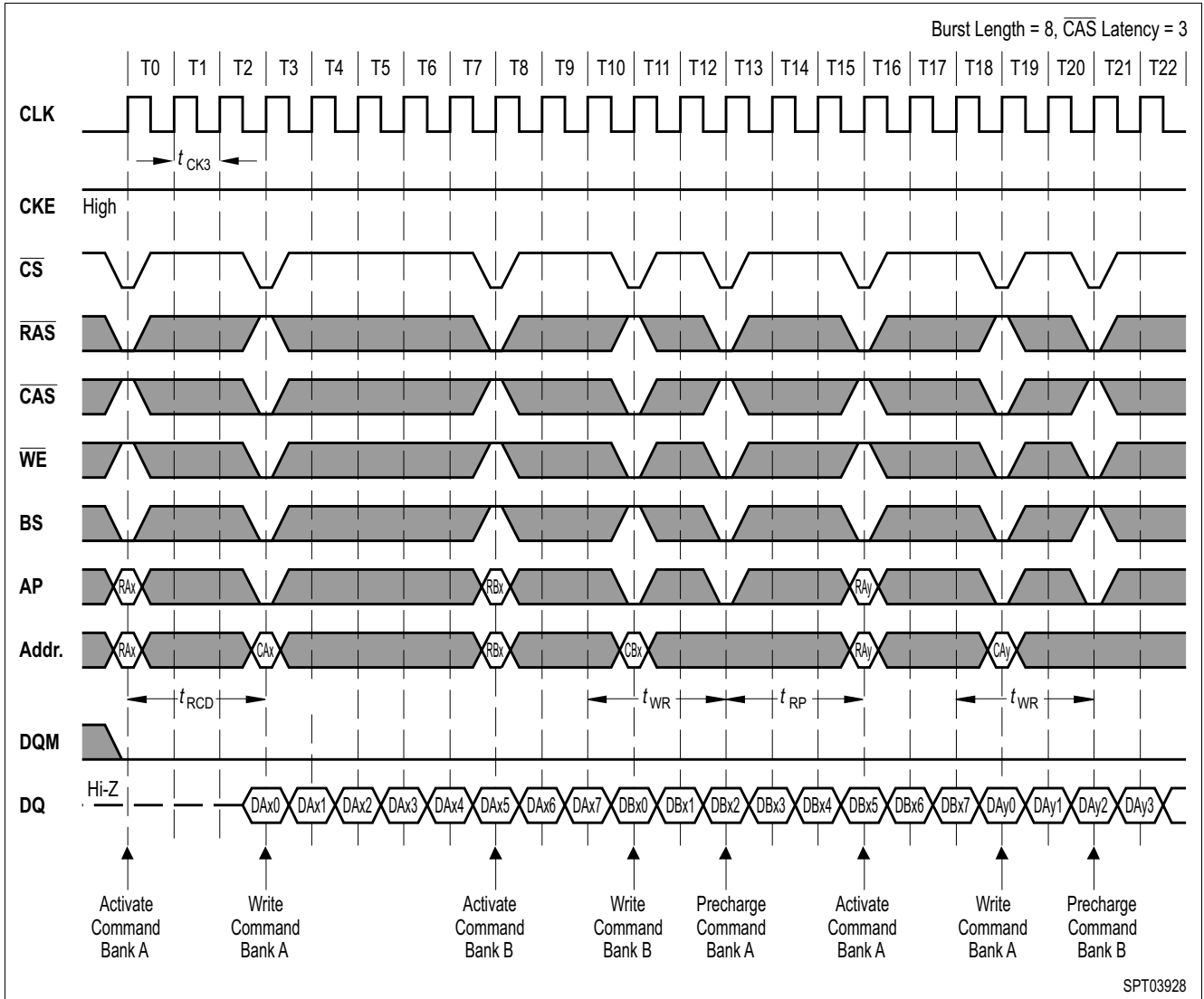


Figure 38 CAS Latency = 3

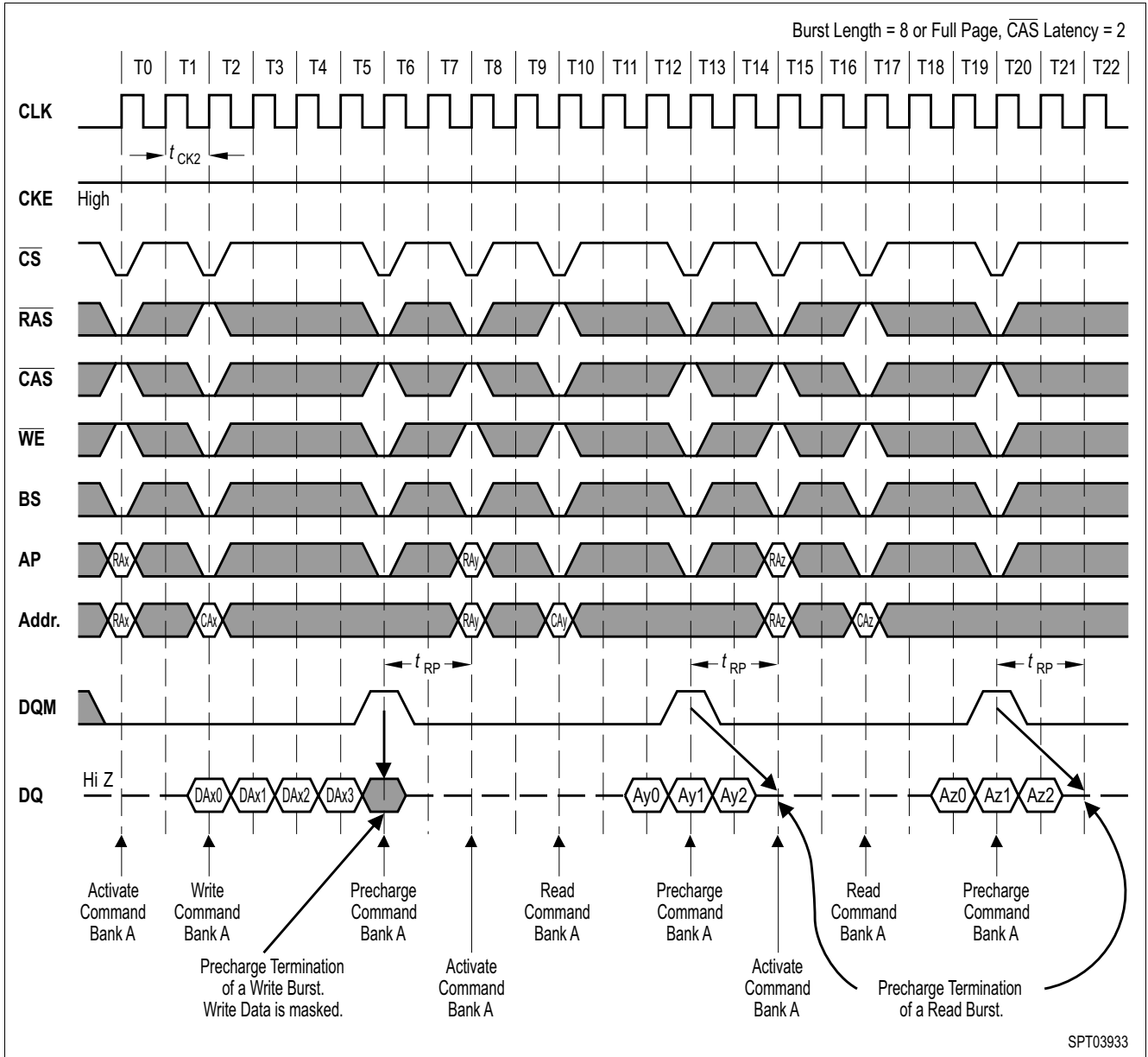


Figure 39 CAS Latency = 2

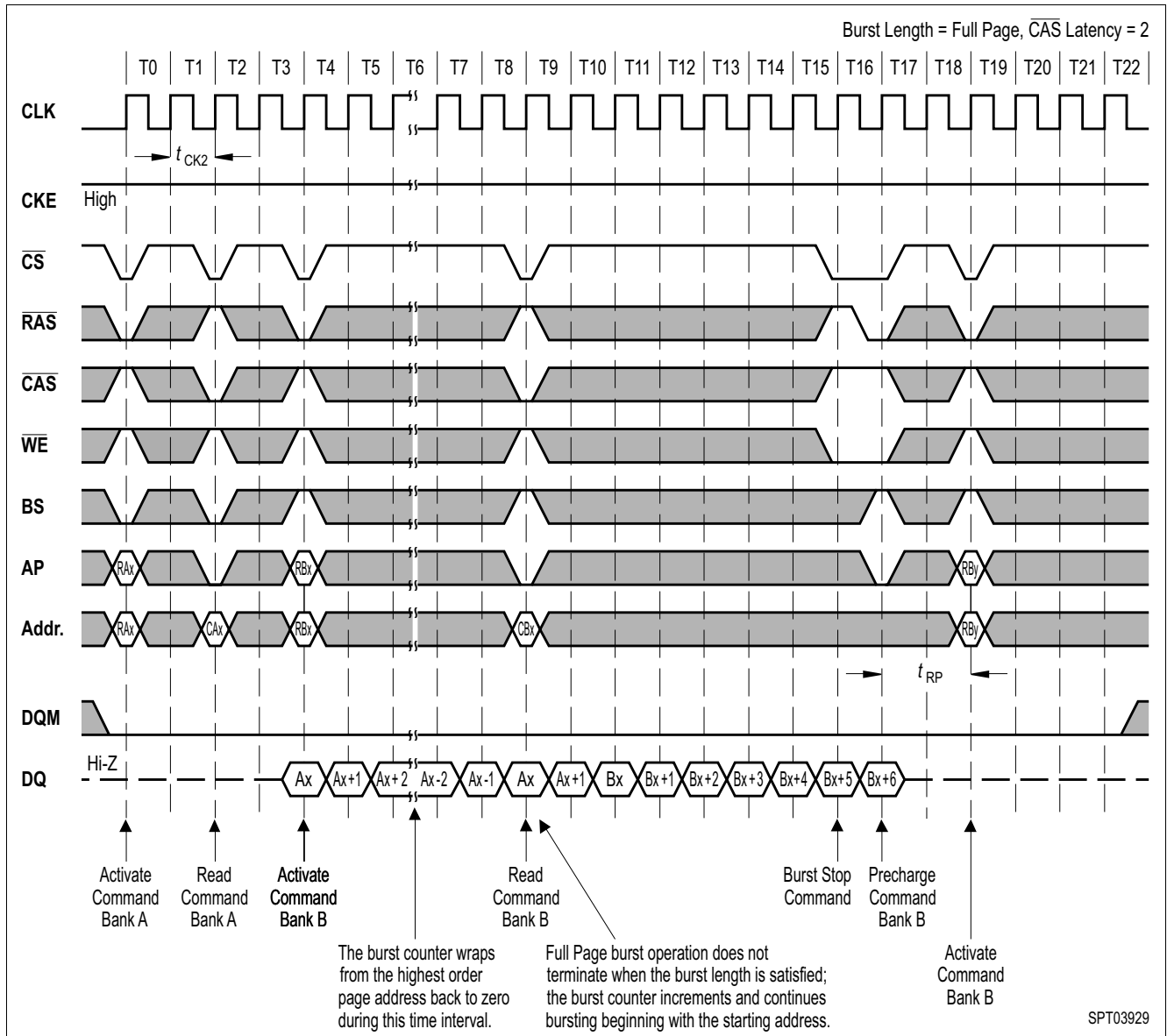


Figure 40 Full Page Burst Read, CAS Latency = 2

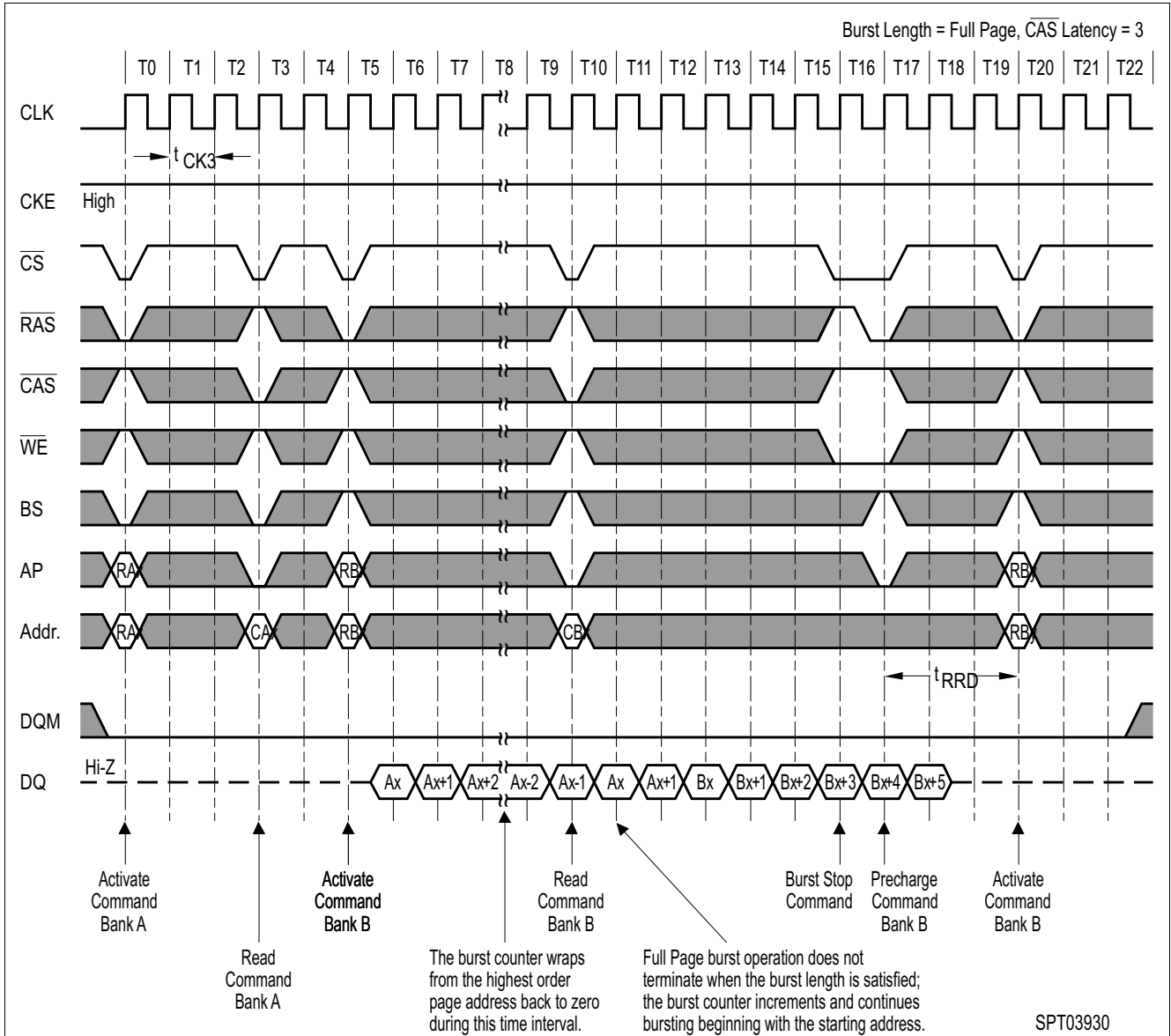


Figure 41 Full Page Burst Write, CAS Latency = 3

6 Package Outlines

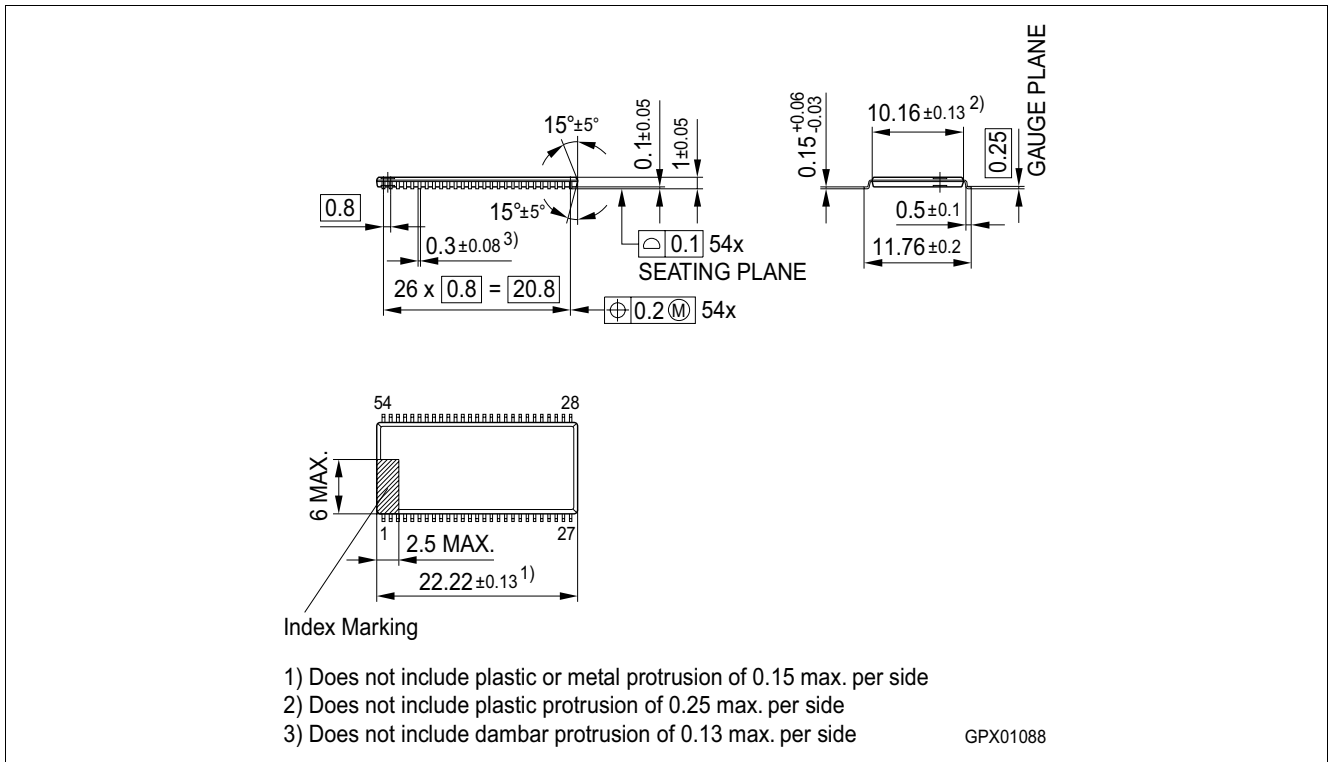


Figure 42 Package Outline PG-TSOPII-54-4 (top view)

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