



Integrated  
Circuit  
Systems, Inc.

# ICS853058

## 8:1, DIFFERENTIAL-TO- 3.3V OR 2.5V LVPECL/ECL CLOCK MULTIPLEXER

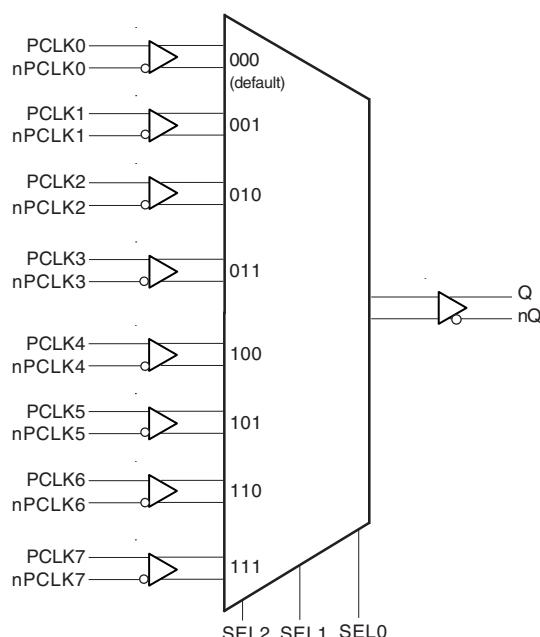
### GENERAL DESCRIPTION

 The ICS853058 is an 8:1 Differential-to-3.3V or 2.5V LVPECL / ECL Clock Multiplexer which can operate up to 2.8GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853058 has 8 differential selectable clock inputs. The PCLK, nPCLK input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL2 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 000 selects PCLK0, nPCLK0).

### FEATURES

- High speed 8:1 differential multiplexer
- One differential 3.3V or 2.5V LVPECL output
- Eight selectable differential PCLK, nPCLK inputs
- PCLK<sub>x</sub>, nPCLK<sub>x</sub> pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2.8GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLK<sub>x</sub> input
- RMS phase jitter @155.52MHz: 0.212ps (typical)
- Part-to-part skew: 325ps (maximum)
- Propagation delay: 450ps (maximum)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to  $3.465V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -3.465V$  to  $-2.375V$
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

### BLOCK DIAGRAM



### PIN ASSIGNMENT

PCLK0	1	24	PCLK7
nPCLK0	2	23	nPCLK7
PCLK1	3	22	PLCK6
nPCLK1	4	21	nPCLK6
V <sub>CC</sub>	5	20	V <sub>CC</sub>
SEL0	6	19	Q
SEL1	7	18	nQ
SEL2	8	17	V <sub>EE</sub>
PCLK2	9	16	PCLK5
nPCLK2	10	15	nPCLK5
PCLK3	11	14	PCLK4
nPCLK3	12	13	nPCLK4

**ICS853058**  
24-Lead, 173-MIL TSSOP  
4.4mm x 7.8mm x 0.92mm body package  
G Package  
Top View



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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential clock input.
2	nPCLK0	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK1	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
5, 20	$V_{cc}$	Power		Positive supply pins.
6, 7, 8	SEL0, SEL1, SEL2	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
9	PCLK2	Input	Pulldown	Non-inverting differential clock input.
10	nPCLK2	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential clock input.
12	nPCLK3	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
13	nPCLK4	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
14	PCLK4	Input	Pulldown	Non-inverting differential clock input.
15	nPCLK5	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
16	PCLK5	Input	Pulldown	Non-inverting differential clock input.
17	$V_{ee}$	Power		Negative supply pin.
18, 19	nQ, Q	Output		Differential output pair. LVPECL interface levels.
21	nPCLK6	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
22	PCLK6	Input	Pulldown	Non-inverting differential clock input.
23	nPCLK7	Input	Pullup/Pulldown	Inverting differential clock input. $V_{cc}/2$ default when left floating.
24	PCLK7	Input	Pulldown	Non-inverting differential clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.



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TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Pulldown Resistor			75		$k\Omega$
$R_{VCC/2}$	Pullup/Pulldown Resistor			50		$k\Omega$

TABLE 3. CONTROL INPUT FUNCTION TABLE

Control Inputs			Outputs	
SEL2	SEL1	SEL0	Q	nQ
0	0	0	PCLK0	nPCLK0
0	0	1	PCLK1	nPCLK1
0	1	0	PCLK2	nPCLK2
0	1	1	PCLK3	nPCLK3
1	0	0	PCLK4	nPCLK4
1	0	1	PCLK5	nPCLK5
1	1	0	PCLK6	nPCLK6
1	1	1	PCLK7	nPCLK7



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**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	5.5V (LVPECL mode, $V_{EE} = 0$ )
Negative Supply Voltage, $V_{EE}$	-5.5V (ECL mode, $V_{CC} = 0$ )
Inputs, $V_I$ (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, $V_I$ (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, $TA$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$	70°C/W (0 mps) (Junction-to-Ambient)

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.375$  TO  $3.465V$ ,  $V_{EE} = 0V$ ;  $TA = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage			2.375	3.3	3.465	V
$I_{EE}$	Power Supply Current					47	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = 2.375$  TO  $3.465V$ ,  $V_{EE} = 0V$ ;  $TA = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	SEL0:SEL2		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	SEL0:SEL2		-0.3		0.8	V
$I_{IH}$	Input High Current	SEL0:SEL2	$V_{CC} = V_{IN} = 3.465V$ , $V_{CC} = V_{IN} = 2.625V$			150	μA
$I_{IL}$	Input Low Current	SEL0:SEL2	$V_{CC} = 3.465V$ , $V_{IN} = 0V$ , $V_{CC} = 2.625V$ , $V_{IN} = 0V$	-150			μA

**TABLE 4C. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.375$  TO  $3.465V$ ,  $V_{EE} = 0V$ ;  $TA = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK0:PCLK7 nPCLK0:nPCLK7	$V_{CC} = V_{IN} = 3.465V$			150	μA
$I_{IL}$	Input Low Current	PCLK0:PCLK7	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-10			μA
		nPCLK0:nPCLK7	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-150			μA
$V_{PP}$	Peak-to-Peak Input Voltage			0.15		1.5	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2			1.2		$V_{CC}$	V
$V_{OH}$	Output High Voltage Voltage; NOTE 3			$V_{CC} - 1.125$		$V_{CC} - 0.935$	V
$V_{OL}$	Output Low Voltage; NOTE 3			$V_{CC} - 1.895$		$V_{CC} - 1.670$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for PCLKx, nPCLKx is  $V_{CC} + 0.3V$ .

NOTE 3: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .



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**TABLE 4D. ECL DC CHARACTERISTICS,  $V_{CC} = 0V$ ,  $V_{EE} = -3.465V$  TO  $-2.375V$ ;  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1			-1.225		-0.935	V
$V_{OL}$	Output Low Voltage; NOTE 1			-1.895		-1.67	V
$V_{PP}$	Peak-to-Peak Input Voltage			0.15		1.5	mV
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 2, 3			$V_{EE} + 1.2$		0	V
$I_{IH}$	Input High Current	PCLK0:PCLK7 nPCLK0:nPCLK7				150	$\mu A$
$I_{IL}$	Input Low Current	PCLK0:PCLK7 nPCLK0:nPCLK7		-10			$\mu A$
				-150			$\mu A$

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

NOTE 3: For single-ended applications, the maximum input voltage for PCLKx, nPCLKx is  $V_{CC} + 0.3V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = 0V$ ,  $V_{EE} = -3.465V$  TO  $-2.375V$  OR  $V_{CC} = 2.375$  TO  $3.465V$ ;  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				2.8	GHz
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, 12kHz - 20MHz		0.212		ps
$t_{PD}$	Propagation Delay; NOTE 1		125		450	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				325	ps
$t_{sk(i)}$	Input Skew				75	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	75		220	ps
$MUX_{-ISOLATION}$	Mux Isolation	155.52MHz, Input Peak-to-Peak = 800mV		-55		dB

All parameters measured up to 1.3GHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined according with JEDEC Standard 65.



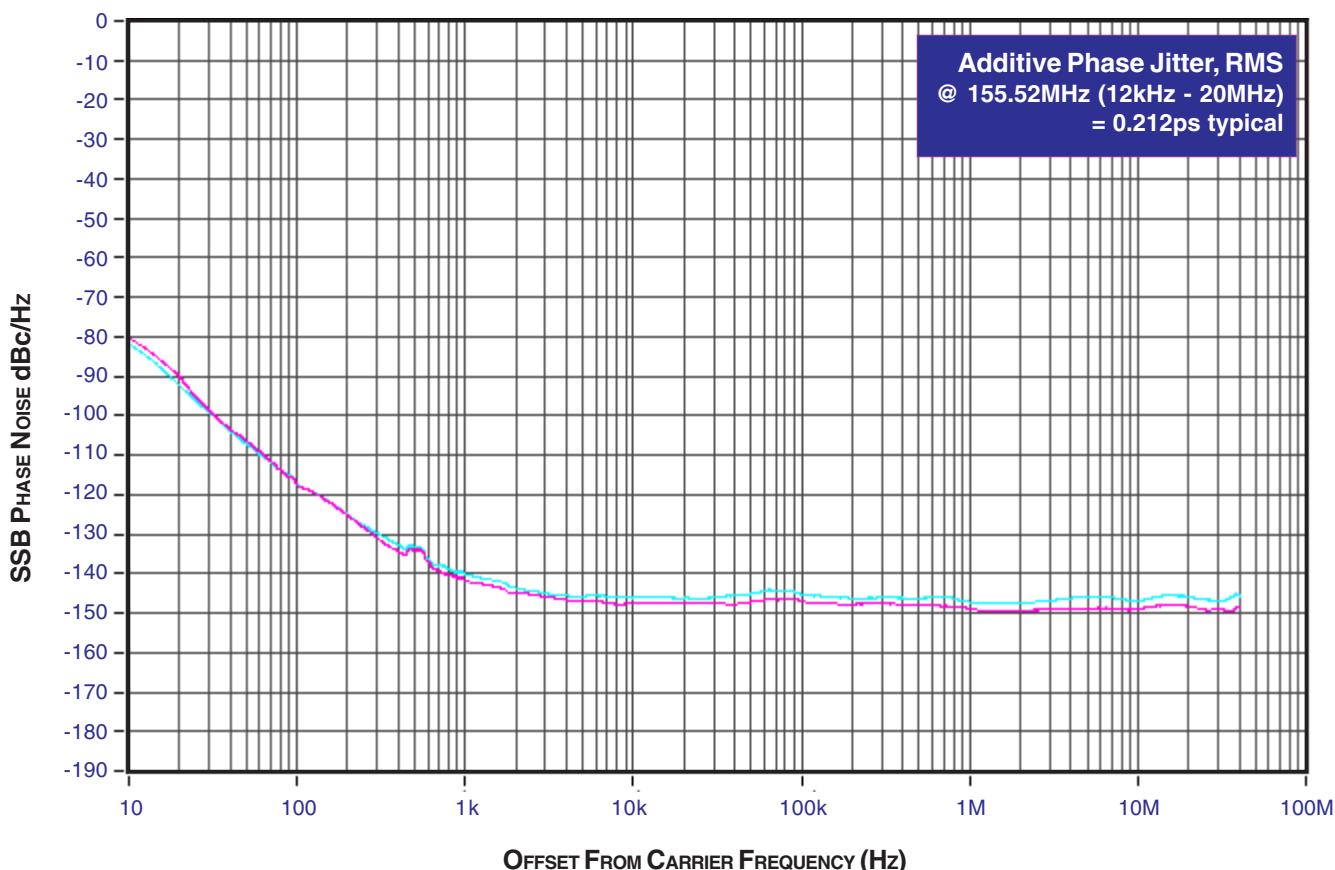
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## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated

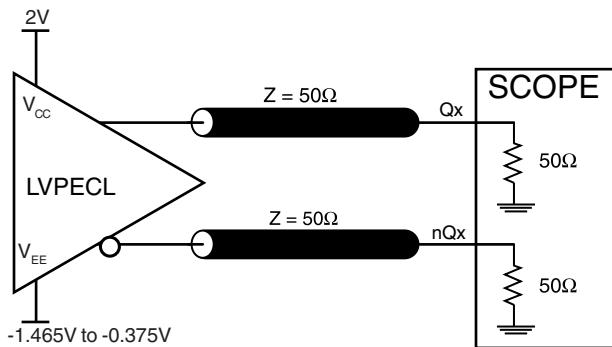
above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.



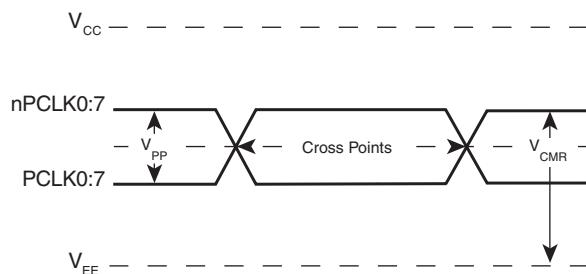
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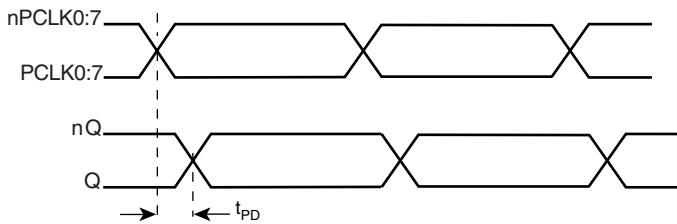
## PARAMETER MEASUREMENT INFORMATION



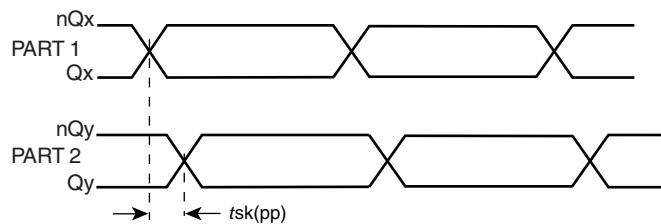
OUTPUT LOAD AC TEST CIRCUIT



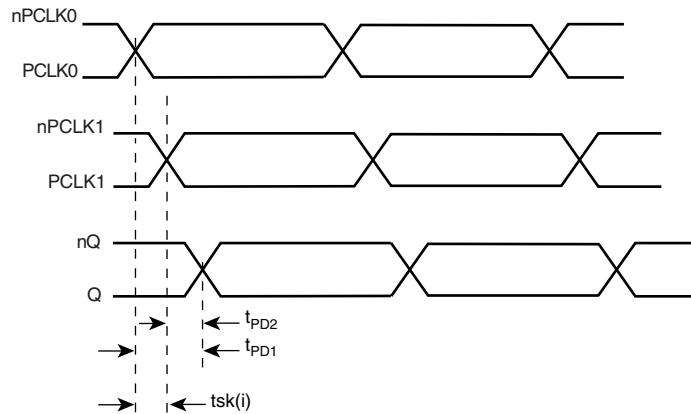
DIFFERENTIAL INPUT LEVEL



PROPAGATION DELAY

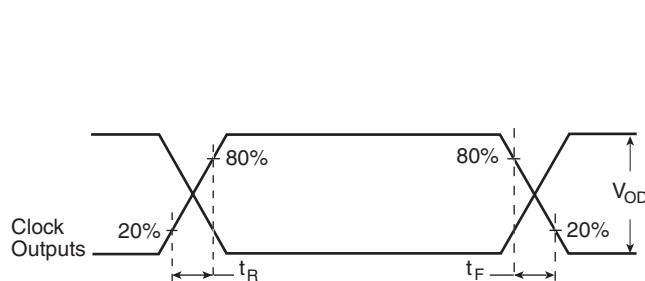


PART-TO-PART SKEW



$$tsk(i) = |t_{PD1} - t_{PD2}|$$

INPUT SKEW



OUTPUT RISE/FALL TIME



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## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

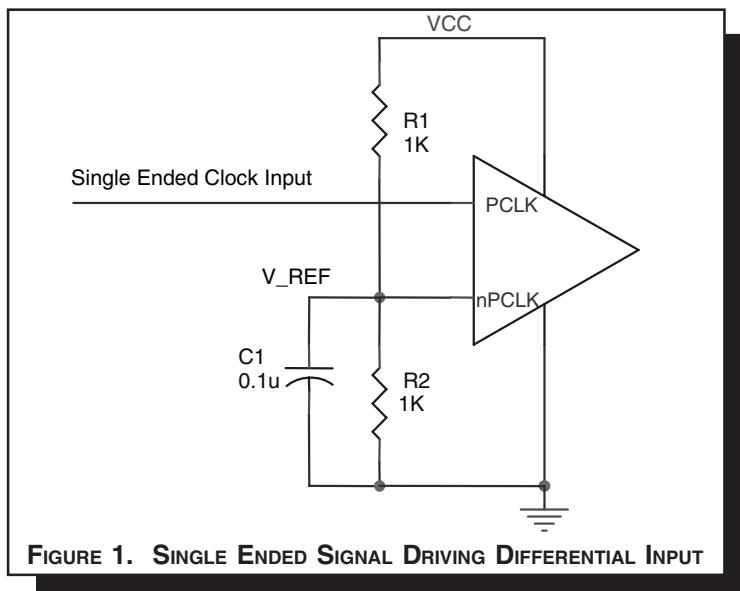


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a  $1k\Omega$  resistor can be tied from PCLK to ground.

##### LVCMS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1k\Omega$  resistor can be used.

#### OUTPUTS:

##### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



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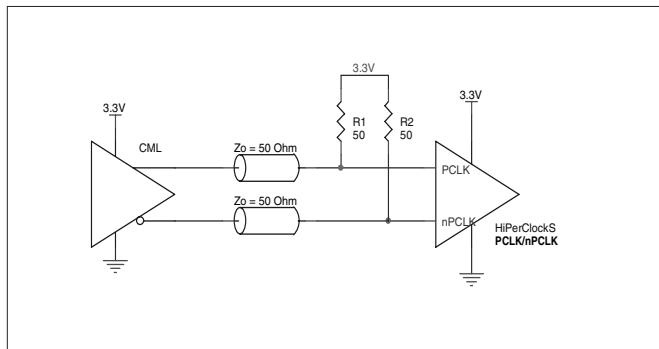
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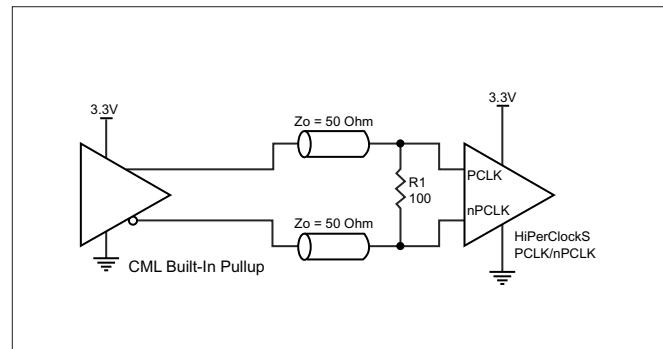
### LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input inter-

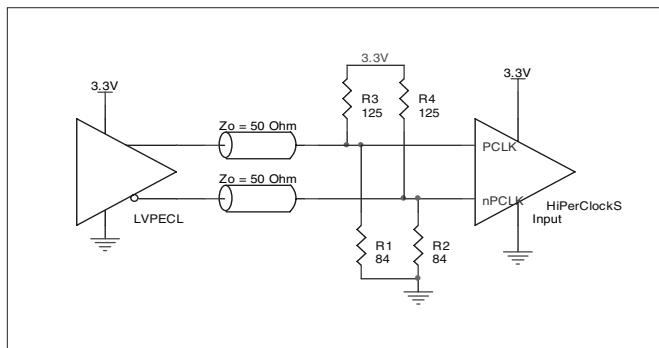
faces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



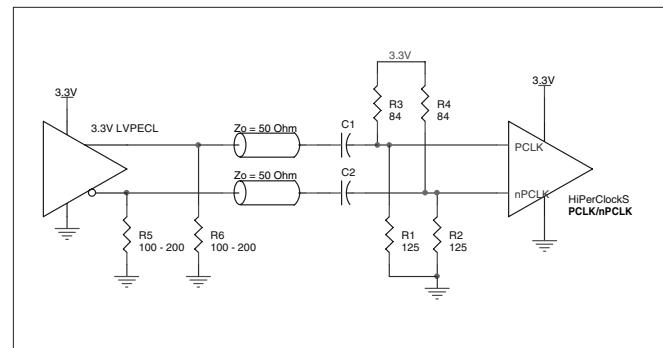
**FIGURE 2A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER**



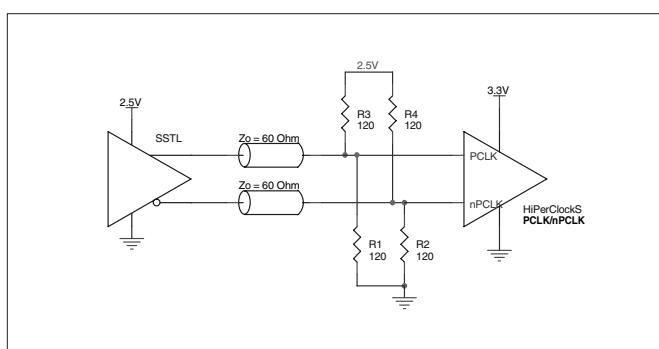
**FIGURE 2B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**



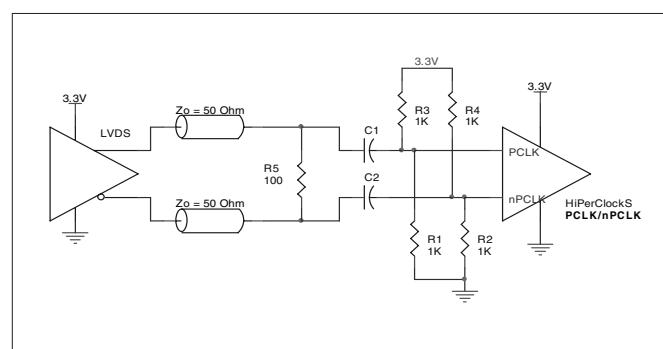
**FIGURE 2C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 2D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**



**FIGURE 2E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**



**FIGURE 2F. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**



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### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$  transmission lines. Matched imped-

ance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

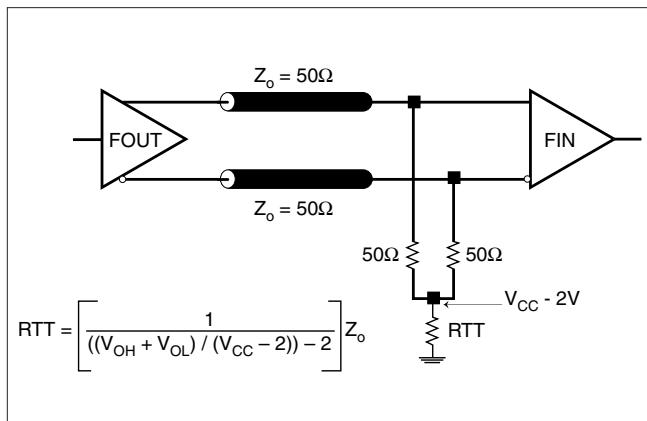


FIGURE 3A. LVPECL OUTPUT TERMINATION

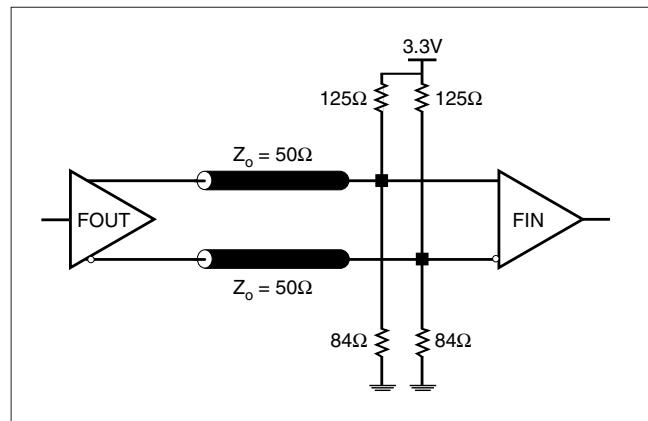


FIGURE 3B. LVPECL OUTPUT TERMINATION



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### TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very

close to ground level. The  $R_3$  in Figure 4B can be eliminated and the termination is shown in Figure 4C.

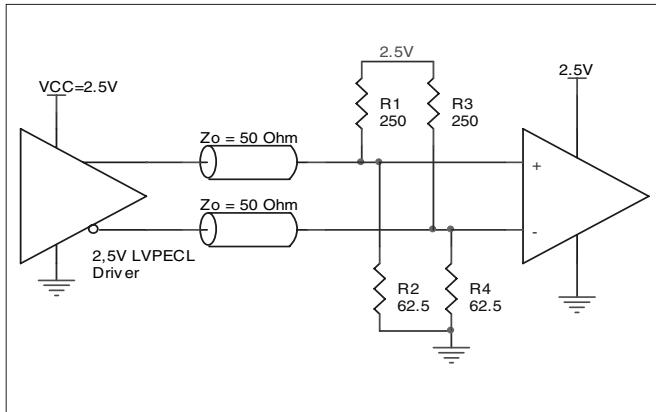


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

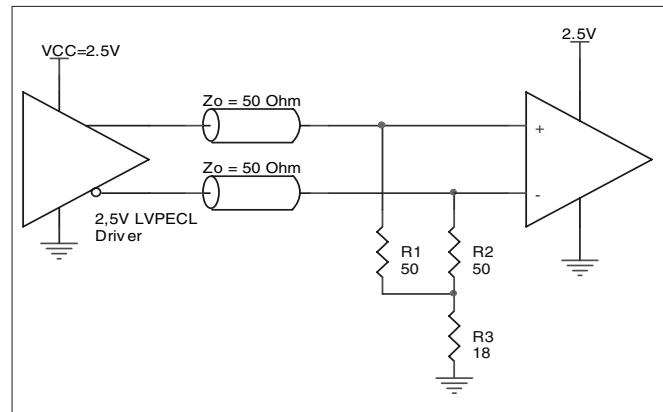


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

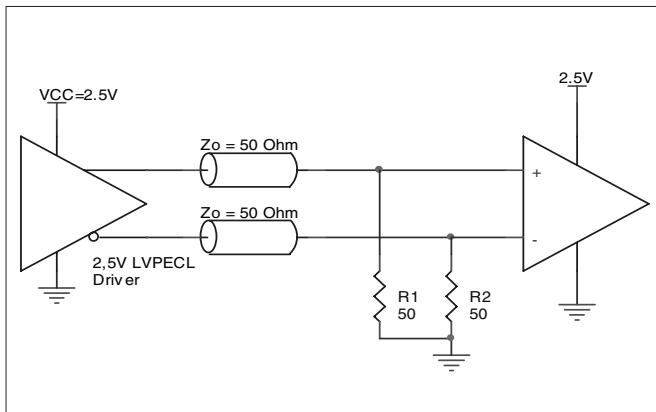


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE



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### SCHEMATIC EXAMPLE

An application schematic example of ICS853058 is shown in *Figure 5*. The inputs can accept various types of differential signals. In this example, the inputs are driven by LVPECL drivers. The ICS853058 output is an LVPECL driver. An example of LVPECL terminations is shown in this schematic.

Other termination approaches are available in the LVPECL Termination Application Note. It is recommended at least one decoupling capacitor per power pin. The decoupling capacitor should be low ESR and located as close as possible to the power pin.

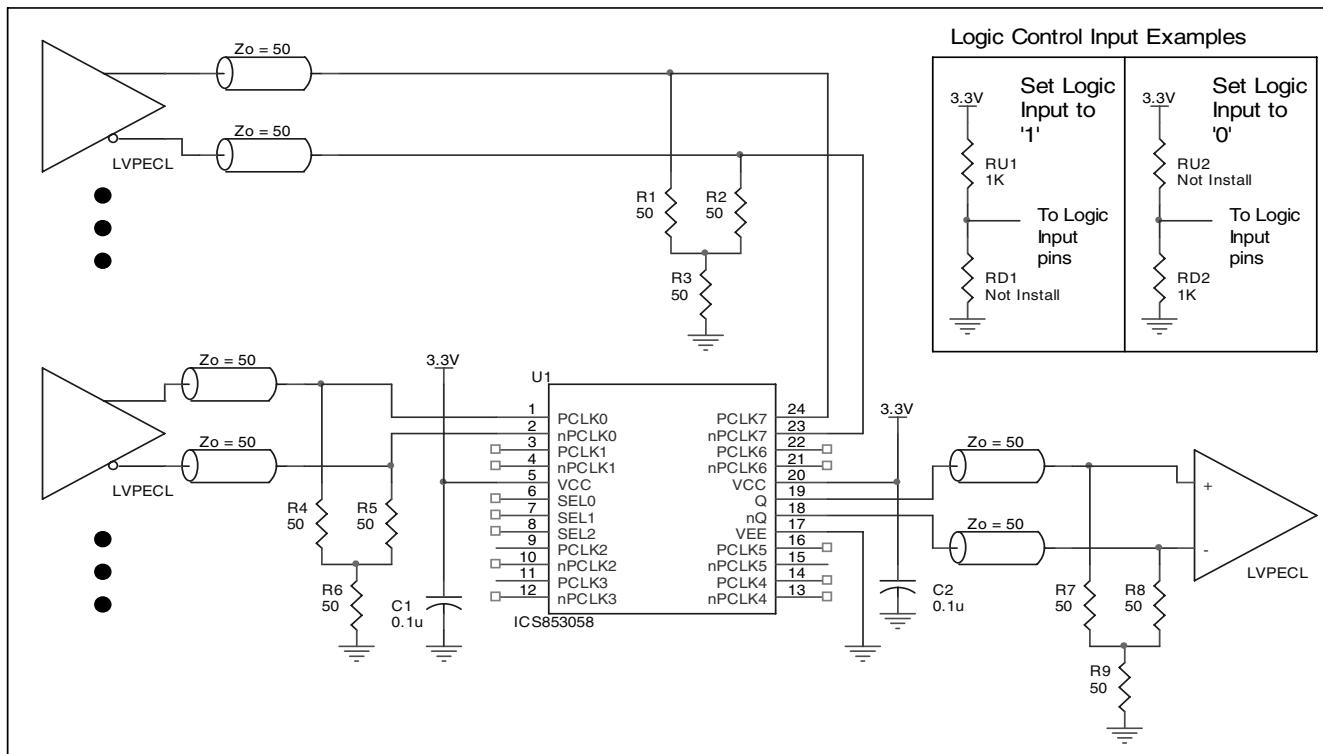


FIGURE 5. ICS853058 SCHEMATIC EXAMPLE



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853058. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS853058 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V \pm 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 47mA = 162.86mW$
- Power (outputs)<sub>MAX</sub> = **30.94mW**

$$\text{Total Power}_{MAX} (3.465V) = 162.86mW + 30.94mW = \mathbf{193.8mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.194\text{W} * 65^\circ\text{C/W} = 97.6^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C.}$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 24-PIN TSSOP FORCED CONVECTION**

<b><math>\theta_{JA}</math> by Velocity (Meters per Second)</b>			
	<b>0</b>	<b>1</b>	<b>2.5</b>
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W



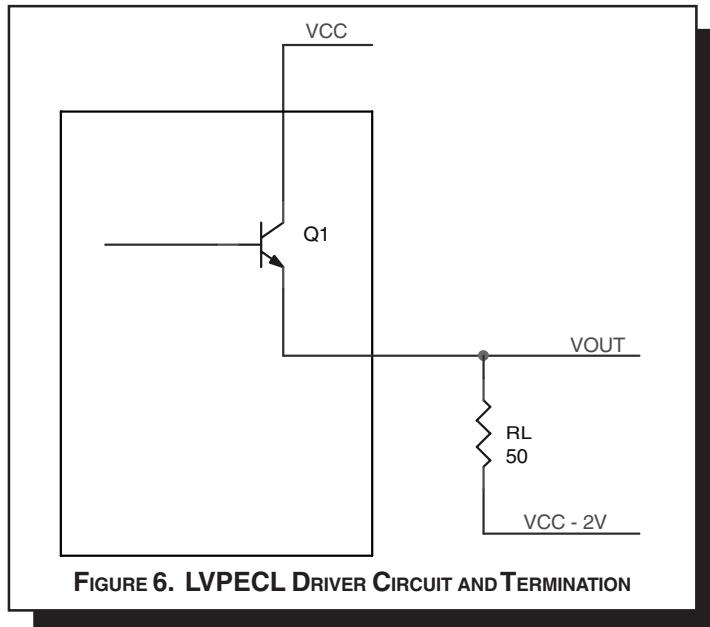
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3.3V OR 2.5V LVPECL/ECL CLOCK MULTIPLEXER

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH_{MAX}} = V_{CC_{MAX}} - 0.935V$

$$(V_{CC_{MAX}} - V_{OH_{MAX}}) = 0.935V$$

- For logic low,  $V_{OUT} = V_{OL_{MAX}} = V_{CC_{MAX}} - 1.67V$

$$(V_{CC_{MAX}} - V_{OL_{MAX}}) = 1.67V$$

$Pd_H$  is power dissipation when the output drives high.

$Pd_L$  is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_{MAX}} - (V_{CC_{MAX}} - 2V))/R_L] * (V_{CC_{MAX}} - V_{OH_{MAX}}) = [(2V - (V_{CC_{MAX}} - V_{OH_{MAX}}))/R_L] * (V_{CC_{MAX}} - V_{OH_{MAX}}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd_L = [(V_{OL_{MAX}} - (V_{CC_{MAX}} - 2V))/R_L] * (V_{CC_{MAX}} - V_{OL_{MAX}}) = [(2V - (V_{CC_{MAX}} - V_{OL_{MAX}}))/R_L] * (V_{CC_{MAX}} - V_{OL_{MAX}}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.2mW$$

Total Power Dissipation per output pair =  $Pd_H + Pd_L = 30.94mW$



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## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 24 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters per Second)			
Multi-Layer PCB, JEDEC Standard Test Boards	0 70°C/W	1 65°C/W	2.5 62°C/W

### TRANSISTOR COUNT

The transistor count for ICS853058 is: 326



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PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

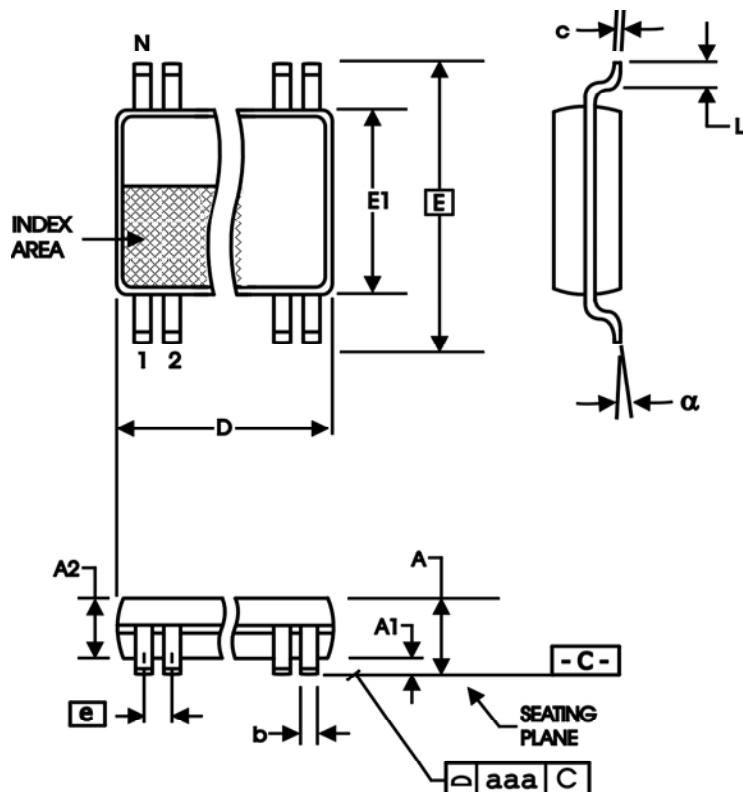


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MS-153



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**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853058AG	ICS853058AG	24 Lead TSSOP	tube	-40°C to 85°C
ICS853058AGT	ICS853058AG	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS853058AGLF	TBD	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS853058AGLFT	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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