Integrated
Circuit
Systems, Inc.

Rambus™ XDR™ Clock Generator

General Description

The **ICS9214** clock generator provides the necessary clock signals to support the Rambus XDR™ memory subsystem and Redwood logic interface. The clock source is a reference clock that may or may not be modulated for spread spectrum. The **ICS9214** provides 4 differential clock pairs in a space saving 28-pin TSSOP package and provides an off-the-shelf high-performance interface solution.

Figure 1 shows the major components of the **ICS9214** XDR Clock Generator. These include the a PLL, a Bypass Multiplexer and four differential output buffers. The outputs can be disabled by a logic low on the OE pin. An output is enabled by the combination of the OE pin being high, and 1 in its SMBus Output control register bit.

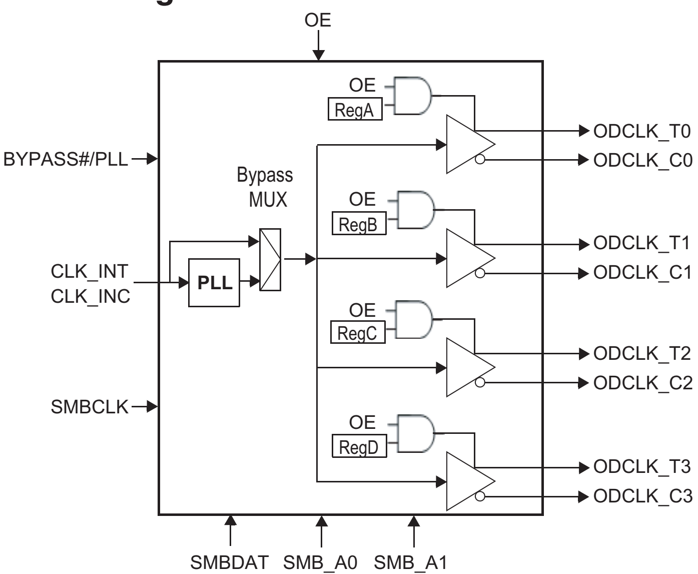
The PLL receives a reference clock, CLK_INT/C and outputs a clock signal at a frequency equal to the input frequency times a multiplier. Table 2 shows the multipliers selectable via the SMBus interface. This clock signal is then fed to the differential output buffers to drive the enabled clocks. Disabled outputs are set to Hi-Z. The Bypass mode routes the input clock, CLK_INT/C, directly to the differential output buffers, bypassing the PLL.

Up to four **ICS9214** devices can be cascaded on the same SMBus. Table 3 shows the SMBus addressing and control for the four devices.

Features

- 400 – 500 MHz clock source
- 4 open-drain differential output drives with short term jitter < 40ps
- Spread spectrum compatible
- Reference clock is differential or single-ended, 100 or 133 MHz
- SMBus programmability for:
  - frequency multiplier
  - output enable
  - operating mode
- Supports frequency multipliers of: 3, 4, 5, 6, 8, 9/2, 15/2 and 15/4
- Support systems where XDR subsystem is asynchronous to other system clocks
- 2.5V power supply

Block Diagram



Pin Configuration

AVDD2.5	1	28	VDD2.5
AGND	2	27	ODCLK_T0
IREFY	3	26	ODCLK_C0
AGND	4	25	GND
CLK_INT	5	24	ODCLK_T1
CLK_INC	6	23	ODCLK_C1
VDD2.5	7	22	VDD2.5
GND	8	21	GND
SMBCLK	9	20	ODCLK_T2
SMBDAT	10	19	ODCLK_C2
OE	11	18	GND
SMB_A0	12	17	ODCLK_T3
SMB_A1	13	16	ODCLK_C3
BYPASS#/PLL	14	15	VDD2.5

ICS9214

28-Pin 4.4mm TSSOP

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	AVDD2.5	PWR	2.5V Analog Power pin for Core PLL
2	AGND	PWR	Analog Ground pin for Core PLL
3	IREFY	OUT	This pin establishes the reference current for the differential clock pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
4	AGND	PWR	Analog Ground pin for Core PLL
5	CLK_INT	IN	"True" reference clock input.
6	CLK_INC	IN	"Complementary" reference clock input.
7	VDD2.5	PWR	Power supply, nominal 2.5V
8	GND	PWR	Ground pin.
9	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
10	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
11	OE	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
12	SMB_A0	IN	SMBus address bit 0 (LSB)
13	SMB_A1	IN	SMBus address bit 1
14	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
15	VDD2.5	PWR	Power supply, nominal 2.5V
16	ODCLK_C3	OUT	"Complementary" side of open drain differential clock output. This open drain output needs an external resistor network..
17	ODCLK_T3	OUT	"True" side of open drain differential clock output. This open drain output needs an external resistor network..
18	GND	PWR	Ground pin.
19	ODCLK_C2	OUT	"Complementary" side of open drain differential clock output. This open drain output needs an external resistor network..
20	ODCLK_T2	IN	"True" side of open drain differential clock output. This open drain output needs an external resistor network..
21	GND	IN	Ground pin.
22	VDD2.5	PWR	Power supply, nominal 2.5V
23	ODCLK_C1	OUT	"Complementary" side of open drain differential clock output. This open drain output needs an external resistor network..
24	ODCLK_T1	OUT	"True" side of open drain differential clock output. This open drain output needs an external resistor network..
25	GND	PWR	Ground pin.
26	ODCLK_C0	OUT	"Complementary" side of open drain differential clock output. This open drain output needs an external resistor network..
27	ODCLK_T0	OUT	"True" side of open drain differential clock output. This open drain output needs an external resistor network..
28	VDD2.5	PWR	Power supply, nominal 2.5V

General SMBus serial interface information for the ICS9214

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D8 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1*** (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D8 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D9 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			*ICS (Slave/Receiver)*
T	*starT bit*		
Slave Address D8$_{(H)}$			
WR	*WRite*		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		*X Byte*	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	*stoP bit*		

Index Block Read Operation

Controller (Host)			*ICS (Slave/Receiver)*
T	*starT bit*		
Slave Address D8$_{(H)}$			
WR	*WRite*		
			ACK
Beginning Byte = N			
			ACK
RT	*Repeat starT*		
Slave Address D9$_{(H)}$			
RD	*ReaD*		
			ACK
			Data Byte Count = X
ACK			
		X Byte	*Beginning Byte N*
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	*Not acknowledge*		
P	*stoP bit*		

SMB Table: Output Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD[1]
Bit 7	-	Test Mode	Reserved for Vendor	RW	Disable	Enable	0
Bit 6	-	MULT2	Multiplier Select	RW	See Table 2.		0
Bit 5	-	MULT1	Multiplier Select	RW	See Table 2.		0
Bit 4	-	MULT0	Multiplier Select	RW	See Table 2.		1
Bit 3	27,26	ODCLK_T/C0	Output Control	RW	Disable	Enable	1
Bit 2	24,23	ODCLK_T/C1	Output Control	RW	Disable	Enable	1
Bit 1	20,19	ODCLK_T/C2	Output Control	RW	Disable	Enable	1
Bit 0	17,16	ODCLK_T/C3	Output Control	RW	Disable	Enable	1

Disable = Output in high-impedance state
Enable = Output is switching

SMB Table: Frequency Multiplier Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Test Mode	Reserved for Vendor	RW	Disable	Enable	0

SMB Table: Revision & Vendor ID Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID4	Revision ID	R	-	-	X
Bit 6	-	RID3	Revision ID	R	-	-	X
Bit 5	-	RID2	Revision ID	R	-	-	X
Bit 4	-	RID1	Revision ID	R	-	-	X
Bit 3		RID0	Revision ID	R	-	-	X
Bit 2		VID2	Vendor ID	R	-	-	0
Bit 1		VID1	Vendor ID	R	-	-	0
Bit 0		VID0	Vendor ID	R	-	-	1

NOTES:
1. PWD = Power Up Default

PLL Multiplier

Table 2 shows the frequency multipliers in the PLL, selectable by programming the MULT0, MULT1 and MULT2 bits in the SMBus Multiplier Control register. Power up default is 4.

Table 2. PLL Multiplier Selection

Byte 0			Frequency Multiplier	Output Frequency (MHz)	
Bit 6	Bit 5	Bit 4		CLK_INT/C = 100 MHz[1]	CLK_INT/C = 133 MHz[1]
MULT2	MULT1	MULT0			
0	0	0	3	300[3]	400
0	0	1	4	400[2]	533
0	1	0	5	500	667
0	1	1	6	600	800
1	0	0	8	800	-[3]
1	0	1	9/2	450	600
1	1	0	15/2	750	-[3]
1	1	1	15/4	375	500

NOTES
1 Output frequencies are based on nominal input frequencies of 100 MHz and 133 MHz. The PLL multipliers are also applicable to spread spectrum modulated input clocks.
2 Default muliplier value at power up
3 Outputs at these settings do not conform to the AC Output Characteristics, or are not supported.
4 Shaded areas are under development and are not yet supported

Device ID and SMBus Device Address

The device ID (SMB_A(1:0)) is part of the SMBus device address. The least significant bit of the address designates a write or read operation. Table 3 shows the addresses for four ICS9214 devices on the same SMBus.

Table 3. SMBus Device Addresses

ICS9214		Hex Address	8-bit SMBus Device Address, Including Oper.			
Device	Operation			SMB_A1	SMB_A0	WR#/RD
0	Write	D8	11011	0	0	0
	Read	D9				1
1	Write	DA		0	1	0
	Read	DB				1
2	Write	DC		1	0	0
	Read	DD				1
3	Write	DE		1	1	0
	Read	DF				1

Operating Modes

Table 4: Operating Modes

OE	BYPASS#/ PLL	Byte 1	Byte 0				ODCLK_T/C3	ODCLK_T/C2	ODCLK_T/C1	ODCLK_T/C0
		Bit 7	Bit 3	Bit 2	Bit 1	Bit 0				
L	X	X	X	X	X	X	Z	Z	Z	Z
H	X	1	X	X	X	X	Reserved for Vendor Test			
H	L	0	X	X	X	X	CLK_INT/C[1]			
H	H	0	0	0	0	0	Z	Z	Z	Z
H	H	0	0	0	0	1	Z	Z	Z	**CLK_INT/C**
H	H	0	0	0	1	0	Z	Z	**CLK_INT/C**	Z
H	H	0	0	0	1	1	Z	Z	**CLK_INT/C**	**CLK_INT/C**
H	H	0	0	1	0	0	Z	**CLK_INT/C**	Z	Z
H	H	0	0	1	0	1	Z	**CLK_INT/C**	Z	**CLK_INT/C**
H	H	0	0	1	1	0	Z	**CLK_INT/C**	**CLK_INT/C**	Z
H	H	0	0	1	1	1	Z	**CLK_INT/C**	**CLK_INT/C**	**CLK_INT/C**
H	H	0	1	0	0	0	**CLK_INT/C**	Z	Z	Z
H	H	0	1	0	0	1	**CLK_INT/C**	Z	Z	**CLK_INT/C**
H	H	0	1	0	1	0	**CLK_INT/C**	Z	**CLK_INT/C**	Z
H	H	0	1	0	1	1	**CLK_INT/C**	Z	**CLK_INT/C**	**CLK_INT/C**
H	H	0	1	1	0	0	**CLK_INT/C**	**CLK_INT/C**	Z	Z
H	H	0	1	1	0	1	**CLK_INT/C**	**CLK_INT/C**	Z	**CLK_INT/C**
H	H	0	1	1	1	0	**CLK_INT/C**	**CLK_INT/C**	**CLK_INT/C**	Z
H	H	0[2]	1[2]	1[2]	1[2]	1[2]	**CLK_INT/C**	**CLK_INT/C**	**CLK_INT/C**	**CLK_INT/C**

Notes

1 Bypass Mode

2 Power up default mode

Absolute Maximum Ratings

Supply Voltage . . . . 4.0 V
Logic Inputs . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . 0°C to +70°C
Storage Temperature . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics - Inputs

TA = 0°C to +70°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 0.125V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD2.5}$, A_{VDD}		2.375		2.625	V
Supply Current	$I_{DD2.5}$, I_{VDD}				125	mA
High-level input voltage	V_{IHCLK}	CLK_INT, CLK_INC	0.6		0.95	V
Low-level input voltage	V_{ILCLK}		-0.15		0.15	V
Crossing point voltage	V_{IXCLK}		0.2		0.55	V
Difference in crossing point voltage	V_{IXCLK}				0.15	V
Input threshold voltage	V_{TH}	Singled-ended CLK_IN[1]	0.35		$0.5_{VDD2.5}$	V
High-level input voltage for single-ended CLK_IN	V_{IHSE}		V_{TH} + 0.3		2.625	V
Low-level input voltage for single-ended CLK_IN	V_{ILSE}		-0.15		V_{TH} - 0.3	V
High-level input voltage	V_{IH}	OE, SMB_A0, SMB_A1, BYPASS#/PLL	1.4		2.625	V
Low-level input voltage	V_{IL}		-0.15		0.8	V
High-level input voltage - SMBus	V_{IHSMB}	SMBCLK, SMBDAT	1.4		3.4652	V
Low-level input voltage - SMBus	V_{ILSMB}		-0.15		0.8	V

Notes:

1 When using singled-ended clock input, VTH is supplied to CLK_INTC as shown in Figure 2. Duty cycle of singled-ended CLK_IN is measured at V_{TH}

2 This range of SMBus input high voltages allows the 9214 to co-exist with 3.3V, 2.5V and 1.8V devices on the same SMBus.

DC Characteristics - Outputs

TA = 0°C to +70°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 0.125V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power up latency	t_{PU}	Power within spec to outputs within spec			3	ms
State transition latency[1]	t_{CO}	SMBus or Mode Select transition to outputs valid and within spec			3	ms
Differential output crossing voltage	V_{OX}	Measured as shown in Fig. 3	0.9		1.1	V
Output Voltage Swing (peak-to-peak singled ended)	V_{COS}	Measured as shown in Fig. 3. Excludes over and undershoot.	300		350	mV
Absolute output low voltage	VOLABS	Measured at ODCLK_T/C pins	0.85			V
Reference Voltage for swing control current	V_{ISET}	V_{DD} = 2.3V, V_{OUT} = 1V	0.98		1.02	V
Ratio of output low current to reference current at typical $V_{DD2.5}$	I_{OL}/I_{REF}	I_{REF} is equal to V_{ISET}/R_{RC}. Tolerance of R_{RC} <=+/-1%.	6.8	7	7.2	-
Minimum current at V_{OLABS}	I_{OLABS}	Measured at ODCLK_T/C pins with termination per Figure 3.	45		-	mA
Low-level output voltage SMBus	V_{OLSMB}	I_{OL} = 4 mA	-		0.4	V
Low-level output current SMBus	I_{OLSMB}	V_{OL}= 0.8 V	6		-	mA
Tristate output current	I_{OZ}	Differential clock output pins	-		50	µA

Notes:

There is no output latency or glitches if a value is written to an output register.
that is the same as its current contents.

AC Characteristics-Inputs

T_A = 0°C to +70°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 0.125V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
CLK_INT/CLK_INC cycle time[1]	$t_{CYCLEIN}$		7		11	ns
Cycle-to-Cycle Jitter	t_{cyc}-t_{cyc} [2]				185	ps
Input clock duty cycle	d_{tin}	over 10,000 cycles	40		60	%
CLK_INT/CLK_INC rise and fall time	t_R, t_F	20% to 80% of input voltage	175		700	ps
Difference between input rise and fall time on same pin of a single device	t_{R-F}	20% to 80% of input voltage	-		150	ps
Spread spectrum modulation frequency	f_{INM} [3]		30		33	kHz
Spread spectrum modulation index	m_{INDEX} [3]	Triangular modulation			0.6	%
		Non-triangular modulation			0.54	%
Input clock slew rate	$t_{sl(I)}$	20% to 80% of input voltage	1		4	V/ns
Input Capacitance[5]	C_{INCLK}	CLK_INT, CLK_INC			7	pF
Input Capacitance[5]	C_{IN}	VI = $V_{DD2.5}$ or GND			10	pF
CLK_INT cycle time	$t_{CYCLETST}$	Bypass Mode	4		40	ns
SMBus clock frequency	f_{SMB}		10		100	kHz

Notes:

1. Measured at (VIH(nom) - VIL(nom))/2 and is the absolute value of the worst case deviation.
2. Measured at crossing points for differential clock input or at VTH for single-ended clock input
3. If input modulation is used. Input modulation is not necessary.
4. The amount of allowed spreading for non-triangular modulation is determined by the induced downstream tracking skew.
5. Capacitance measured at f = 1 MHz, DC bias = 0.9V, VAC <100mV.

AC Characteristics-Outputs

T_A = 0°C to +70°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 0.125V (unless otherwise stated)

PARAMETER[1]	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output clock cycle time	t_{CYCLE}		1.5		2.5	ns
Short term jitter (over 1 to 6 clock cycles)	t_J[2]	f = 400 to 635 MHz	-		40	ps
		f = 635 to 800 MHz	-		30	ps
Output Phase error when tracking SSC	$t_{ERR,SSC}$		-100		100	ps
Change in skew	t_{SKEW}[3]	T_A = 0°C to +70°C, AVDD2.5, VDD2.5 = 2.5 V +/- 0.125V	-		15	ps
Long term average output duty cycle	DC		45		55	%
Cycle-to-cycle duty cycle error	t_{DCERR}	f = 400 to 635 MHz	-		40	ps
		f = 635 to 800 MHz	-		30	ps
Output rise and fall times	t_R, t_F	20% to 80% of output voltage	100		300	ps
Difference between output rise and fall time on same pin of a single device	t_{R-F}	20% to 80% of output voltage, f = 400 to 800 MHz	-		100	ps
Dynamic output impedance	Z_{OUT}[4]	V_{OL} = 0.9 V	1000		-	Ω

Notes:

1. Max and min output clock cycle times are based on nominal output frequencies of 400 and 667 MHz respectively. For spread spectrum modulated input clocks, the output clocks track the input modulation.
2. Output short-term jitter is the absolute value fo the worst case deviation and is defined in the Jitter section.
3. tSKEW is the timing difference between any two of the four differential clocks and is measured at common mode voltage.
4. Zout is defined at the output pins.
5. Guaranteed by design and characterization, not 100% tested in production

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		95		°C/W
	θ_{JA}	3 m/s air flow		80		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still Air		4.5		°C/W
Maximum Case Temp					120	°C

Clock Output Drivers

Figure 2 shows the clock driver equivalent circuit. The differential driver produces a specified voltage swing on the channel by switching the currents going into ODCLK_T and ODCLK_C. The external resistor R_{RC} at the IREFY pin sets the maximum current. The minimum current is zero.

The voltage at the IREFY pin, V_{IREFY}, is by design equal to 1 V nominally, and the driver current is seven times the current flowing through R_{RC}. So, the output low current can be estimated as $I_{OL} = 7/ R_{RC}$.

The driver output characteristics are defined together with the external resistors, R_1, R_2, and R_3. The output clock signals are specified at the measurement points indicated in Figure 2. Table 5 shows example values for the resistors.

R_1, R_2, and R_3 and the clock driver output impedance, Z_{OUT}, must match the impedance of the channel, Z_{CH} , to minimize secondary reflections. Z_{OUT} is specified as 1000 Ohms, minimum to accomplish this. The effective impedance can be estimated by:

$$(1000R_1/(1000+R_1)+R2) \quad R_3/(1000R_1/(1000+R_1)+R_2+R_3)$$

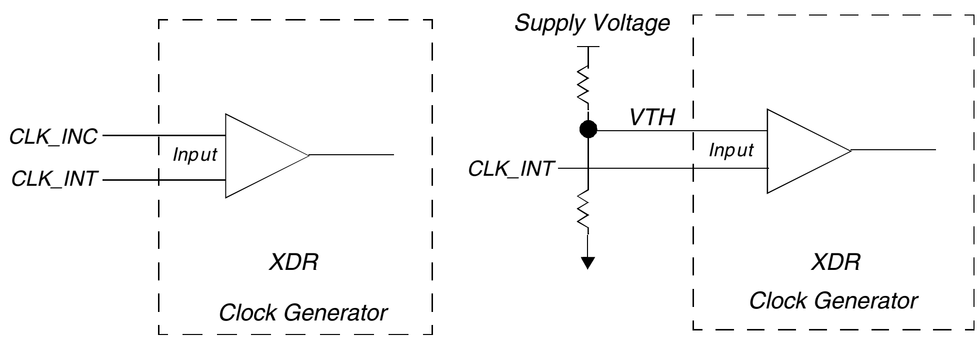
Pull-up resistor R_T terminates the transmission line at the load to minimize clock signal reflection signal reflections. Table 5 shows the resistor values for establishing and effective source termination impedance of 49.2 Ohms to match a 50 Ohm channel. The termination voltages are 2.5 V for V_{TS} and 1.2 V for V_T. The resistor values R1 = 38.3 Ohms, R_2 = 19.1 Ohms, R_3 = 54.9 Ohms and R_{RC} = 200 Ohms can be used to match a 28 Ohm channel.

Table 5. Example Resistor Values and Termination Voltages for a 50 Ohm Channel[1]

Symbol	Parameter	Value	Tolerance	Unit
R_1	Termination resistor	39.2	+/- 1%	Ω
R_2	Termination resistor	66.5	+/- 1%	Ω
R_3	Termination resistor	93.1	+/- 1%	Ω
R_T	Termination resistor	49.9	+/- 1%	Ω
R_{RC}	Swing control resistor	200	+/- 1%	Ω
V_{TS}	Source termination voltage	2.5	+/-5%	V
V_T	Termination voltage	1.2	+/-5%	V

Notes:

1 A different set of resistors is used in Figure 2 when testing for maximum output current of the clock driver (I_{OLABS}). These resistors are: $R_1 = 34Ω$, $R_2 = 31.8Ω$, $R_3 = 48.7Ω$, $R_T=28Ω$, $R_{RC} = 147Ω$



a. Differential input *b. Single-ended input*

Figure 1. Differential and single-ended reference clock inputs

Input Clock Signal

The **ICS9214** receives either a differential or single-ended reference clock (CLK_INT/C). When the reference input clock is from a differential clock source, it must meet the voltage levels and timing requirements listed in the **DC Characteristics – Inputs** and **AC Characteristics – Inputs** tables.

For a singled-ended clock input, an external voltage divider and a supply voltage, as shown in Figure 2, provide a reference voltage V_{TH} at the CLK_INC pin to determine the proper switching point for CLK_INT. The range of V_{TH} is specified in the **DC Characteristics – Inputs** table.

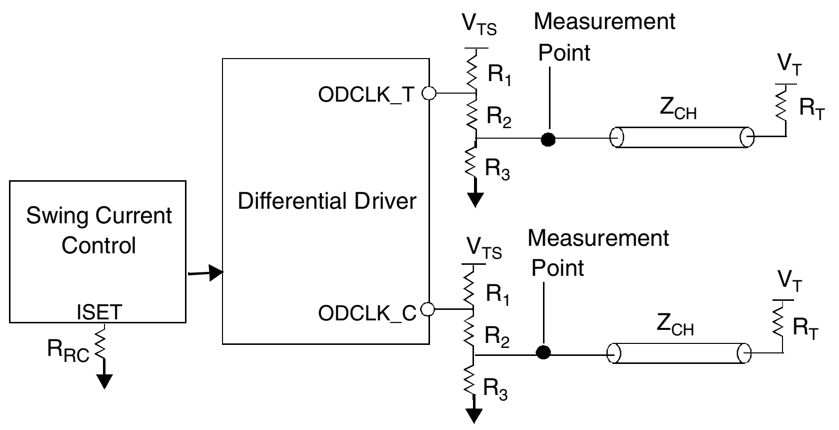


Figure 2. Example System Clock Driver Equivalent Circuit

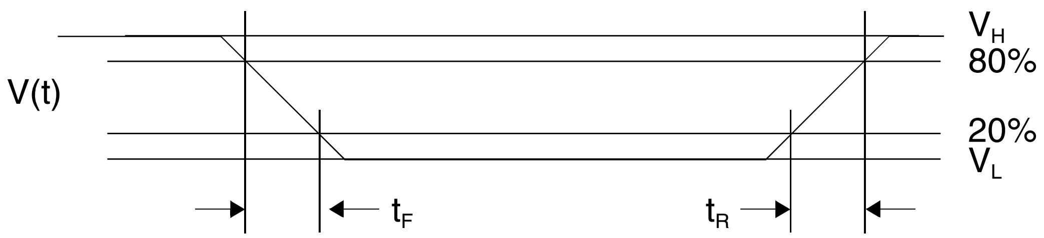


Figure 3. Input and Output Voltage Waveforms

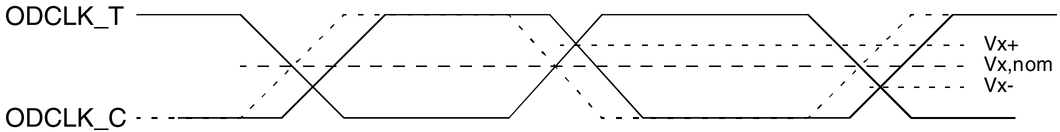
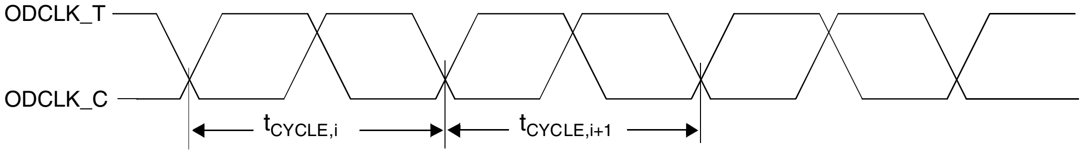


Figure 4. Crossing-point Voltage

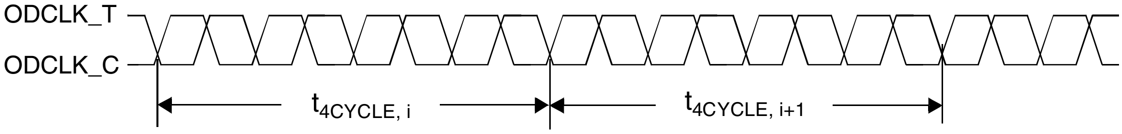
Power Sequencing

Supply voltages for the **ICS9214** must be applied before, or at the same time and external input and output signals.



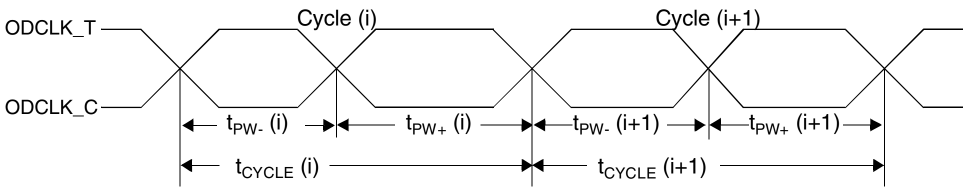
$t_J = t_{CYCLE,} - t_{CYCLE,\ i+1}$ over 10,000 consecutive cycles

Figure 5. Cycle-to-cycle Jitter



$t_J = t_{4CYCLE,\ i} - t_{4CYCLE\ \ i+1}$ over 10,000 consecutive cycles

Figure 6. Short-term Jitter



$t_{DC,ERR} = t_{PW+}(i) - t_{PW+}(i+1)$ and $t_{PW-}(i) - t_{PW-}(i+1)$

Figure 7. Cycle-to-cycle Duty Cycle Error

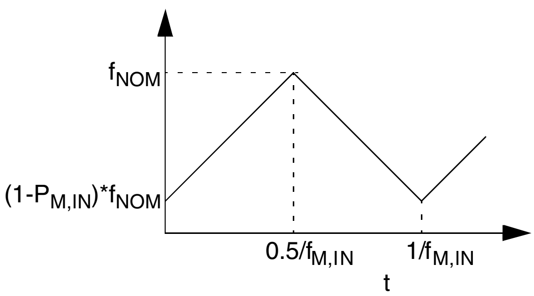


Figure 8. Input frequency Modulation

Phase Noise

The 9214 meets the single side band phase noise spectral purity for offset frequencies between 1 MHz and 100 MHz as described by the equation:

10log[1+(50 x 106/f)2.4] -138 dBc/Hz

This equation is shown in **Figure 9. Phase Noise Plot**

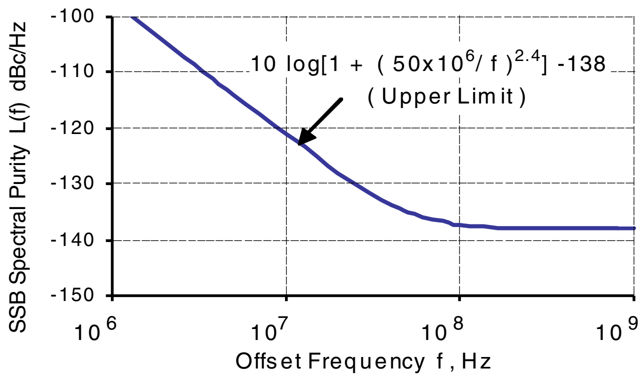
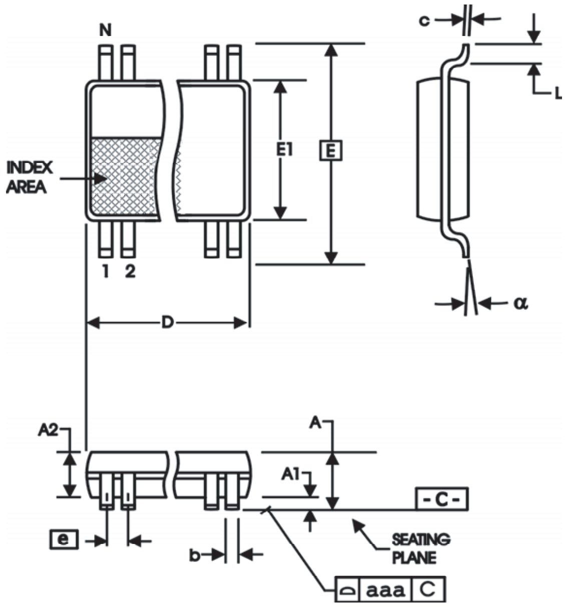


Figure 9 : Phase Noise Plot

Sample points are for this equation are shown in **Table 6. Phase Noise Data Points**

Offset Frequency (MHz)	1	5	10	15	20	40	80	100
SSB Spectral Purity (dbc/Hz)	-97	-114	-121	-125.2	-128	-133.7	-136.8	-137.3

Table 6 : Phase Noise Data Points



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

ICS9214yG LF-T

Example:

ICS XXXX y G LF- T

- **T** — **Designation for tape and reel packaging**
- **LF** — **Annealed Lead Free (Optional)**
- **G** — **Package Type**
  G = TSSOP
- **y** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type**
- **ICS** — **Prefix**
  ICS = Standard Device

Revision History

Rev.	Issue Date	Description	Page #
0.1	3/30/2005	Updated SMBus table Byte 2, Bit 3 from:0 to:1. Updated PLL Multiplier Selection Table, from: Byte 1 to: Byte 0, and Bit 2,1,0, to: Bit 6,5,4. Updated Ordering Information from "Lead Free" to "Annealed Lead Free"	4-5,15
A	4/6/2005	Added Phase noise spec Removed unsupported speeds from PLL Multiplier Selection, Changed minimum output raise, fall times from 140ps to 100 ps Compliant with Rev 0.81 of XCG spec.	Various
B	4/22/2005	1. Changed write address from D2 to a valid address (D8) 2. Changed read address from D3 to a valid address (D9)	3
C	11/11/2005	Added the 15/4 entry in the gear table to the list of supported frequencies	5
D	4/7/2006	Added Thermal Characteristics Table.	10