Integrated Circuit Systems, Inc.

Direct Rambus™ Clock Generator Lite

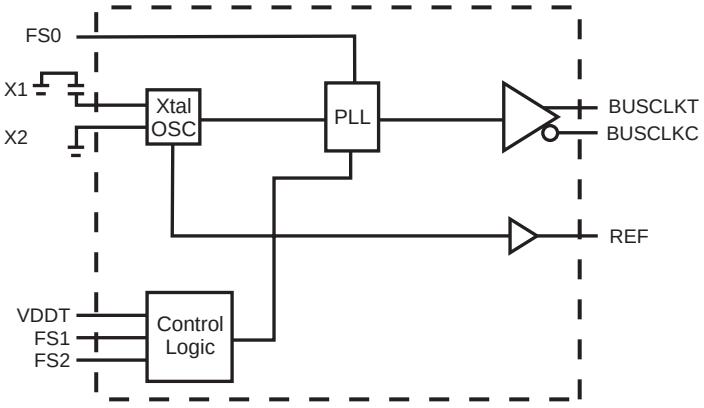
General Description

ICS9219 is a High-speed clock generator providing 400 or 533 MHz differential clock source for direct Rambus™ memory system. **ICS9219** takes a crystal as an input reference source, and produces the differential output clock required for the Rambus channel. **ICS9219** provides a solution for a broad range of Direct Rambus memory applications. **ICS9219** can be used in single or dual Rambus channels. An additional LVCMOS output, which provides a reference clock at the crystal frequency for the other system blocks is also included.

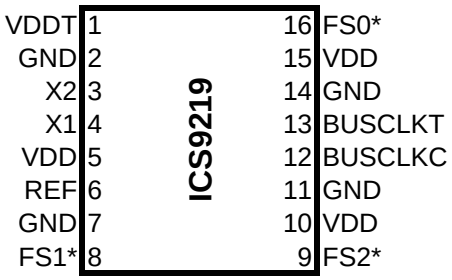
Features

- Compatible with all Direct Rambus™ based ICs
- Provides differential clock source for direct Rambus memory system with 1GHz data transfer rate capability
- Cycle to Cycle jitter is less than 100ps
- 3.3V ± 4% supply
- LVCMOS REF clock @ crystal frequency
- Output edge rate control to minimize EMI

Block Diagram



Pin Configuration



16-Pin 173 mil TSSOP

* Pins have 60K internal pull-up to VDD

Table 1. PLL Multiplier Selection and Output Frequency

FS0	Mult	BUSCLK[1]
0	16	400.00
1	21.33[2]	533.30

Notes:

1 Output frequencies are based on 25MHz XTAL Input multipliers are also applicable to spread spectrum modulated input clocks.

2 Default muliplier value at power up.

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDT	PWR/IN	Power supply, nominal 3.3V/Test mode
2	GND	PWR	Ground pin.
3	X2	OUT	Crystal output (14MHz to 25MHz)
4	X1	IN	Crystal input (14MHz to 25MHz)
5	VDD	PWR	Power supply, nominal 3.3V
6	REF	OUT	Reference of Input
7	GND	PWR	Ground pin.
8	FS1*	IN	Frequency select pin.
9	FS2*	IN	Real-time frequency select pin with internal 120Kohm pull-up resistor (check SMBus HW/SW setting for priority).
10	VDD	PWR	Power supply, nominal 3.3V
11	GND	PWR	Ground pin.
12	BUSCLKC	OUT	Output clock connected to the Rambus channel. This output is the complement of BUSCLK.
13	BUSCLKT	OUT	Output clock connected to the Rambus channel. This output is the true component of BUSCLK.
14	GND	PWR	Ground pin.
15	VDD	PWR	Power supply, nominal 3.3V
16	FS0*	IN	Frequency select pin.

* Pins have 60K internal pull-up to VDD

Table 2: Function Table

VDDT	FS(2:0)			INPUT MULT	MODE	BUSCLKT	BUSCLKC	REF
	FS2	FS1	FS0					
3.3V	0	0	0	16	NORMAL	INPUT x MULT	BUSCLKC	INPUT
3.3V	1	1	1	21.33	NORMAL	INPUT x MULT	BUSCLKC	INPUT
3.3V	1	1	0	16	NORMAL	INPUT x MULT	BUSCLKC	INPUT
3.3V	0	0	1	21.33	NORMAL	INPUT x MULT	BUSCLKC	INPUT
3.3V	1	0	X	-	TEST	BUSCLKT/2	BUSCLKC/2	INPUT
3.3V	0	1	X	-	TEST	BUSCLKT/4	BUSCLKC/4	INPUT
0	0	0	X	-	TEST	X1	X1(INVERT)	INPUT
0	1	1	X	-	TEST	X1	X1(INVERT)	INPUT
0	1	0	X	-	TEST	X1/2	X1(INVERT)/2	INPUT
0	0	1	X	-	TEST	X1/4	X1(INVERT)/4	INPUT

Absolute Maximum Ratings over operating free-air temperature

Supply voltage range, V_{DD} or V_{DDT} (see Note 1) . . . . . -0.5 V to 4 V
Input voltage range,V_I, at any input terminal . . . . . -0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O, at any output terminal (BUSCLKT/C). . . . . -0.5 V to V_{DD} + 0.5 V
ESD rating (MIL-STD 883C, Method 3015) . . . . . > 2 kV, Machine Model >200 V
Operating free-air temperature range, T_A . . . . . 0˚C to 85˚C
Storage temperature range, T_{stg} . . . . . -65˚C to 150˚C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to the GND terminals.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3	3.3	3.6	V
Low-level input voltage, V_{IL}	FS (2:0)			0.35 x V_{DD}	V
High-level input voltage, V_{IH}	FS (2:0)	0.65 x V_{DD}			
Internal pullup resistance	FS (2:0)	90		150	kΩ
Input frequency at crystal input		14.0625	25	26	MHz
Low-level output current, I_{OL}		BUSCLKT/C		16	mA
		REF		10	
High-level output current, I_{OH}		BUSCLKT/C		-16	mA
		REF		-10	
Input capacitance (CMOS), C_L	FS (2:0)			15	pF
	X1, X2			15	
Operating free-air temperature		0		85	C

Timing Requirements

	MIN	MAX	UNIT
Clock cycle time, $t_{(CYCLE)}$	2.5	3.7	ns
Input slew rate, S_R	0.5	4	V/ns
State transition latency (V_{DDX} or S0 to CLKs - normal mode), $t_{(STL)}$		3	ms

Crystal Specifications

	MIN	MAX	UNIT
Frequency	14.0625	26	MHz
Frequency tolerance (at 25°C) ± 3°C)	-15	15	ppm
Equivalent resistance (C_L = 10 pF)		100	Ω
Temperature drift (-10°C to 75°C)		10	ppm
Drive level	0.01	1500	μΩ
Motional inductance	20.7	25.3	mH
Insulation resistance	500		MΩ
Spurious attenuation ratio (at frequency ±500 kHz)	3		dB
Overtone spurious	8		dB

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Electrical Characteristics over Recommended Operating Free-Air Temperature

PARAMETER			TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_X	Differential crossing-point output voltage		See Figures 1 and 2		1.25	1.6	1.85	V
V_{COS}	Peak-to-peak output voltage swing, single ended		V_{OH} - V_{OL}	See Figure 1	0.4	0.6	0.7	V
V_{IK}	Input clamp voltage		V_{DD} = 3V	I_I = -18 mA			-1.2	V
R_I	Input resistance	X1, X2	V_{DD} = 3.3V	V_I = V_O		>50		k
I_{IH}	High-level input current	X2	V_{DD} = 3.3V	V_O = 2V			27	mA
		FS0	V_{DD} = 3.6V	V_I = V_{DD}			10	mA
		FS1, FS2	V_{DD} = 3.6V	V_I = V_{DD}			10	
I_{IL}	Low-level input current	X2	V_{DD} = 3.6V	V_O = 0V			-5.7	mA
		FS0	V_{DD} = 3.6V	V_I = 0V	-30		-100	mA
		FS1, FS2	V_{DD} = 3.6V	V_I = 0V	-10		-50	
V_{OH}	High-level output voltage	BUSCLKT/C, REF	See Figure 1				2.1	V
			V_{DD} = min to max	I_{OH} = -1 mA	V_{DD} - 0.1V			
			V_{DD} = 3V	I_{OH} = -16 mA	2.2	2.5		
V_{OL}	Low-level output voltage	BUSCLKT/C, REF	See Figure 1		1			V
			V_{DD} = min to max	I_{OH} = 1 mA		0.05	0.1	
			V_{DD} = 3V	I_{OH} = 16 mA		0.25	0.5	
I_{OH}	High-level output current	BUSCLKT/C, REF	V_{DD} = 3.135V	V_O = 1V		-50	-32	mA
			V_{DD} = 3.3V	V_O = 1.65V		-50		
			V_{DD} = 3.465V	V_O = 3.135V	-21	-15		
I_{OL}	Low-level output current	BUSCLKT/C, REF	V_{DD} = 3.135V	V_O = 1.95V	43	69		mA
			V_{DD} = 3.3V	V_O = 1.65V		69		
			V_{DD} = 3.465V	V_O = 0.9V		30	36	
r_{OH}	High-level dynamic output resistance[4]		$\angle I_O$ - 14.5 mA to $\angle I_O$ - 16.5 mA		12	25	40	
r_{OL}	Low-level dynamic output resistance[4]		$\angle I_O$ - 14.5 mA to $\angle I_O$ - 16.5 mA		12	17	40	
C_O	Output capacitance	BUSCLKT, BUSCLKC, REF					3	pF
I_{DD}	Static supply current		Outputs high or low (V_{DDT} = 0V)				6.5	mA
I_{DDL}	Static supply current		Outputs high or low (V_{DDT} = 0V)				50	mA
$I_{DD\ (NORMAL)}$	Supply current in normal state		400 MHz			84	100	mA
			533MHz			91	120	mA

* V_{DD} refers to any of the following: V_{DD}, V_{DDT}.

** All typical values are at V_{DD} = 3.3V, T_A 25°C.

[4] $r_O = \angle V_O / \angle I_O$. This is defined at the output terminals, not at the measurement point of figure 1.

Switching Characteristics over Recommended Operating Free-Air Temperature Range.

PARAMETER			TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$t_{(CYCLE)}$	Clock cycle time (BUSCLKT/C)			1.8		3.7	ns
t_J	Total jitter over 1, 2, 3, 4, 5 or 6 clock cycles	400 MHz	See Figure 3		42	50	ps
		533 MHz			33	50	
t_{JL}	Long-term jitter	400 MHz	See Figure 4			300	ps
		533 MHz				300	
D_C	Output duty cycle over 10,000 cycles		See Figure 5	43%	51	53%	
$t_{DC,ERR}$	Output cycle-to-cycle duty cycle error	400 MHz	See Figure 6		30	50	ps
		533 MHz			30	50	
t_{CR}, t_{DF}	Output rise and fall times (measured at 20%-80% of output voltage)	BUSCLKT/C	See Figure 7	120	250	400	ps
Δt_{RF}	Difference between rise and fall times on a single device (20% ± 80%) |tCR - tCF|		See Figure 7		50	100	ps
$t_{CYCLE(L)}$	Clock cycle time (REF)		See Figure 8 Measured at 50%	80		142.2	ns
$t_{(CJ)}$	REF cycle jitter			-0.2	0.1	0.2	ns
$t_{(CJ10)}$	REF 10-cycle jitter			-1.3 $t_{(CJ)}$		1.3 $t_{(CJ)}$	ns
$D_{C(2)}$	Output duty cycle	REF		47%	50	53%	
t_{CRL}, t_{CFL}	Output rise and fall times (measured at 20%-80% of output voltage)	REF	See Figure 7		0.8	1	ns
PLL loop bandwidth			fmod = 50 kHz			-3	dB
			fmod = 8 MHz	-20			

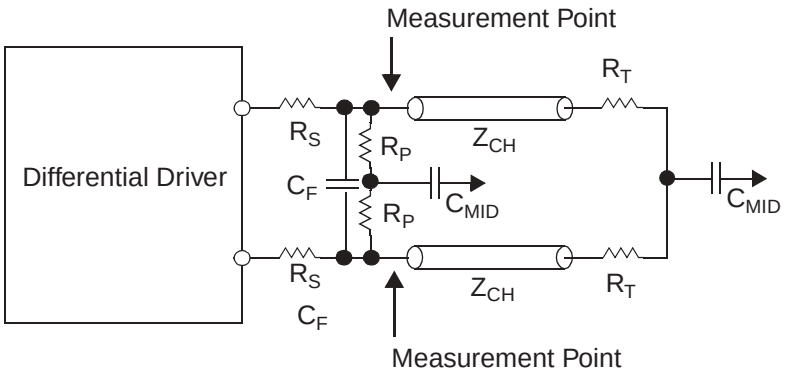


Figure 1. Example System Clock Driver Equivalent Circuit

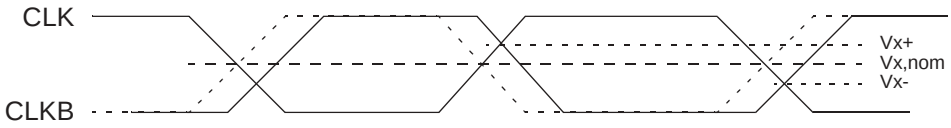
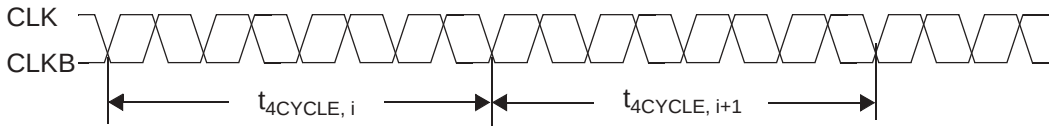
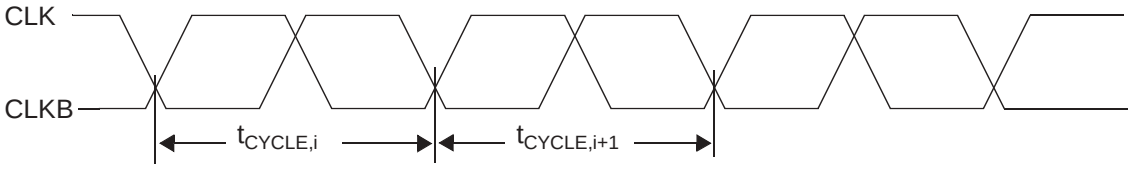


Figure 2. Crossing-point Voltage



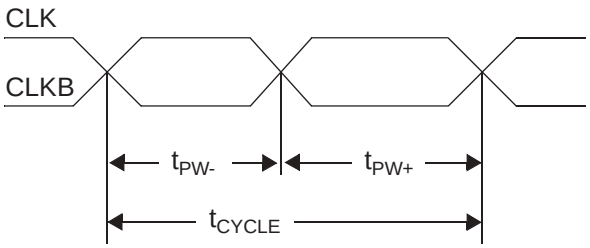
$t_J = t_{4CYCLE, i} - t_{4CYCLE, i+1}$ over 10,000 consecutive cycles

Figure 3. Short-term jitter



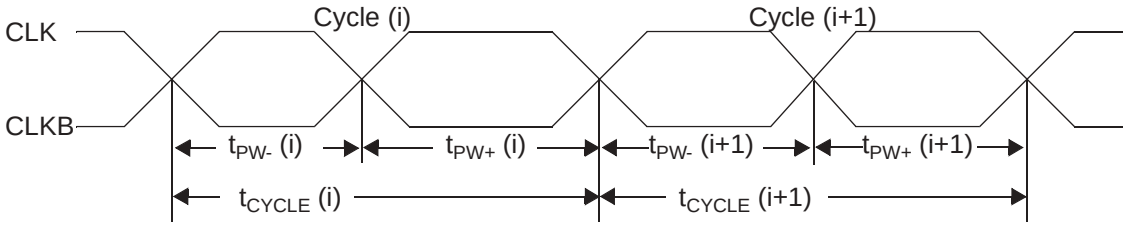
$t_J = t_{CYCLE,i} - t_{CYCLE, i+1}$ over 10,000 consecutive cycles

Figure 4. Cycle-to-cycle jitter



$DC = (t_{PW+} / t_{CYCLE})$

Figure 5. Duty Cycle



$t_{DC,ERR} = t_{PW+}(i) - t_{PW+}(i+1)$ and $t_{PW-}(i) - t_{PW-}(i+1)$

Figure 6. Cycle-to-cycle Duty Cycle Error

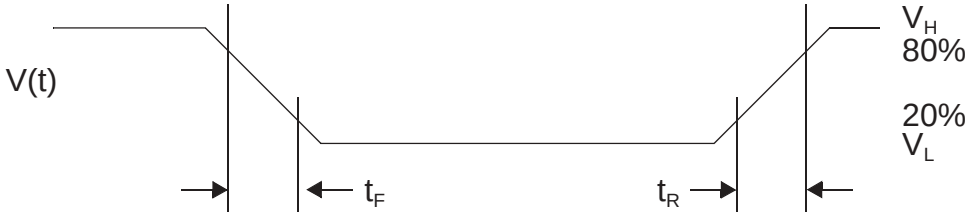


Figure 7. Input and Output Voltage Waveforms

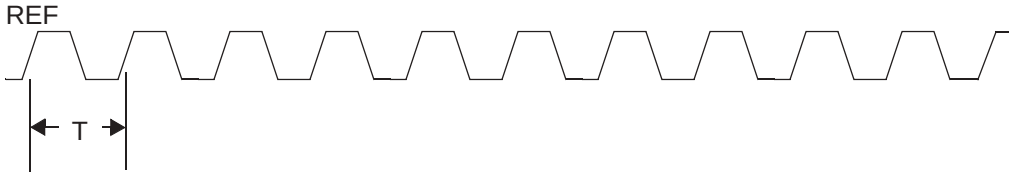
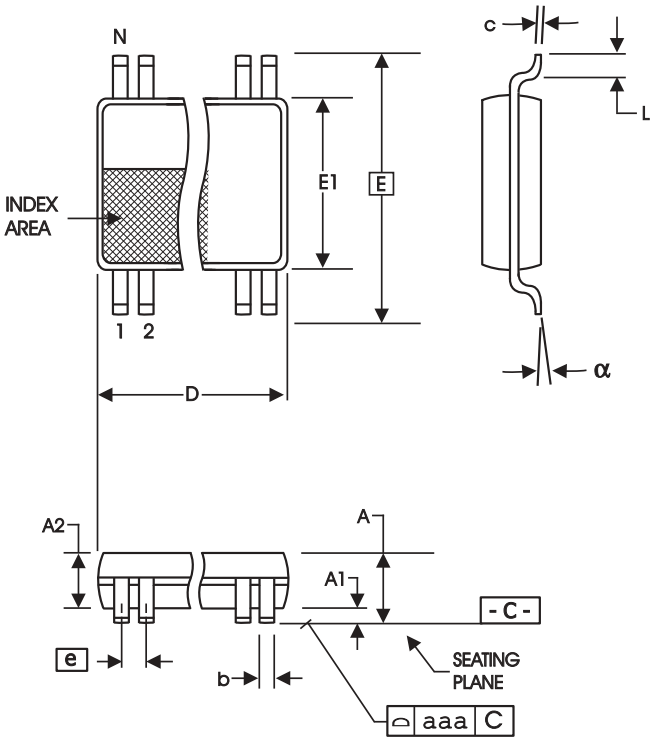


Figure 8. REF Jitter



4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
16	4.90	5.10	.193	.201

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

Ordering Information

ICS9219yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

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