Integrated Circuit Systems, Inc.

ICS9341

133MHz Clock Generator and Integrated Buffer for PowerPC™

General Description

The **ICS9341** generates all clocks required for high speed PowerPC RISC microprocessor systems. Generating clocks in phase with an external reference frequency.

Spread Spectrum may be enabled by driving the SS_EN pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9341** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Features

Generates the following system clocks:

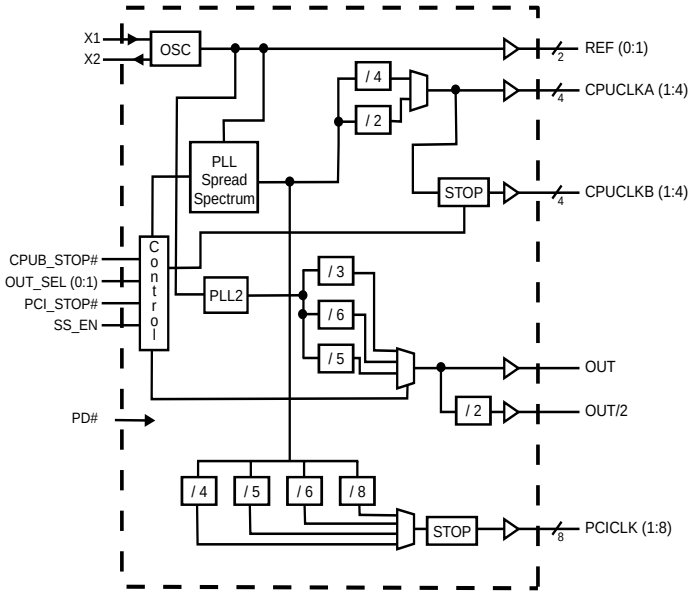
- 4-CPUA (3.3V, up to 133MHz)
- 4-CPUB (3.3V, up to 133MHz)
- 8-PCI (3.3V, 33.3MHz)
- 1-OUT (3.3v, 64MHz)
- 1-OUT/2 (3.3V, OUT/2MHz)
- 2-REF (3.3V, 14.318MHz)

- Up to 133MHz frequency support.
- Stop clocks for power management
- Spread Spectrum for EMI control
  ±.25% center spread

Skew characteristics:

- CPU - CPU: <350ps
- CPU - PCI: <500ps
- PCI - PCI: <500ps

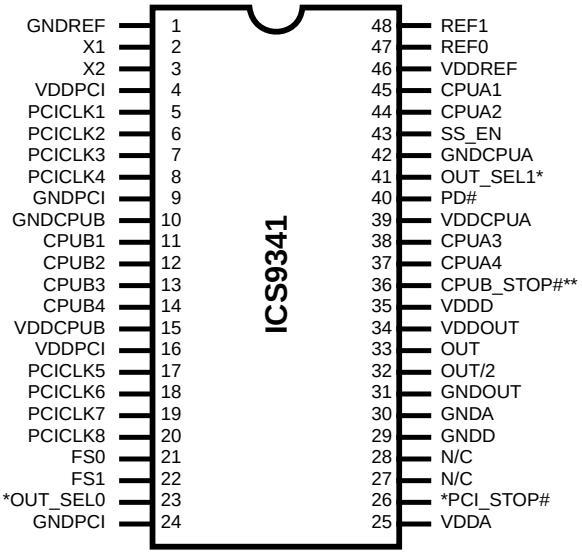
Block Diagram



Power Groups:

VDDREF, GNDREF = REF, X1, X2
GNDPCI, VDDPCI = PCICLK
VDD66, GND66 = 3V66
VDD48, GND48 = 48MHz
VDDCOR, GNDCOR = PLL Core
VDDLCPU/2 , GNDLCPU/2 = CPU/2
VDDLIOAPIC, GNDIOAPIC = IOAPIC

Pin Configuration



48-pin SSOP

* Internal pull-up resistor of 120K to 3.3V on indicated inputs

** Internal pull-down resistor of 120K to GND on indicated inputs.

Pin Descriptions

Pin number	Pin name	Type	Description
1	GNDREF	PWR	Ground pin for REF clocks.
2	X1	IN	XTAL_IN 14.318MHz crystal input.
3	X2	OUT	XTAL_OUT Crystal output.
4, 16	VDDPCI	PWR	3.3Volts power pin for PCICLKs.
5, 6, 7, 8, 17, 18, 19, 20	PCICLK (1:8)	OUT	PCI clock output at 3.3V. Synchronous to CPU clocks.
9, 24	GNDPCI	PWR	Ground pin for PCI clocks.
10	GNDCPUB	PWR	Ground pin for CPUB clocks.
11, 12, 13, 14	CPUB (1:4)	OUT	CPUCLK outputs up to 133.3MHz.
15	VDDCPUB	PWR	Power pin for the CPU bank B CLKs. 3.3V.
21, 22	FS (0:1)	IN	Logic - input for frequency selection.
23, 41	*OUT_SEL (0:1)	IN	These control the output functionality of the OUT and OUT/2 pins. Refer to table for details.
24	GNDPCI	PWR	Gnd pin for PCICLKs.
25	VDDA	PWR	Power for analog outputs.
26	*PCI_STOP#	IN	This active low input stops PCI clocks.
27, 28	N/C	-	Not connected
29	GNDD	PWR	Digitial ground
30	GNDA	PWR	Analog ground
31	GNDOUT	PWR	Ground for output pins.
32	OUT/2	OUT	Half the OUT frequency. Dependent on OUT_SEL. Refer to table for details.
33	OUT	OUT	This output frequency is dependent on OUT_SEL. Refer to table for details.
34	VDDOUT	PWR	Power for OUT pins 3.3V.
35	VDDD	PWR	Power for digitial outputs.
36	CPUB_STOP#**	IN	This active low input stops the CPUB clocks at a logic "0" level when input low.
45, 44, 38, 37	CPUA (1:4)	OUT	CPUCLK outputs up to 133.3MHz.
39	VDDCPUA	PWR	Power pin for the CPU bank A CLKs. 3.3V.
40	PD#	IN	This asynchronous input powers down the chip when drive active(Low). The internal PLLs are disabled and all the output clocks are held at a Low state.
42	GNDCPUA	PWR	Ground pin for CPUB clocks.
43	SS_EN	IN	Spread spectrum is turned on by driving this input high and turned off by driving low.
46	VDDREF	PWR	Power pin for REF clocks.
47, 48	REF	OUT	14.318MHz reference clock outputs at 3.3V.

Frequency Selection

FS1	FS0	CPUA, CPUB (MHz)	PCI (MHz)	REF (MHz)
1	1	133.3	33.3	14.318
1	0	100	33.3	14.318
0	1	83.3	33.3	14.318
0	0	66.6	33.3	14.318

OUT_SEL1	OUT_SEL0	OUT (MHz)	OUT/2 (MHz)
1	1	48	24
1	0	40	20
0	1	64	32
0	0	Stopped	Stopped

PD# Timing Diagram

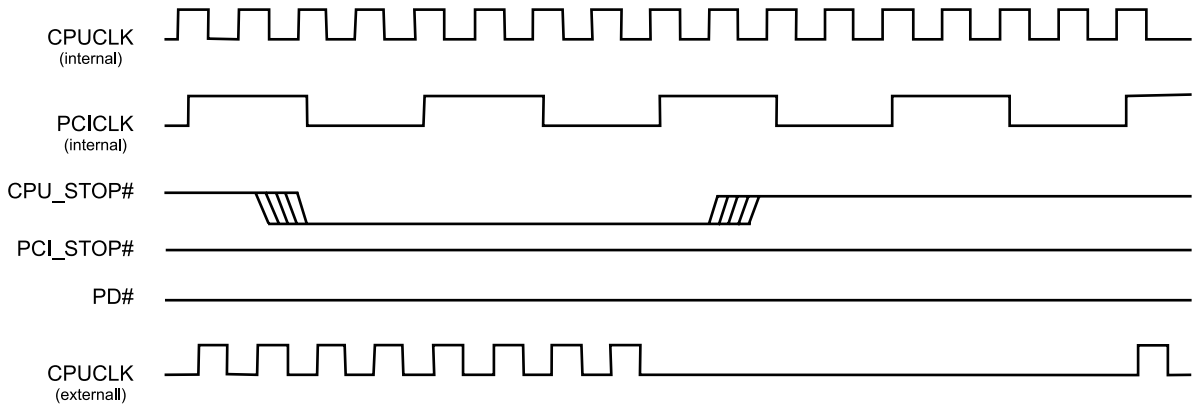
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9341 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

CPU_STOP# Timing Diagram

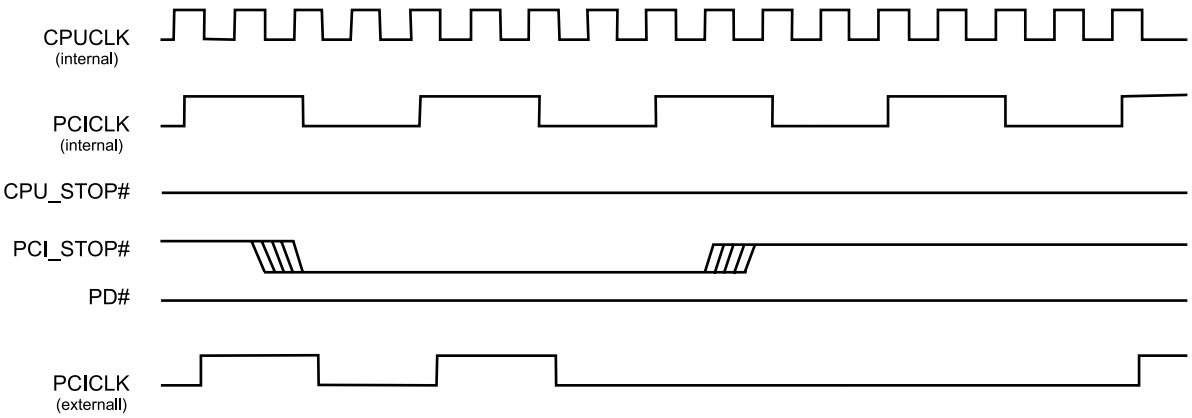
CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU and 3V66 clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU clock) and must be internally synchronized to the external output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. The internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. PD# and PCI_STOP# are shown in a high state.

PCI_STOP# Timing Diagram

PCI_STOP# is an input to the clock synthesizer. It is used to turn off the PCI clocks for low power operation. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. **ONLY one rising edge of PCICLK_F is allowed** after the clock control logic switched for the PCI outputs to become enabled/disabled.



Notes:
1. All timing is referenced to CPUCLK.
2. Internal means inside the chip.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high state.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	Select @ 66MHz; Max discrete cap loads		215	250	mA
	$I_{DD3.3OP83}$	Select @ 83MHz; Max discrete cap loads		200	225	mA
	$I_{DD3.3OP100}$	Select @ 100MHz; Max discrete cap loads		180	200	mA
	$I_{DD3.3OP133}$	Select @ 133MHz; Max discrete cap loads		160	175	mA
Power Down Supply Current	$I_{DD3.3PD}$	PD# = 0		160	300	µA
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	13.5	18	22.5	pF
Transition Time[1]	T_{Trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_S	From 1st crossing to 1% target Freq.		1		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{CPUA-CPUB}$	V_T = 1.5 V		100	350	ps
Skew[1]	$t_{CPU-PCI}$	V_T = 1.5 V		500	800	ps

Electrical Characteristics - CPUA

T_A = 0 - 70º C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -8.0 mA	2	2.4		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.32	0.4	V
Output High Current	I_{OH2B}	V_{OH} =1.7 V		-37	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2.5	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1	2.5	ns
Duty Cycle	d_{t2B}[1]	VT = 1.5 V	40	50	55	%
Skew	t_{sk2B}[1]	VT = 1.5 V		125	175	ps
Jitter, Cycle-to-cycle	$tj_{cyc-cyc2B}$[1]	VT = 1.5 V		230	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUB

T_A = 0 - 70º C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -8.0 mA	2	2.4		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.32	0.4	V
Output High Current	I_{OH2B}	V_{OH} =1.7 V		-37	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.9	3	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	3	ns
Duty Cycle	d_{t2B}[1]	VT = 1.5 V	40	49	55	%
Skew	t_{sk2B}[1]	VT = 1.5 V		90	175	ps
Jitter, Cycle-to-cycle	$tj_{cyc-cyc2B}$[1]	VT = 1.5 V		230	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70º C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L =30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	47		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.8	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.7	2.5	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		150	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		120	500	ps

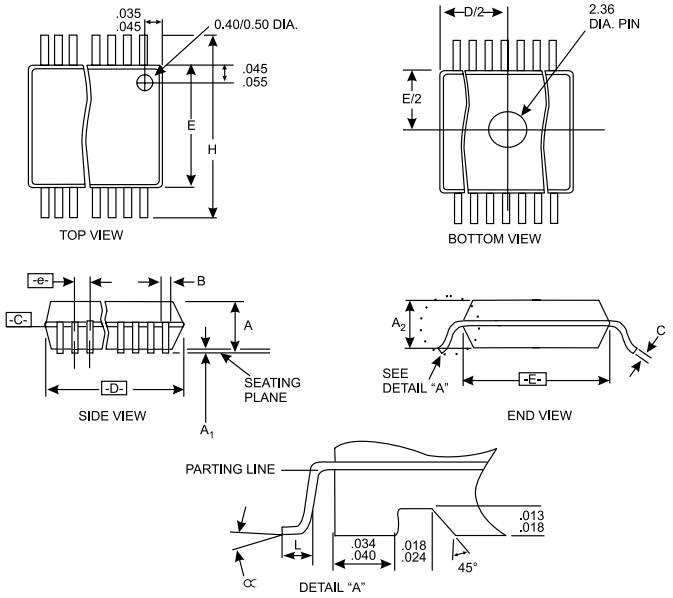
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, OUT, OUT/2

T_A = 0 - 70º C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 10 mA		0.33	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-30	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	23		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; OUT	1.5	1.8	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; OUT	1.5	2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V; OUT	45	52	55	%
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; OUT/2	1.5	2.2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; OUT/2	1.5	2.1	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V; OUT/2	45	50	55	%
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; REF	1.5	2.7	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; REF	1.5	2.8	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V; REF	45	50	55	%
Jitter, Cycle-to-cycle1	$t_{jcyc-cyc5}$	V_T = 1.5 V; OUT, OUT/2		280	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V; REF		450	1000	ps

[1]Guaranteed by design, not 100% tested in production.



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9341yF

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device