Integrated Circuit Systems, Inc.

ICS952702

Programmable Timing Control Hub for K7™ System

Recommended Application:

SiS746/746FX style chipset

Output Features:

- 1 - Pair of differential open drain CPU outputs
- 1 - Single-ended open drain CPU output
- 8 - PCICLK @ 3.3V including 2 PCI clock free running
- 2 - AGPCLK @ 3.3V
- 3 - REF @ 3.3V
- 2 - ZCLK @ 3.3V
- 2 - IOAPIC @ 2.5V
- 1 - 12_48MHz @ 3.3V
- 1 - 24_48MHz @ 3.3V

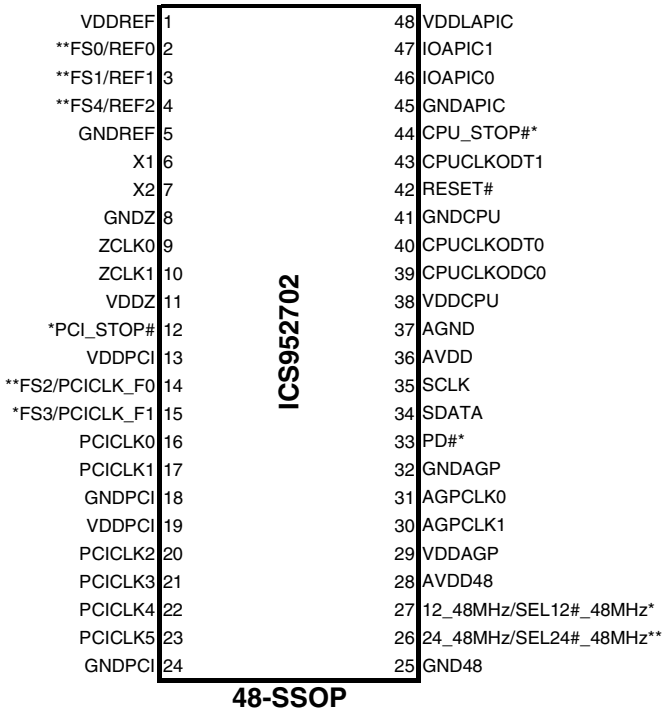
Key Specifications:

- CPU Output Jitter <250ps
- AGP Output Jitter <250ps
- ZCLK Output Jitter <250ps
- PCI Output Jitter <500ps
- CPU-AGP/PCI/ZCLK skew: 2.5ns~3.5ns

Features/Benefits:

- Selectable synchronous/asynchronous AGP/PCI frequency
- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference or XTAL input.

Pin Configuration



48-SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Functionality

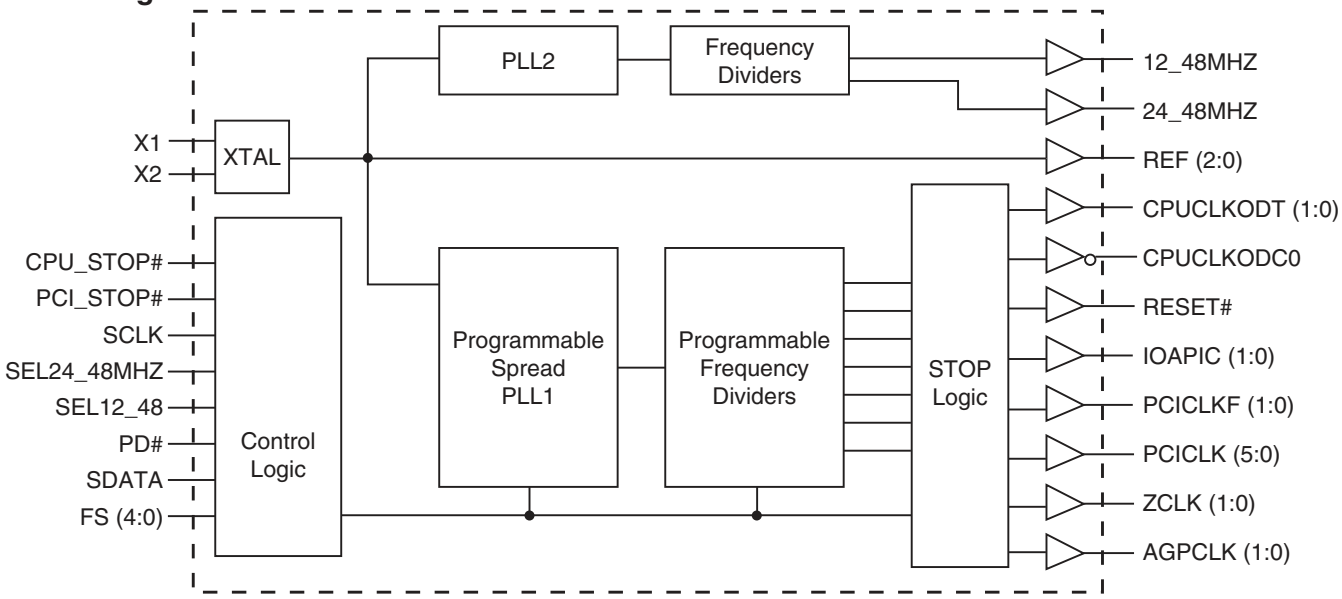
Bit4	Bit3	Bit2	Bit1	Bit0	CPU	ZCLK	AGP	PCI
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz
0	0	0	0	0	200.00	133.33	66.67	33.33
0	0	0	0	1	200.99	133.99	67.00	33.50
0	0	0	1	0	200.00	66.67	66.67	33.33
0	0	0	1	1	206.00	137.33	68.67	34.33
0	0	1	0	0	133.33	133.33	66.67	33.33
0	0	1	0	1	214.00	142.66	71.33	35.67
0	0	1	1	0	218.00	145.33	72.67	36.33
0	0	1	1	1	222.00	148.00	74.00	37.00
0	1	0	0	0	100.00	133.33	66.67	33.33
0	1	0	0	1	100.99	134.65	67.33	33.66
0	1	0	1	0	100.00	66.67	66.67	33.33
0	1	0	1	1	103.00	137.33	68.67	34.33
0	1	1	0	0	100.00	133.33	66.67	33.33
0	1	1	0	1	107.00	142.66	71.33	35.67
0	1	1	1	0	109.00	145.33	72.67	36.33
0	1	1	1	1	111.00	148.00	74.00	37.00
1	0	0	0	0	166.67	133.33	66.67	33.33
1	0	0	0	1	166.99	133.59	66.80	33.40
1	0	0	1	0	166.67	66.67	66.67	33.33
1	0	0	1	1	171.67	137.33	68.67	34.33
1	0	1	0	0	175.00	140.00	70.00	35.00
1	0	1	0	1	178.34	142.66	71.33	35.67
1	0	1	1	0	181.67	145.33	72.67	36.33
1	0	1	1	1	185.00	148.00	74.00	37.00
1	1	0	0	0	133.33	133.33	66.67	33.33
1	1	0	0	1	133.99	133.99	67.00	33.50
1	1	0	1	0	133.33	66.67	66.67	33.33
1	1	0	1	1	137.33	137.33	68.67	34.33
1	1	1	0	0	140.00	140.00	70.00	35.00
1	1	1	0	1	142.66	142.66	71.33	35.67
1	1	1	1	0	145.33	145.33	72.67	36.33
1	1	1	1	1	148.00	148.00	74.00	37.00

General Description

The **ICS952702** is a two chip clock solution for desktop designs using SIS 746 style chipsets. When used with a zero delay buffer such as the ICS9179-16 for PC133 or the ICS93735 for DDR applications it provides all the necessary clocks signals for such a system.

The **ICS952702** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
1	5	REF output, Xtal
11	8	Hyper ZCLK output
28	25	24/48MHz fixed, Fixed PLL (Fix1)
13,19	18,24	PCICLK output
29	32	AGP output
48	45	IOAPIC output
38	41	CPU_T/C output
36	37	CPU PLL, CPU MCLK

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	**FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	**FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
4	**FS4/REF2	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
5	GNDREF	PWR	Ground pin for the REF outputs.
6	X1	IN	Crystal input, Nominally 14.318MHz.
7	X2	OUT	Crystal output, Nominally 14.318MHz
8	GNDZ	PWR	Ground pin for the ZCLK outputs
9	ZCLK0	OUT	3.3V Hyperzip clock output.
10	ZCLK1	OUT	3.3V Hyperzip clock output.
11	VDDZ	PWR	Power supply for ZCLK clocks, nominal 3.3V
12	*PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low.
13	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
14	**FS2/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
15	*FS3/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
16	PCICLK0	OUT	PCI clock output.
17	PCICLK1	OUT	PCI clock output.
18	GNDPCI	PWR	Ground pin for the PCI outputs
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	PCICLK2	OUT	PCI clock output.
21	PCICLK3	OUT	PCI clock output.
22	PCICLK4	OUT	PCI clock output.
23	PCICLK5	OUT	PCI clock output.
24	GNDPCI	PWR	Ground pin for the PCI outputs
25	GND48	PWR	Ground pin for the 48MHz outputs
26	24_48MHz/SEL24#_48MHz**	I/O	Selectable 24 or 48MHz clock output / Latched select input for 24/48MHz output. 0=24MHz, 1 = 48MHz.
27	12_48MHz/SEL12#_48MHz*	I/O	Selectable 12 or 48MHz clock output / Latched select input for 12/48MHz output. 0=12MHz, 1 = 48MHz.
28	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V
29	VDDAGP	PWR	Power supply for AGP clocks, nominal 3.3V
30	AGPCLK1	OUT	AGP clock output
31	AGPCLK0	OUT	AGP clock output
32	GNDAGP	PWR	Ground pin for the AGP outputs
33	PD#*	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms.
34	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
35	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
36	AVDD	PWR	3.3V Analog Power pin for Core PLL
37	AGND	PWR	Analog Ground pin for Core PLL
38	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
39	CPUCLKODC0	OUT	"Complememtary" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
40	CPUCLKODT0	OUT	True clock of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
41	GNDCPU	PWR	Ground pin for the CPU outputs
42	RESET#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
43	CPUCLKODT1	OUT	True clock of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
44	CPU_STOP#*	IN	Stops all CPUCLK besides the free running clocks
45	GNDAPIC	PWR	Ground pin for the IOAPIC outputs.
46	IOAPIC0	OUT	IOAPIC clock outputs, norminal 2.5V.
47	IOAPIC1	OUT	IOAPIC clock outputs, norminal 2.5V.
48	VDDLAPIC	PWR	Power pin for the IOAPIC outputs. 2.5V.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor

General SMBus serial interface information for the ICS952702

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**ICS (Slave/Receiver)**
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**ICS (Slave/Receiver)**
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3$_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 1: Frequency Selection Table

FSA FSB

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	ZCLK	AGP	PCI	Spread %
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	
0	0	0	0	0	200.00	133.33	66.67	33.33	+/-0.35% center
0	0	0	0	1	200.99	133.99	67.00	33.50	+/-0.35% center
0	0	0	1	0	200.00	66.67	66.67	33.33	+/-0.35% center
0	0	0	1	1	206.00	137.33	68.67	34.33	+/-0.35% center
0	0	1	0	0	133.33	133.33	66.67	33.33	+/-0.35% center
0	0	1	0	1	214.00	142.66	71.33	35.67	+/-0.35% center
0	0	1	1	0	218.00	145.33	72.67	36.33	+/-0.35% center
0	0	1	1	1	222.00	148.00	74.00	37.00	+/-0.35% center
0	1	0	0	0	100.00	133.33	66.67	33.33	+/-0.35% center
0	1	0	0	1	100.99	134.65	67.33	33.66	+/-0.35% center
0	1	0	1	0	100.00	66.67	66.67	33.33	+/-0.35% center
0	1	0	1	1	103.00	137.33	68.67	34.33	+/-0.35% center
0	1	1	0	0	100.00	133.33	66.67	33.33	+/-0.35% center
0	1	1	0	1	107.00	142.66	71.33	35.67	+/-0.35% center
0	1	1	1	0	109.00	145.33	72.67	36.33	+/-0.35% center
0	1	1	1	1	111.00	148.00	74.00	37.00	+/-0.35% center
1	0	0	0	0	166.67	133.33	66.67	33.33	+/-0.35% center
1	0	0	0	1	166.99	133.59	66.80	33.40	+/-0.35% center
1	0	0	1	0	166.67	66.67	66.67	33.33	+/-0.35% center
1	0	0	1	1	171.67	137.33	68.67	34.33	+/-0.35% center
1	0	1	0	0	175.00	140.00	70.00	35.00	+/-0.35% center
1	0	1	0	1	178.34	142.66	71.33	35.67	+/-0.35% center
1	0	1	1	0	181.67	145.33	72.67	36.33	+/-0.35% center
1	0	1	1	1	185.00	148.00	74.00	37.00	+/-0.35% center
1	1	0	0	0	133.33	133.33	66.67	33.33	+/-0.35% center
1	1	0	0	1	133.99	133.99	67.00	33.50	+/-0.35% center
1	1	0	1	0	133.33	66.67	66.67	33.33	+/-0.35% center
1	1	0	1	1	137.33	137.33	68.67	34.33	+/-0.35% center
1	1	1	0	0	140.00	140.00	70.00	35.00	+/-0.35% center
1	1	1	0	1	142.66	142.66	71.33	35.67	+/-0.35% center
1	1	1	1	0	145.33	145.33	72.67	36.33	+/-0.35% center
1	1	1	1	1	148.00	148.00	74.00	37.00	+/-0.35% center

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	SS_EN	Spread Enable Control	RW	OFF	ON	1
Bit 5	27	SEL12/48MHz	Output Control	RW	12MHz	48MHz	Latch
Bit 4	-	FS4	Freq Select Bit 4	RW	See Table 1: Frequency Selection Table		Latch
Bit 3	-	FS3	Freq Select Bit 3	RW			Latch
Bit 2	-	FS2	Freq Select Bit 2	RW			Latch
Bit 1	-	FS1	Freq Select Bit 1	RW			Latch
Bit 0	-	FS0	Freq Select Bit 0	RW			Latch

I²C Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	26	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 6	27	48MHz	Output Control	RW	Disable	Enable	1
Bit 5	-	SEL24/48MHz	Output Control	RW	24MHz	48MHz	Latch
Bit 4	47	IOAPIC1	Output Control	RW	Disable	Enable	1
Bit 3	46	IOAPIC0	Output Control	RW	Disable	Enable	1
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	43	CPUCLKODT1	Output Control	RW	Disable	Enable	1
Bit 0	40/39	CPUCLKODT0/C0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	15	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 6	14	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 5	23	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	22	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	21	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	20	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	17	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	16	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	4	REF2	Output Control	RW	Disable	Enable	1
Bit 6	3	REF1	Output Control	RW	Disable	Enable	1
Bit 5	2	REF0	Output Control	RW	Disable	Enable	1
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	10	ZCLK1	Output Control	RW	Disable	Enable	1
Bit 2	9	ZCLK0	Output Control	RW	Disable	Enable	1
Bit 1	30	AGPCLK1	Output Control	RW	Disable	Enable	1
Bit 0	31	AGPCLK0	Output Control	RW	Disable	Enable	1

I²C Table: Async Frequency Selection & Output Skew Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	ASYNC2	Fix PLL Async Freq Programming bits	RW	See Table 2: Async Frequency Selection Table		0
Bit 6	-	ASYNC1		RW			0
Bit 5	-	ASYNC0		RW			0
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	ZCLKSkw1	CPU-ZCLK Skew Control	RW	00:0ps; 01:250ps; 10:500ps; 11:750ps This byte will advance or delay the skew by 250ps per step		0
Bit 2	-	ZCLKSkw0		RW			1
Bit 1	-	AGPSkw1	CPU-AGP Skew Control	RW	00:0ps; 01:250ps; 10:500ps; 11:750ps This byte will advance or delay the skew by 250ps per step		0
Bit 0	-	AGPSkw0		RW			1

Table 2: Asynchronous Frequency Selection Table

B4 bit7	B4 bit6	B4 bit5	ZCLK	AGP	PCI
0	0	0	Main PLL	Main PLL	Main PLL
0	0	1	132	66	33
0	1	0	132	75.4	37.7
0	1	1	132	88	44
1	0	0	Main PLL	Main PLL	Main PLL
1	0	1	132	66	33
1	1	0	132	75.4	33
1	1	1	132	88	33

Table 3: AGP Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	Bit	0		*01		10		11	MSB
			1		2		4		8
	0	0	4	100	8	1000	16	1100	32
	1	1	3	101	6	1001	12	1101	24
	10	10	5	110	10	1010	20	1110	40
	11	11	15	111	30	1011	60	1111	120
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Revision ID & Output Divider Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REV_ID3	Revision ID	R	-	-	0
Bit 6	-	REV_ID2		R	-	-	0
Bit 5	-	REV_ID1		R	-	-	0
Bit 4	-	REV_ID0		R	-	-	1
Bit 3	-	AGPDiv3	AGP divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table		1
Bit 2	-	AGPDiv2		RW			1
Bit 1	-	AGPDiv1		RW			0
Bit 0	-	AGPDiv0		RW			1

I²C Table: Slew Rate Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIStr1	PCICLK_F(1:0) Strength Control	RW	00=.63x; 01=.75x; 10=.88x; 11=1x Strength		1
Bit 6	-	PCIStr0		RW			1
Bit 5	-	PCIStr1	PCICLK(2:0) Strength Control	RW	00=.63x; 01=.75x; 10=.88x; 11=1x Strength		1
Bit 4	-	PCIStr0		RW			1
Bit 3	-	PCIStr1	PCICLK(5:3) Strength Control	RW	00=.63x; 01=.75x; 10=.88x; 11=1x Strength		1
Bit 2	-	PCIStr0		RW			1
Bit 1	-	AGPStr1	AGPCLK Strength Control	RW	00=.7x; 01=.8x; 10=.9x; 11=1x Strength		1
Bit 0	-	AGPStr0		RW			1

I²C Table: Reserved Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	1
Bit 6	-	Reserved	Reserved	R	-	-	1
Bit 5	-	Reserved	Reserved	R	-	-	1
Bit 4	-	Reserved	Reserved	R	-	-	1
Bit 3	-	Reserved	Reserved	R	-	-	1
Bit 2	-	Reserved	Reserved	R	-	-	1
Bit 1	-	Reserved	Reserved	R	-	-	1
Bit 0	-	Reserved	Reserved	R	-	-	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Watchdog Timer Control Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDSA control	WD soft alarm control	RW	Disable	Enable	0
Bit 6	-	WDHRB	WD Hard Alarm Status Read back	R	Normal	Alarm	X
Bit 5	-	WDSRB	WD Soft Alarm Status Read back	R	Normal	Alarm	X
Bit 4	-	GR_EN	Gear Shift Reset Enable	RW	Disable	Enable	0
Bit 3	-	WDTCtrl	Watch Dog Time base control	RW	290ms base	1160ms base	0
Bit 2	-	WD2	WD Timer Bit2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer will wait before it goes to alarm mode. Default is 7 X 290ms =2s.		1
Bit 1	-	WD1	WD Timer Bit1	RW			1
Bit 0	-	WD0	WD Timer Bit0	RW			1

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-	WDFSEN	WD Safe Frequency Mode	RW	Latched FS/Byte0	WD B10 b(4:0)	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte 0 Bit (4:0)		0
Bit 3	-	WD SF3		RW			1
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	N Div9	N Divider Bit 9	RW	-	-	X
Bit 5	-	M Div5	The decimal representation of M Div (5:0) + 2 is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	The decimal representation of N Div (9:0) + 8 is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	N Div6		RW	-	-	X
Bit 5	-	N Div5		RW	-	-	X
Bit 4	-	N Div4		RW	-	-	X
Bit 3	-	N Div3		RW	-	-	X
Bit 2	-	N Div2		RW	-	-	X
Bit 1	-	N Div1		RW	-	-	X
Bit 0	-	N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD(op)}$	Full Active, C_L = full load; Select @ 100MHz		180	250	mA
Power Down Supply Current	I_{DDPD}	All diff pairs tri-stated		1.2	12	mA
Input frequency	F_i	V_{DD} = 3.3 V;	11	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	30	45	pF
Spread Modulation Frequency[1]	f_{SS}		320		33	KHz
Clk Stabilization[1]	T_{STAB}	From V_{DD} Power-Up of de-assertion of PD# to 1st clock.			1.8	ms
Skew	$T_{CPU-AGP}$	CPU @ crossing, AGP @ 1.5V	2.5	3.1	3.5	ns
Skew	$T_{CPU-ZCLK}$	CPU @ crossing, ZCLK @ 1.5V	2.5	3.3	3.5	ns
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V CPU @ crossing, PCI @ 1.5V	2.5	2.9	3.5	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKODC/T

TA = 0 - 70°C; VDD = 1.7 V +/-5%; CL = 5 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	Termination to Vpull-up(external)	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to Vpull-up(external)			0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Time[1]	t_{r2B}	V_{OL} = 20%, V_{OH} = 80%		0.38	0.9	ns
Fall Time[1]	t_{f2B}	V_{OH} = 80%, V_{OL} = 20%,		0.44	0.9	ns
Differential voltage-AC[1]	V_{DIF}		0.4			V
Differential voltage-DC[1]	V_{DIF}		0.2			V
Differential Crossover Voltage[1]	V_X		550	1200	1250	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45	51.5	55	%
Skew[1]	t_{sk2B}	V_T = 50%		140	200	ps
Jitter Diff, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = VX		60	250	ps
Jitter SE, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.0V		100	250	ps
Jitter, Absolute[1]	t_{jabs2B}	V_T = 50%	-250		250	ps

Notes:

[1] - Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16		57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.25	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.1	2.5	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		170	500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		150	500	ps
	t_{jabs1}	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGPCLK, ZCLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V			-33	
		V_{OH} = 3.135 V	-33			mA
Output Low Current	I_{OL}[1]	V_{OL} = 1.95 V	38			
		V_{OL} = 0.4 V			30	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	2	2.2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.9	2.2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50.5	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		70	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		240	250	ps

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.6	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V		210	1000	ps
	t_{jabs5}	V_T = 1.5 V			800	ps

Electrical Characteristics - IOAPIC

T_A = 0 - 70°C;V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -5.5 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V			-27	
		V_{OH} = 2.375 V	-27			mA
Output Low Current	I_{OL}[1]	V_{OL} = 1.2 V	27			
		V_{OL} = 0.3 V			30	mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1	1.6	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1	1.6	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45	49.8	55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.25 V		300	500	ps
Skew	T_{sk4}[1]			10	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 12_48MHz, 24_48MHz

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V			-29	
		V_{OH} = 3.135 V	-23			mA
Output Low Current	I_{OL}[1]	V_{OL} = 1.95 V	29			
		V_{OL} = 0.4 V			27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.5	4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.5	4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.8	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		370	500	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

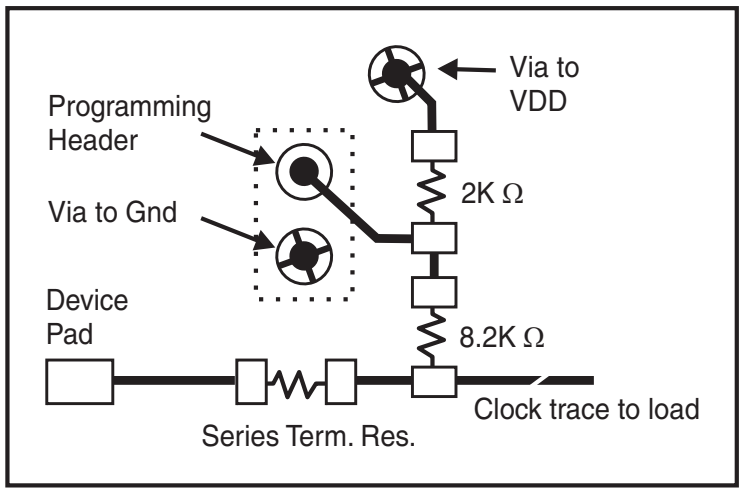
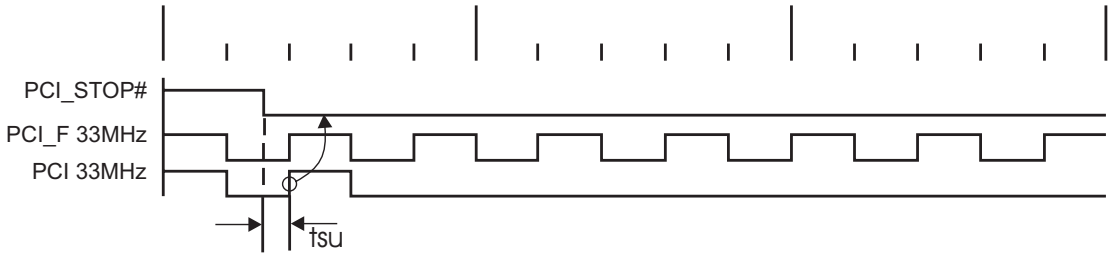


Fig. 1

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI and stoppable PCI_F clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

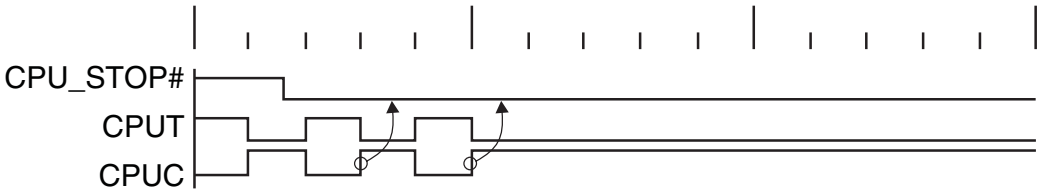
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

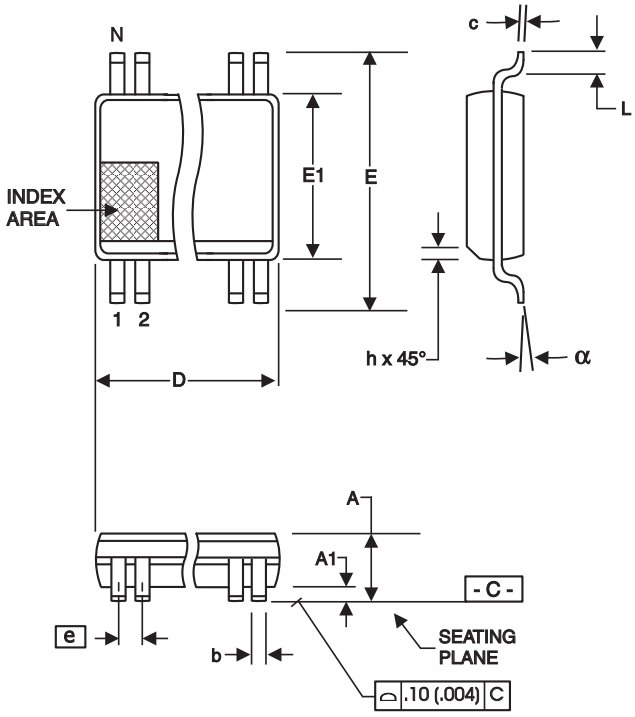
The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=Low and CPUC=High. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float



300 mil SSOP Package

300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
□	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

Ordering Information

ICS952702yFLFT

Example:

ICS 95XXXX y FLF - T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0795D—05/06/05

Revision History

Rev.	Issue Date	Description	Page #
D	5/6/2005	Added LF Ordering Information	16