3.3V CMOS 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER, DUAL 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16903

FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ± 0.3V, Normal Range**
- **V_{CC} = 2.7V to 3.6V, Extended Range**
- **V_{CC} = 2.5V ± 0.2V**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in TSSOP package**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Suitable for heavy loads**

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND (Outputs Only)	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK}	Continuous Clamp Current, V_I < 0 or V_I > V_{CC}	±50	mA
I_{OK}	Continuous Clamp Current, V_O < 0	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. This value is limited to 4.6V maximum.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
C_{OUT}	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

NOTE:

1. As applicable to the device type.

DESCRIPTION:

This 12-bit universal bus driver is built using advanced dual metal CMOS technology. This device has dual outputs and can operate as a buffer or an edge-triggered register. In both modes, parity is checked on APAR, which arrives one cycle after the data to which it applies. The $\overline{YERR}$ output, which is produced one cycle after APAR, is open drain.

MODE selects one of the two data paths. When MODE is low, the device operates as an edge-triggered register. On the positive transition of the clock (CLK) input and when the clock-enable ($\overline{CLKEN}$) input is low, data setup at the A inputs is stored in the internal registers. On the positive transition of CLK and when $\overline{CLKEN}$ is high, only data setup at the 9A-12A inputs is stored in their internal registers. When MODE is high, the device operates as a buffer and data at the A inputs passes directly to the outputs. The 11A/$\overline{YERREN}$ serves a dual purpose; it acts as a normal data bit and also enables $\overline{YERR}$ data to be clocked into the $\overline{YERR}$ output register.

When used as a single device, parity output enable ($\overline{PAROE}$) must be tied high; when parity input/output (PARI/O) is low, even parity is selected and when PARI/O is high, odd parity is selected. When used in pairs and $\overline{PAROE}$ is low, the parity sum is output on PARI/O for cascading to the second ALVCH16903. When used in pairs and $\overline{PAROE}$ is high, PARI/O accepts a partial parity sum from the first ALVCH16903.

A buffered output-enable ($\overline{OE}$) input can be used to place the 24 outputs and $\overline{YERR}$ in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

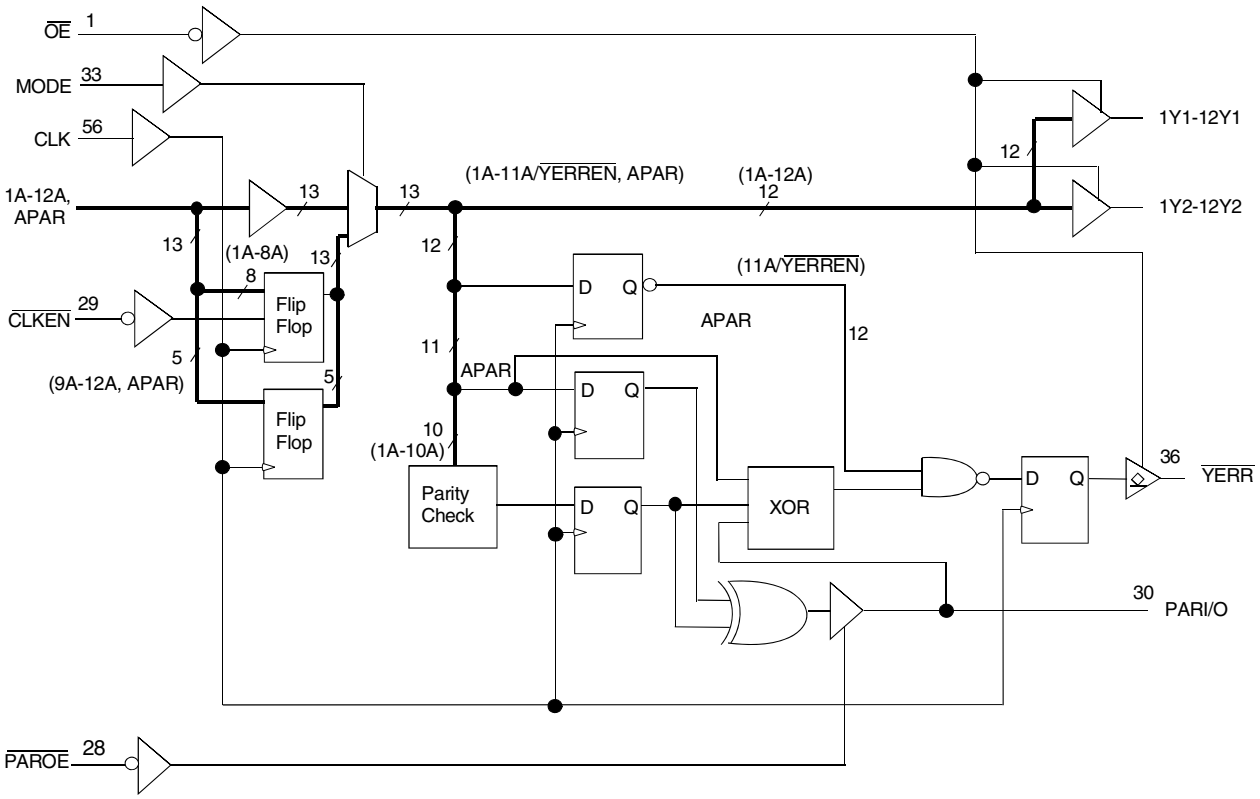
The ALVCH16903 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16903 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high-impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

APPLICATIONS:

- **3.3V high speed systems**
- **3.3V and lower voltage computing systems**

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE(1)

Inputs					Outputs	
$\overline{OE}$	MODE	$\overline{CLKEN}$	CLK	A	1Yx-8Yx	9Yx-12Yx
L	L	L	↑	H	H	H
L	L	L	↑	L	L	L
L	L	H	↑	H	Y(2)	H
L	L	H	↑	L	Y(2)	L
L	H	X	X	H	H	H
L	H	X	X	L	L	L
H	X	X	X	X	Z	Z

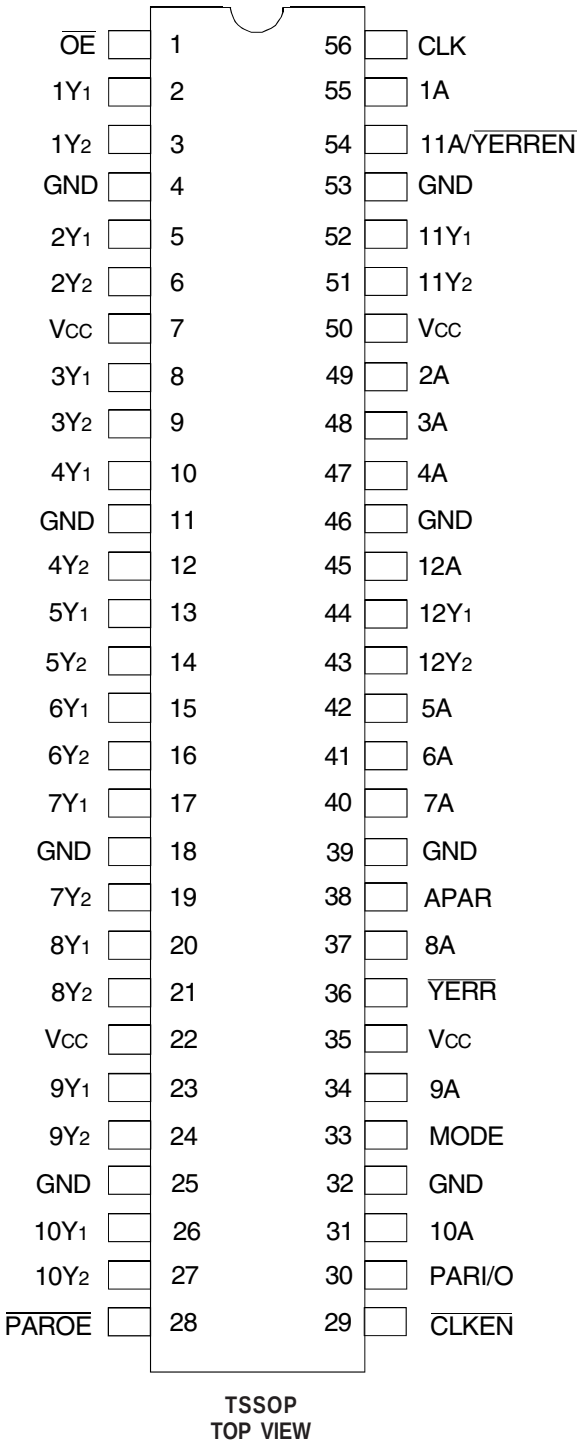
NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state conditions were established.

PARITY FUNCTION TABLE(1)

Inputs						Output
$\overline{OE}$	$\overline{PAROE}$(2)	11A/ $\overline{YERREN}$(3)	PARI/O	Σ OF INPUTS 1A-10A=H	APAR	$\overline{YERR}$
L	H	L	L	0, 2, 4, 6, 8, 10	L	H
L	H	L	L	1, 3, 5, 7, 9	L	L
L	H	L	L	0, 2, 4, 6, 8, 10	H	L
L	H	L	L	1, 3, 5, 7, 9	H	H
L	H	L	H	0, 2, 4, 6, 8, 10	L	L
L	H	L	H	1, 3, 5, 7, 9	L	H
L	H	L	H	0, 2, 4, 6, 8, 10	H	H
L	H	L	H	1, 3, 5, 7, 9	H	L
H	X	X	X	X	X	H
L	X	H	X	X	X	H

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. When used as a single device, $\overline{PAROE}$ must be tied HIGH.
3. Valid after appropriate number of clock pulses have set internal register.

PIN CONFIGURATION



TSSOP
TOP VIEW

PARI/O FUNCTION TABLE(1)

Inputs			Output
$\overline{PAROE}$	Σ OF INPUTS 1A-10A = H	APAR	PARI/O
L	0, 2, 4, 6, 8,10	L	L
L	1, 3, 5, 7, 9	L	H
L	0, 2, 4, 6, 8, 10	H	H
L	1, 3, 5, 7, 9	H	L
H	X	X	Z

NOTE:
1. This table applies to the first device of a cascaded pair of ALVCH16903 devices.

PIN DESCRIPTION

Pin Names	I/O	Description
1A-12A	I	Data Inputs(1)
1Y1-12Y2	O	3-State Data Outputs
CLK	I	Clock Input
$\overline{CLKEN}$	I	Clock Enable Input (Active LOW)
MODE	I	Select Pin
$\overline{YERREN}$	I	Error Signal Output Enable (Active LOW)
$\overline{PAROE}$	I	Parity Output Enable (Active LOW)
PARI/O	I/O	Parity Input/Output
$\overline{YERR}$	O	Error Signal (Open Drain)
$\overline{OE}$	I	Output Enable Input (Active LOW)
APAR	I	Parity Input

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
I_{OH}	YERR Output	V_{CC} = 0V to 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZ}(2)	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC} or GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V, V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA
Ci	Control Inputs	V_{CC} = 3.3V	V_I = V_{CC} or GND	—	5.5	—	pF
	Data Inputs			—	5.5	—	
Co	YERR Output	V_{CC} = 3.3V	V_O = V_{CC} or GND	—	5	—	pF
	Data Outputs			—	6	—	
Cio	PARI/O	V_{CC} = 3.3V	V_O = V_{CC} or GND	—	7	—	pF

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	–75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	–45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA
I_{BHLO}							

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS, xYx PORTS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA, V_{IH} = 1.7V	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA, V_{IH} = 1.7V	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 12mA, V_{IH} = 2V	2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA, V_{IH} = 2V	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA, V_{IL} = 0.7V	—	0.4	
			I_{OL} = 12mA, V_{IL} = 0.7V	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA, V_{IL} = 0.8V	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA, V_{IL} = 0.8V	—	0.55	
I_{OH}	High-Level Output Current	V_{CC} = 2.3V	Y Port	—	–12	mA
		V_{CC} = 2.7V		—	–12	
		V_{CC} = 3V	PARI/O	—	–12	
			Y Port	—	–24	
I_{OL}	Low-Level Output Current	V_{CC} = 2.3V	Y Port	—	12	mA
		V_{CC} = 2.7V		—	12	
		V_{CC} = 3V	PARI/O	—	12	
			Y Port	—	24	
			$\overline{YERR}$ Output	—	24	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OUTPUT DRIVE CHARACTERISTICS FOR $\overline{YERR}$ AND PARI/O

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	PARI/O	V_{CC} = 3V	I_{OH} = – 12mA, V_{IH} = 2V	2	—	V
V_{OL}	PARI/O	V_{CC} = 3V	I_{OL} = 12mA, V_{IL} = 0.8V	—	0.55	V
V_{OL}	$\overline{YERR}$ Output only	V_{CC} = 3V	I_{OL} = 24mA	—	0.5	V

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS FOR BUFFER MODE, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V Typical	V_{CC} = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	57.5	65	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		15	17.5	

OPERATING CHARACTERISTICS FOR REGISTER MODE, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V Typical	V_{CC} = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	57	87.5	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		16.5	34	

SIMULTANEOUS SWITCHING CHARACTERISTICS(1)

Parameter		From (Input)	To (Output)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Register mode	CLK	Y	1.8	6.5		6.1	1.8	5	ns
t_{PHL}				1.4	5.9		5.1	1.7	4.5	

NOTE:
1. All outputs switching.

SWITCHING CHARACTERISTICS(1)

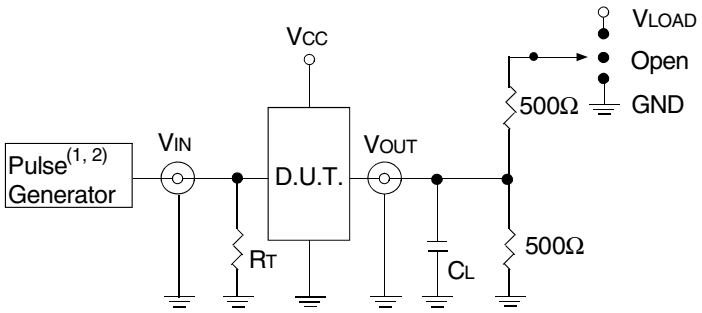
Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		125	—	125	—	125	—	MHz
t_{PLH} t_{PHL}	Propagation Delay, Buffer Mode xAx to xYx	1	4.4	—	4.2	1.1	3.8	ns
t_{PLH} t_{PHL}	Propagation Delay, Both Modes CLK to $\overline{YERR}$	1	5.7	—	4.9	1.4	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay, Both Modes CLK to PARI/O	1.2	8.6	—	7.9	1.7	6.6	ns
t_{PLH} t_{PHL}	Propagation Delay, Both Modes CLK to PARI/O	1	6.8	—	5.2	1.3	4.5	ns
t_{PLH} t_{PHL}	Propagation Delay, Both Modes Mode to xYx	1	5.9	—	5.8	1.3	4.9	ns
t_{PLH}	Propagation Delay, Register Mode	1	6.1	—	5.5	1.2	4.8	ns
t_{PHL}	CLK to xYx	1	5.9	—	4.9	1.2	4.6	
t_{PLH}	Propagation Delay, Both Modes $\overline{OE}$ to $\overline{YERR}$	1	3.6	—	4.2	1.9	4	ns
t_{PHL}	Propagation Delay, Both Modes $\overline{OE}$ to $\overline{YERR}$	1.2	5.1	—	4.9	1.5	4.2	ns
t_{PZH} t_{PZL}	Output Enable Time, Both Modes $\overline{OE}$ to xYx	1.1	6.5	—	6.4	1.4	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time, Both Modes $\overline{PAROE}$ to PARI/O	1	5.6	—	6	1	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time, Both Modes $\overline{OE}$ to xYx	1	6.4	—	5.2	1.7	5	ns
t_{PHZ} t_{PLZ}	Output Disable Time, Both Modes $\overline{PAROE}$ to PARI/O	1	3.2	—	3.8	1.2	3.8	ns
t_{SU}	Set-up Time, Register Mode, 1A-12A before CLK↑	1.7	—	1.9	—	1.45	—	ns
t_{SU}	Set-up Time, Buffer Mode, 1A to 10A before CLK↑	5.9	—	5.2	—	4.4	—	ns
t_{SU}	Set-up Time, Register Mode, APAR before CLK↑	1.2	—	1.5	—	1.3	—	ns
t_{SU}	Set-up Time, Buffer Mode, APAR before CLK↑	4.6	—	3.6	—	3.1	—	ns
t_{SU}	Set-up Time, Both Modes, PARI/O before CLK↑	2.4	—	2	—	1.7	—	ns
t_{SU}	Set-up Time, Buffer Mode, 11A/$\overline{YERREN}$ before CLK↑	2	—	1.9	—	1.6	—	ns
t_{SU}	Set-up Time, Register Mode, $\overline{CLKEN}$ before CLK↑	2.5	—	2.6	—	2.2	—	ns
t_H	Hold Time, Register Mode, 1A-12A after CLK↑	0.4	—	0.25	—	0.55	—	ns
t_H	Hold Time, Buffer Mode, 1A-10A after CLK↑	0.25	—	0.25	—	0.25	—	ns
t_H	Hold Time, Register Mode, APAR after CLK↑	0.7	—	0.4	—	0.7	—	ns
t_H	Hold Time, Buffer Mode, APAR after CLK↑	0.25	—	0.25	—	0.25	—	ns
t_H	Hold Time, Register Mode, PARI/O after CLK↑	0.25	—	0.25	—	0.4	—	ns
t_H	Hold Time, Buffer Mode, PARI/O after CLK↑	0.25	—	0.25	—	0.5	—	ns
t_H	Hold Time, Buffer Mode, 11A/$\overline{YERREN}$ after CLK↑	0.25	—	0.25	—	0.4	—	ns
t_H	Hold Time, Register Mode, $\overline{CLKEN}$ after CLK↑	0.25	—	0.5	—	0.4	—	ns
t_W	Pulse Width, CLK↑	3	—	3	—	3	—	ns
$t_{SK(O)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2 Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

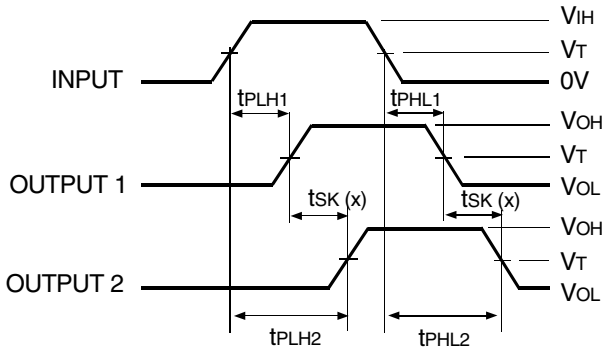
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

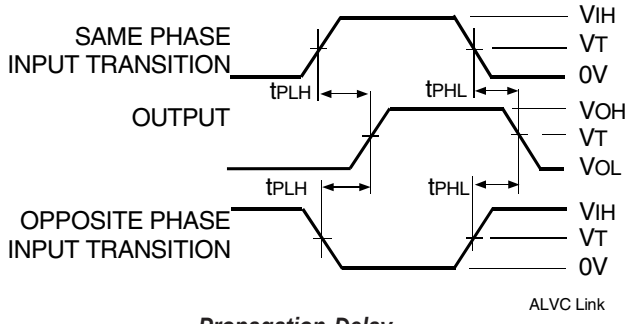


$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

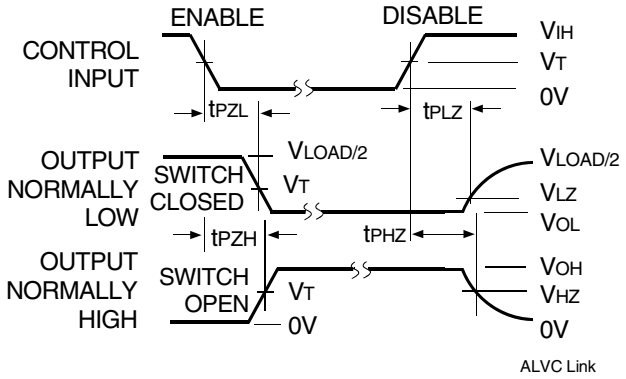
Output Skew - $t_{SK(x)}$

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



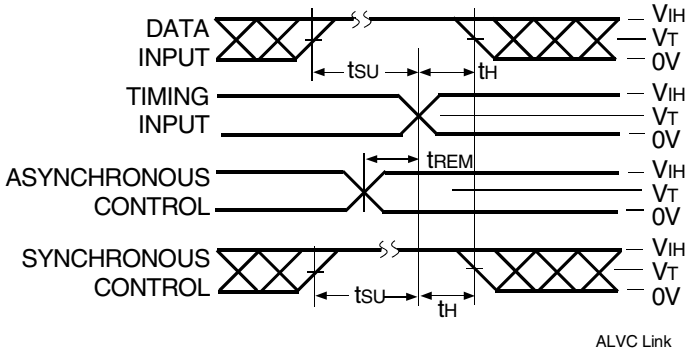
Propagation Delay



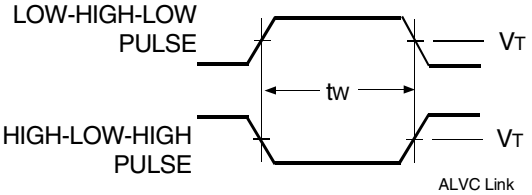
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

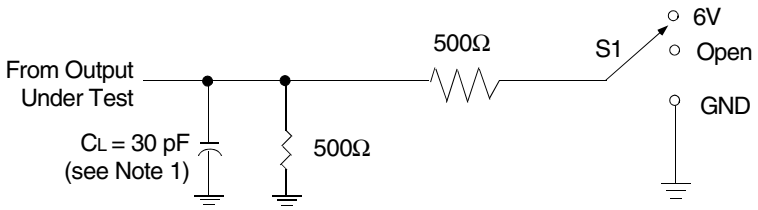


Set-up, Hold, and Release Times



Pulse Width

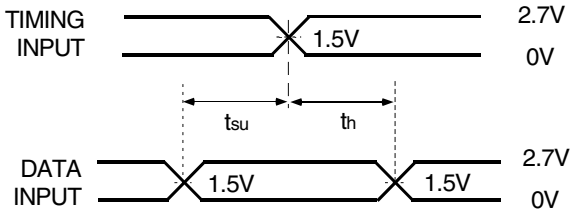
PARAMETER MEASUREMENT INFORMATION
VCC = 2.7V AND 3.3V ± 0.3V



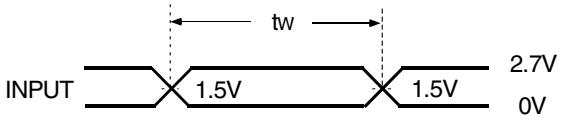
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6V GND

$\overline{YERR}$	S1
t_{PHL} (see Note 8) t_{PLH} (see Note 9)	6V 6V

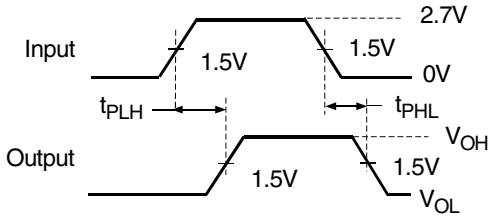
Load Circuit



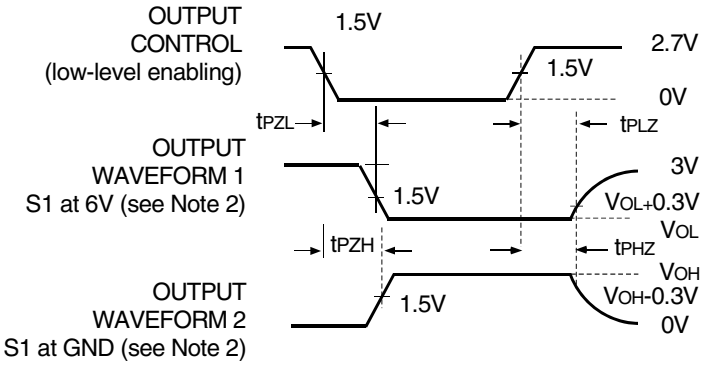
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



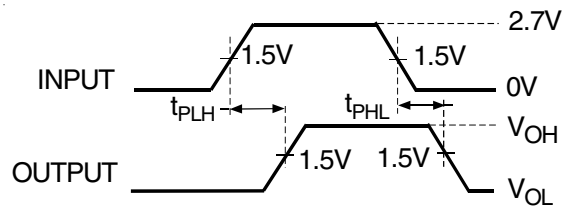
Voltage Waveforms
Propagation Delay Times



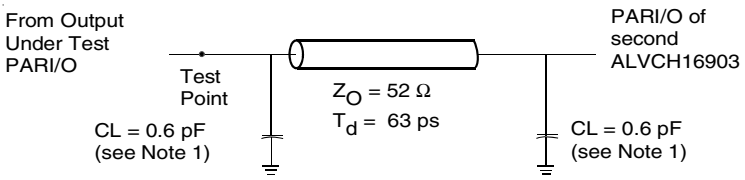
Voltage Waveforms
Enable and DisableTimes

NOTES:
1. CL includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50Ω, tr ≤ 2 ns, tf ≤ 2 ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. t_{PHL} is measured at 1.5V.
9. t_{PLH} is measured at V_{OL} +0.3V.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS
VCC = 2.7V AND 3.3V ± 0.3V

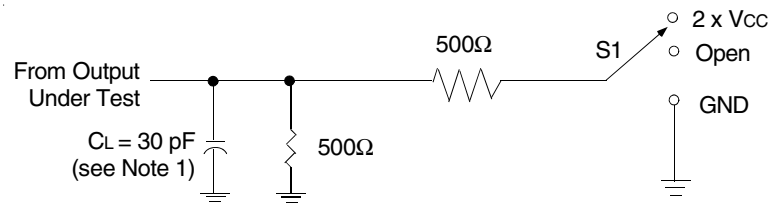


PARI/O Load Circuit



NOTE:
1. CL includes probe and jig capacitance.

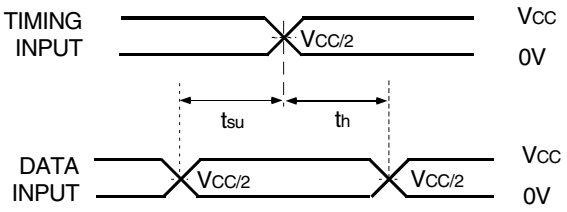
PARAMETER MEASUREMENT INFORMATION
VCC = 2.5V ±0.2V



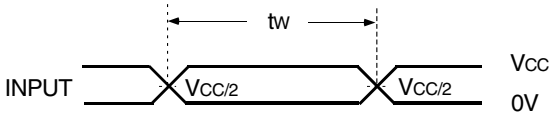
Load Circuit

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND

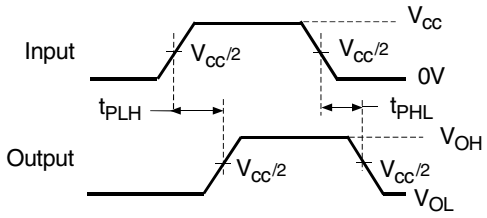
$\overline{YERR}$	S1
t_{PHL} (see Note 8)	2 x V_{CC}
t_{PLH} (see Note 9)	2 x V_{CC}



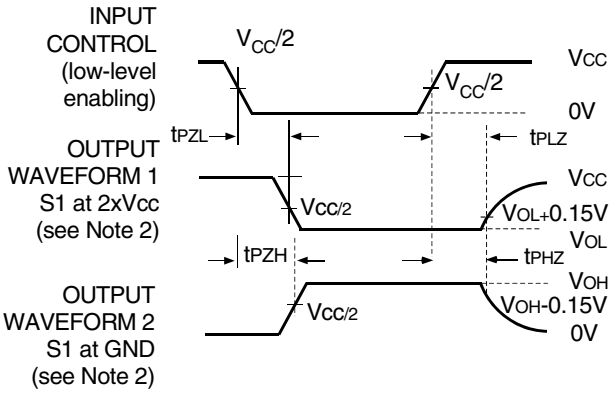
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



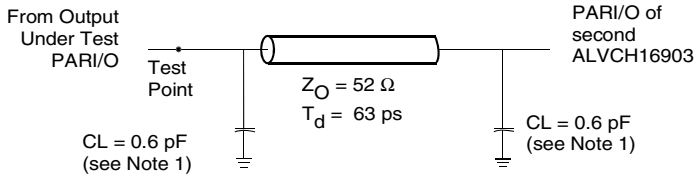
Voltage Waveforms
Propagation Delay Times



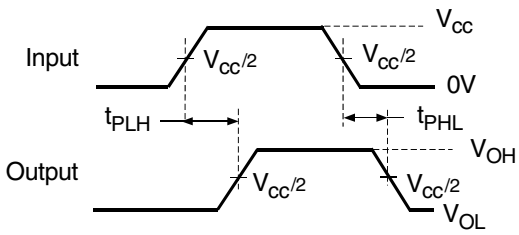
Voltage Waveforms
Enable and DisableTimes

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, tr ≤ 2 ns, tf ≤ 2 ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. t_{PHL} is measured at V_{CC} /2.
9. t_{PLH} is measured at V_{OL} + 0.15V.

PARAMETER MEASUREMENT INFORMATION
VCC = 2.5V ± 0.2V

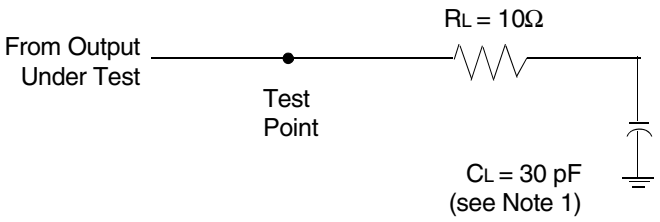


Load Circuit

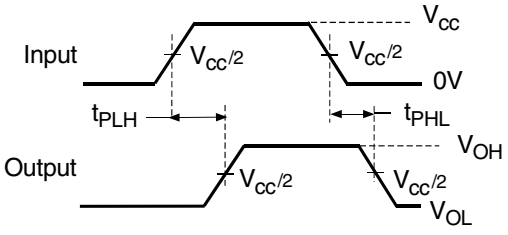


Voltage Waveforms
Propagation Delay Times

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Zo = 50Ω, tr ≤ 2 ns, tf ≤2ns.
3. t_{PLH} and t_{PHL} are the same as t_{pd}.



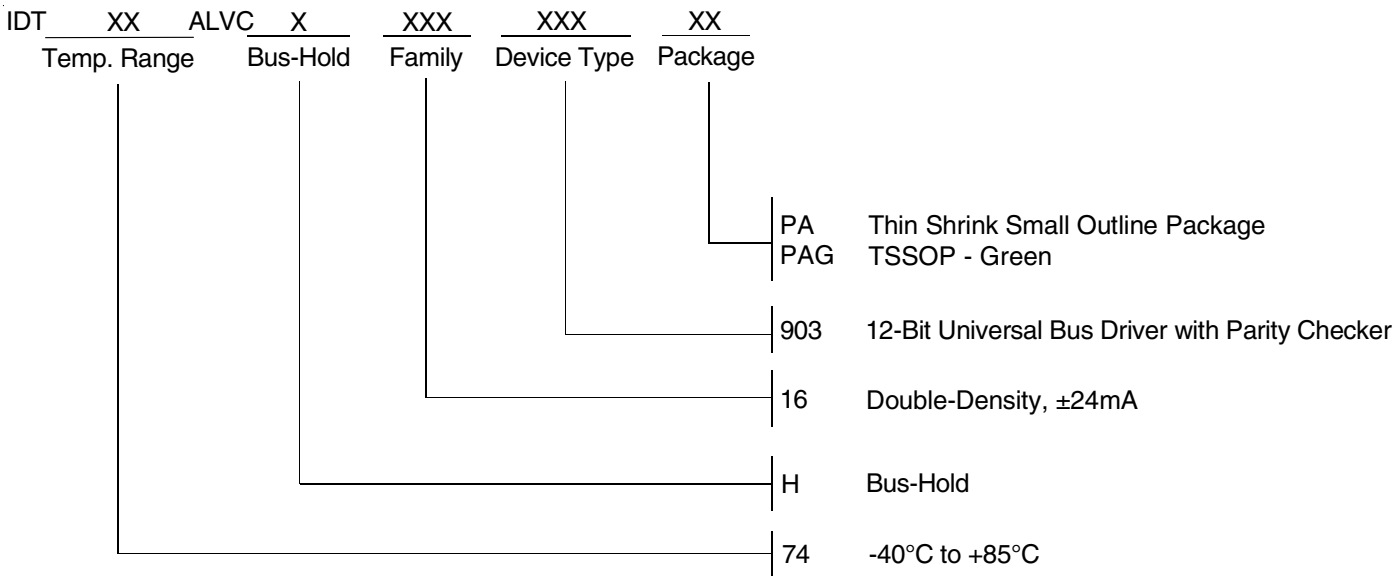
Load Circuit



Voltage Waveforms
Propagation Delay Times

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Zo = 50Ω, tr ≤ 2 ns, tf ≤2ns.

ORDERING INFORMATION



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