

IS61LF6436A IS61LF6432A

ISSI®

64K x 32, 64Kx36 SYNCHRONOUS FLOW-THROUGH STATIC RAM

OCTOBER 2005

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Power-down control by ZZ input
- JEDEC 100-Pin TQFP package
- Power Supply:
 - +3.3V V_{DD}
 - +3.3V or 2.5V V_{DDQ}
- Control pins mode upon power-up:
 - MODE in interleave burst mode
 - ZZ in normal operation mode
- Industrial Temperature Available:
(-40°C to +85°C)
- Lead-free available

DESCRIPTION

The *ISSI* IS61LF6432A and IS61LF6436A are high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, memory. IS61LF6432A is organized as 65,536 words by 32 bits. IS61LF6436A is organized as 65,536 words by 36 bits. They are fabricated with *ISSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. **BW_a** controls DQ_a, **BW_b** controls DQ_b, **BW_c** controls DQ_c, **BW_d** controls DQ_d, conditioned by **BWE** being LOW. A LOW on **GW** input would cause all bytes to be written.

Bursts can be initiated with either **ADSP** (Address Status Processor) or **ADSC** (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IS61LF6432A/36A and controlled by the **ADV** (burst address advance) input pin.

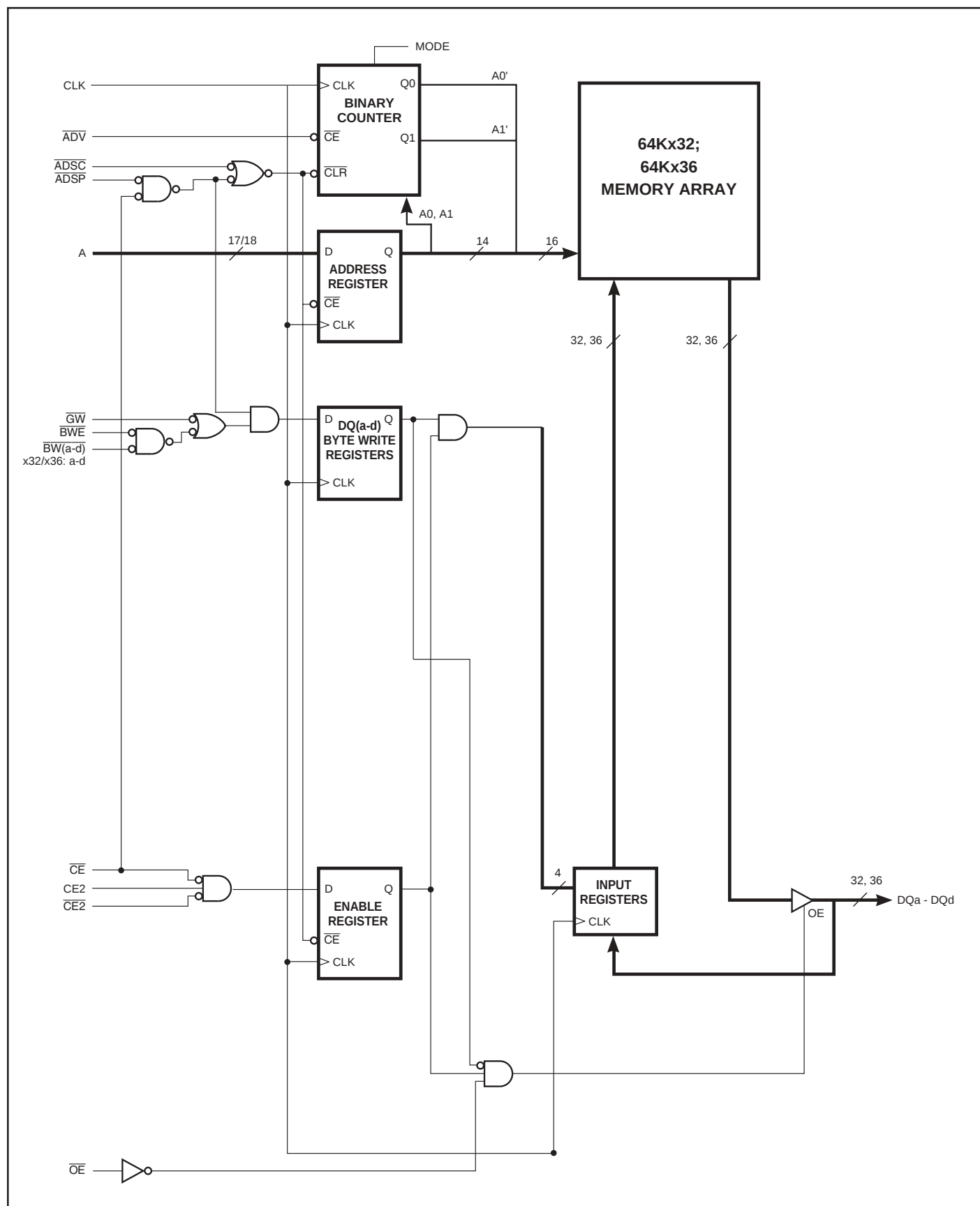
The mode pin is used to select the burst sequence order. Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

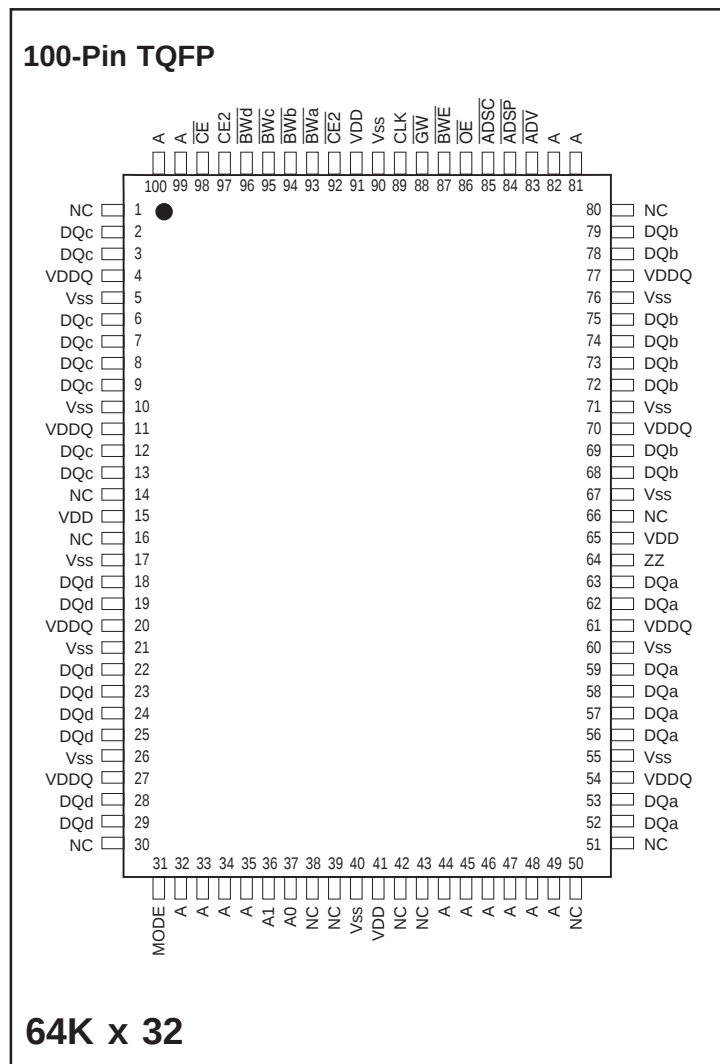
Symbol	Parameter	8.5	Unit
t _{KQ}	Clock Access Time	8.5	ns
t _{KC}	Cycle Time	11	ns
	Frequency	90	MHz

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BLOCK DIAGRAM



PIN CONFIGURATION

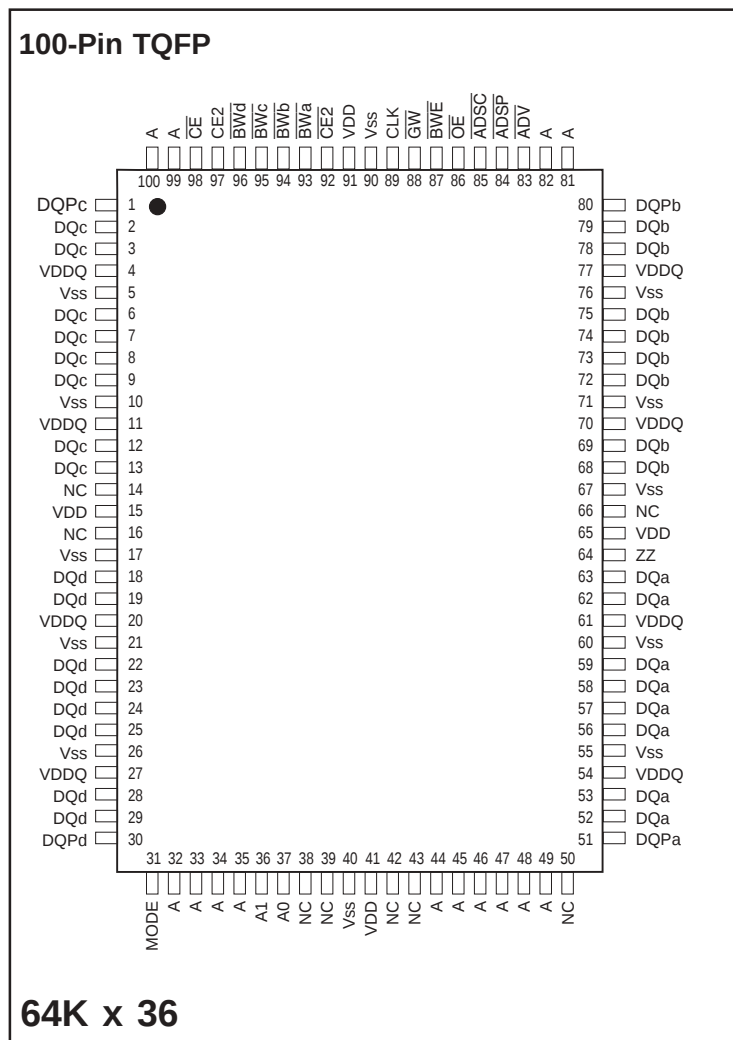


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWA-BWd}}$	Individual Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable

$\overline{\text{GW}}$	Synchronous Global Write Enable
$\overline{\text{CE}}, \overline{\text{CE2}}, \text{CE2}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
VDD	+3.3V Power Supply
Vss	Ground
VDDQ	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable

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DQPa-DQPd	Parity Data I/O

TRUTH TABLE

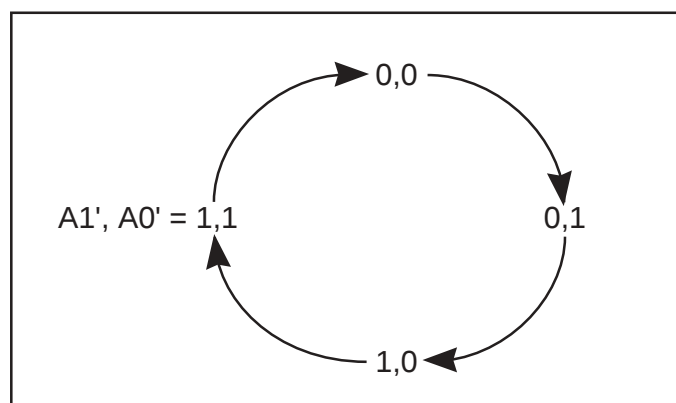
Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITE	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWA}$	$\overline{BWb}$	$\overline{BWC}$	$\overline{BWD}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to V _{SS} for I/O Pins	-0.5 to V _{DDQ} + 0.3	V
V _{IN}	Voltage Relative to V _{SS} for for Address and Control Inputs	-0.5 to V _{DD} + 0.5	V
V _{DD}	Voltage on V _{DD} Supply Relative to V _{SS}	-0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{DD}	3.3V (I/O) V _{DDQ}	2.5V (I/O) V _{DDQ}
Industrial	−40°C to +85°C	3.3V, +10%, −5%	3.3V, +10%, −5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	2.5V (I/O)		3.3V (I/O)		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = −4.0 mA (3.3V) I _{OH} = 1.0 mA (2.5V)	2.0	—	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V _{IH}	Input HIGH Voltage		1.7	V _{DD} + 0.3	2.0	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage		−0.3	0.7	−0.3	0.8	V
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{DD}	−5	5	−5	5	μA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , $\overline{OE} = V_I$	−5	5	−5	5	μA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		8.5	Unit
				Max.	
I _{CC}	AC Operating Supply Current	Device Selected, $\overline{OE} = V_{IH}$, ZZ ≤ V _{IL} , All Inputs ≤ 0.2V or ≥ V _{DD} − 0.2V, Cycle Time ≥ t _{KC} min.	IND.	150	mA
I _{SB1}	Standby Current CMOS Input	Device Deselected, V _{DD} = Max., V _{IN} ≤ V _{SS} + 0.2V or ≥ V _{DD} − 0.2V f = 0	IND.	75	mA
I _{ZZ}	Sleep Mode	ZZ > V _{IH}	IND.	35	mA

Notes:

1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to V_{SS}, or tied to V_{DD}.
2. The MODE pin should be tied to V_{DD} or V_{SS}. It exhibits ±10 μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} − 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

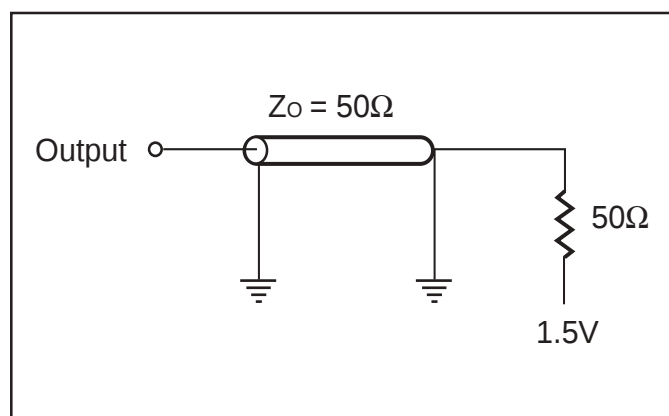


Figure 1

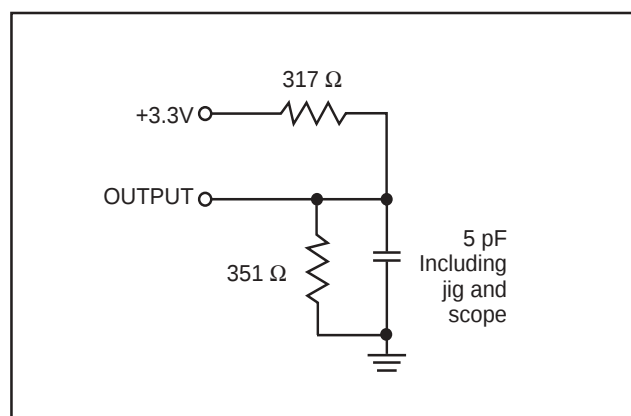


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

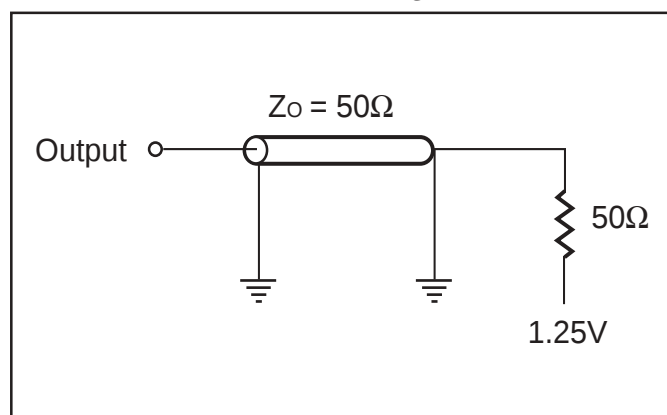


Figure 3

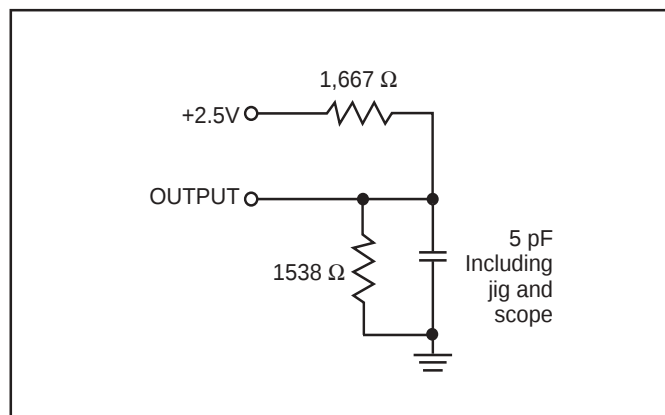


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	8.5		Unit
		Min.	Max.	
f _{MAX} ⁽³⁾	Clock Frequency	—	90	MHz
t _{KC} ⁽³⁾	Cycle Time	11	—	ns
t _{KH}	Clock High Time	4.5	—	ns
t _{KL} ⁽³⁾	Clock Low Time	4.5	—	ns
t _{KQ} ⁽³⁾	Clock Access Time	—	8.5	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	2	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	2	3.5	ns
t _{OEQ} ⁽³⁾	Output Enable to Output Valid	—	4.0	ns
t _{OEQX} ⁽¹⁾	Output Enable to Output Invalid	2	—	ns
t _{ELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	ns
t _{EHZ} ^(1,2)	Output Disable to Output High-Z	—	5.0	ns
t _{AS} ⁽³⁾	Address Setup Time	2	—	ns
t _{SS} ⁽³⁾	Address Status Setup Time	2	—	ns
t _{WS} ⁽³⁾	Write Setup Time	2	—	ns
t _{CES} ⁽³⁾	Chip Enable Setup Time	2	—	ns
t _{AVS} ⁽³⁾	Address Advance Setup Time	2	—	ns
t _{AH} ⁽³⁾	Address Hold Time	1	—	ns
t _{SH} ⁽³⁾	Address Status Hold Time	0.5	—	ns
t _{WH} ⁽³⁾	Write Hold Time	0.5	—	ns
t _{CEH} ⁽³⁾	Chip Enable Hold Time	0.5	—	ns
t _{AVH} ⁽³⁾	Address Advance Hold Time	0.5	—	ns

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

The timing diagram illustrates the relationship between various control signals and data flow over time. The signals shown are:

- CLK**: Clock signal with period t_{KC} .
- $\overline{ADSP}$** : Address Strobe, Pulse Width t_{AS} , Setup t_{SH} , Hold t_{KH} , and Delay t_{KL} . It is blocked by $\overline{CE}$ inactive.
- $\overline{ADSC}$** : Address Strobe, Pulse Width t_{AS} , Setup t_{SH} .
- $\overline{ADV}$** : Address Valid, Pulse Width t_{AV} .
- Address**: Shows three read operations (RD1, RD2, RD3) and one write operation (WR1). Setup t_{AS} , Hold t_{AH} , and Delay t_{AD} are indicated.
- $\overline{GW}$** : Global Write, Pulse Width t_{WS} , Setup t_{WH} .
- $\overline{BWE}$** : Bank Write Enable, Pulse Width t_{WS} , Setup t_{WH} .
- $\overline{BWD-BWA}$** : Bank Write Data, Pulse Width t_{WS} , Setup t_{WH} .
- $\overline{CE}$** : Chip Enable, Setup t_{CES} , Hold t_{CEH} . It masks $\overline{ADSP}$.
- $\overline{CE2}$** : Chip Enable 2, Setup t_{CES} , Hold t_{CEH} . It is only sampled with $\overline{ADSP}$ or $\overline{ADSC}$.
- $\overline{CE2}$** : Chip Enable 2, Setup t_{CES} , Hold t_{CEH} . It is unselected with $\overline{CE2}$.
- $\overline{OE}$** : Output Enable, Setup t_{OEHZ} .
- DATAOUT**: Data Output, High-Z, Setup t_{KQLZ} , Delay t_{KQ} , and various output delays (t_{OEQX} , t_{KQX} , t_{KQHZ}).
- DATAin**: Data Input, High-Z, Setup t_{DS} , Hold t_{DH} .

The diagram is divided into four main sections: Single Read Flow-through, Single Write, Burst Read, and Unselected.

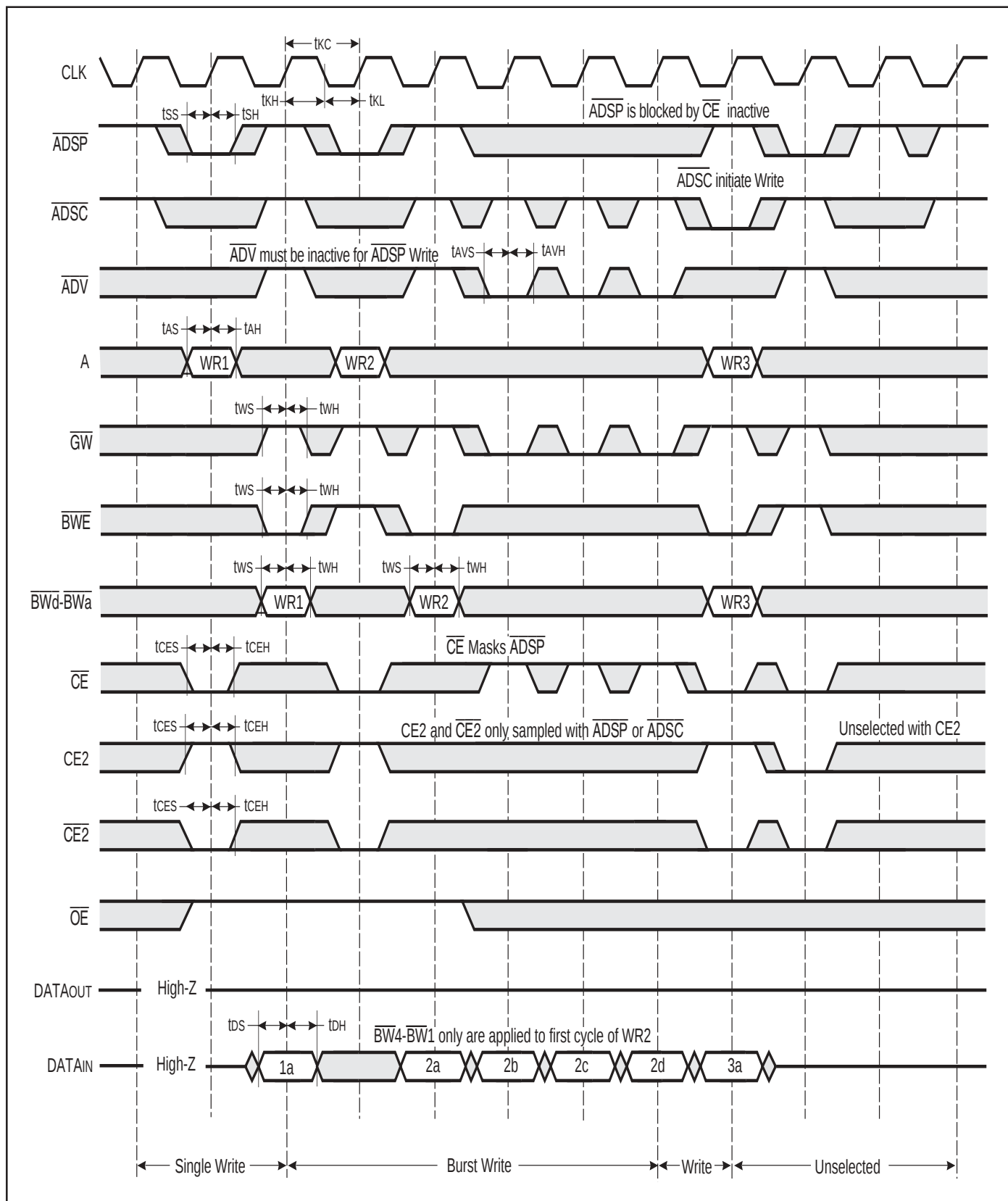
WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	8.5		Unit
		Min.	Max.	
$t_{KC}^{(1)}$	Cycle Time	11	—	ns
$t_{KH}^{(1)}$	Clock High Time	4.5	—	ns
$t_{KL}^{(1)}$	Clock Low Time	4.5	—	ns
$t_{AS}^{(1)}$	Address Setup Time	2	—	ns
$t_{SS}^{(1)}$	Address Status Setup Time	2	—	ns
$t_{WS}^{(1)}$	Write Setup Time	2	—	ns
$t_{DS}^{(1)}$	Data In Setup Time	3	—	ns
$t_{CES}^{(1)}$	Chip Enable Setup Time	2	—	ns
$t_{AVS}^{(1)}$	Address Advance Setup Time	2	—	ns
$t_{AH}^{(1)}$	Address Hold Time	1	—	ns
$t_{SH}^{(1)}$	Address Status Hold Time	0.5	—	ns
$t_{DH}^{(1)}$	Data In Hold Time	1	—	ns
$t_{WH}^{(1)}$	Write Hold Time	0.5	—	ns
$t_{CEH}^{(1)}$	Chip Enable Hold Time	0.5	—	ns
$t_{AVH}^{(1)}$	Address Advance Hold Time	0.5	—	ns

Notes:

1. Tested with load in Figure 1.

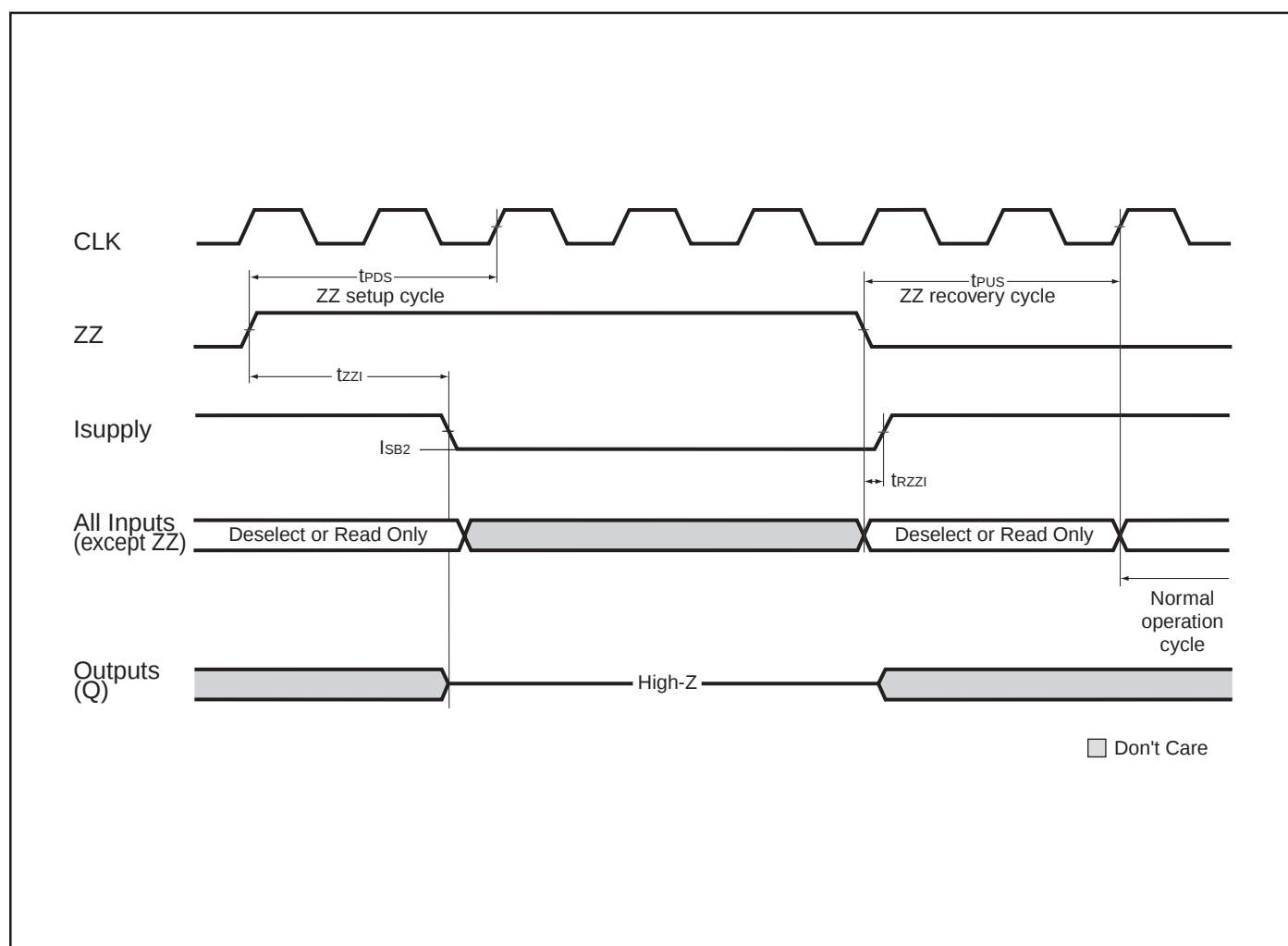
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	$ZZ \geq V_{ih}$	—	35	mA
t_{PDS}	ZZ active to input ignored		—	2	cycle
t_{PUS}	ZZ inactive to input sampled		2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current		—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current		0	—	ns

SNOOZE MODE TIMING



ORDERING INFORMATION

3.3V I/O OR 2.5V I/O

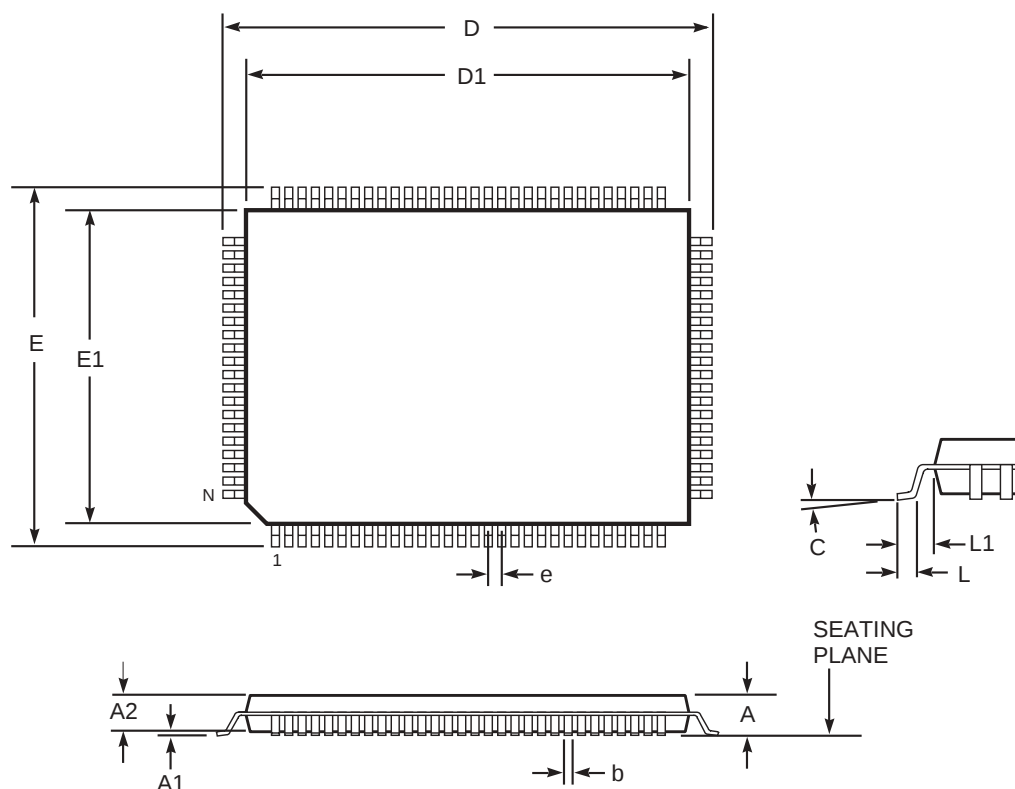
Industrial Range: -40°C TO +85°C

Speed (ns)	Order Part No.	Package
8.5	IS61LF6432A-8.5TQI	TQFP
	IS61LF6432A-8.5TQLI	TQFP, Lead-free
8.5	IS61LF6436A-8.5TQI	TQFP
	IS61LF6436A-8.5TQLI	TQFP, Lead-free

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



Thin Quad Flat Pack (TQ)									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
Ref. Std.									
No. Leads (N)	100					128			
A	—	1.60	—	0.063		—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006		0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057		1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015		0.17	0.27	0.007	0.011
D	21.90	22.10	0.862	0.870		21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791		19.90	20.10	0.783	0.791
E	15.90	16.10	0.626	0.634		15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555		13.90	14.10	0.547	0.555
e	0.65 BSC		0.026 BSC			0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030		0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.			1.00 REF.		0.039 REF.	
C	0°	7°	0°	7°		0°	7°	0°	7°

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.