Single Micropower, Chopper Stabilized, RRIO Operational Amplifier

ISL28133

The ISL28133 is a single micropower, chopper stabilized operational amplifier that is optimized for single supply operation from 1.65V to 5.5V. Its low supply current of 18µA and wide input range enable the ISL28133 to be an excellent general purpose op amp for a range of applications. The ISL28133 is ideal for handheld devices that operates off 2 AA or single Li-ion batteries.

The ISL28133 is available in the 5 Ld SOT-23, the 5 Ld SC70 and the 6 Ld 1.6mmx1.6mm µTDFN packages. All devices operates over the extended temperature range of -40°C to +125°C.

Features

- Low Input Offset Voltage . . . . 8µV, Max.
- Low Offset TC . . . . 0.075µV/°C, Max
- Input Bias Current . . . . 300pA, Max.
- Quiescent Current . . . . .18µA, Typ.
- Wide Supply Range. . . . . 1.65V to 5.5V
- Low Noise (0.01Hz to 10Hz) . . . . . . .1.1µV_{P-P}, Typ.
- Rail-to-Rail Inputs and Output
- Operating Temperature Range . . -40°C to +125°C

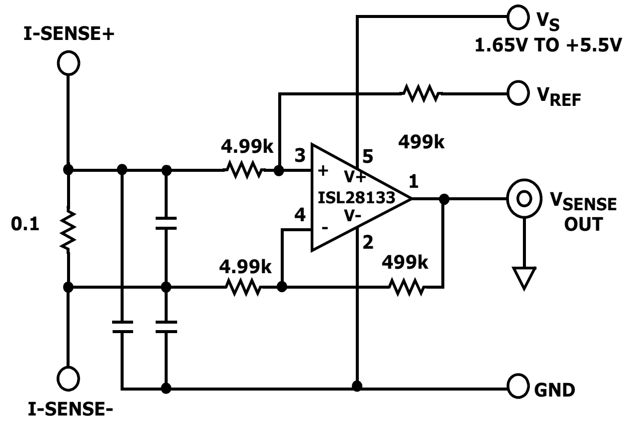
Applications* (see page 17)

- Bidirectional Current Sense
- Temperature Measurement
- Medical Equipment
- Electronic Weigh Scales

Related Literature

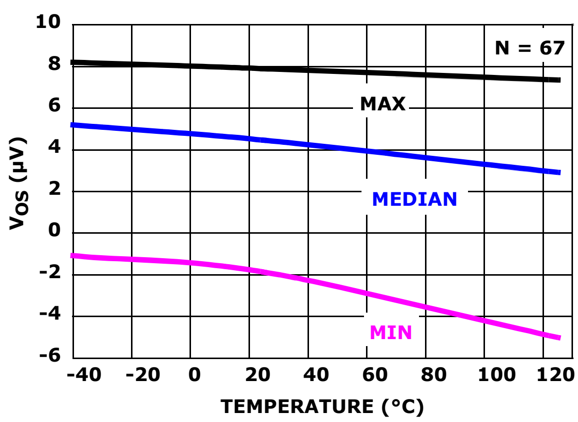
- AN1480 "ISL28133ISENS-EV1Z Evaluation Board Users Guide"
- AN1499 "ISL28133EVAL1Z High Gain Evaluation Board User's Guide"

Typical Application

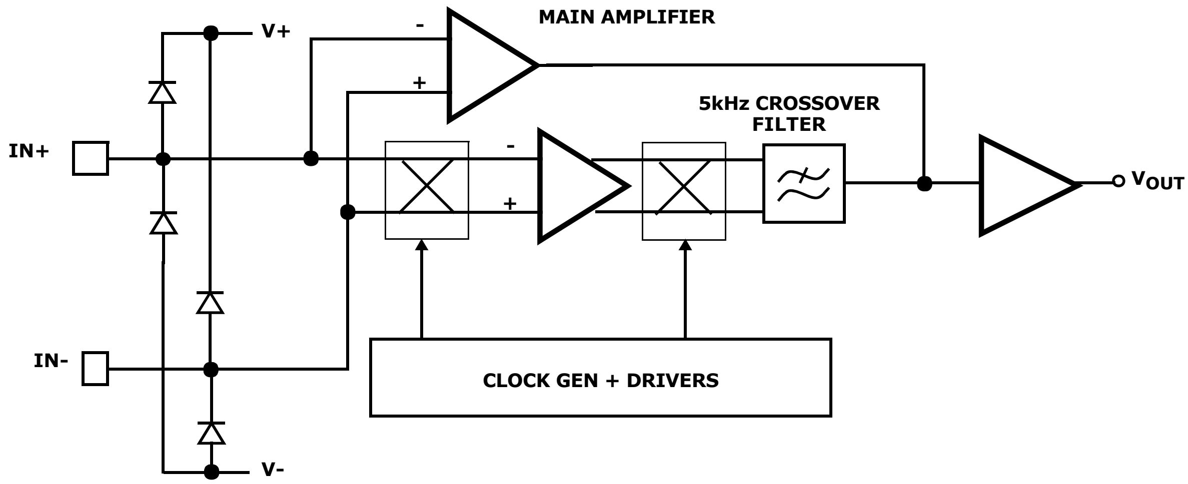


BIDIRECTIONAL CURRENT SENSE AMPLIFIER

V_{OS} vs Temperature



Block Diagram



Ordering Information

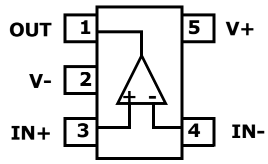
PART NUMBER	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28133FHZ-T7 (Notes 1, 2)	BCFA	5 Ld SOT-23	MDP0038
ISL28133FEZ-T7 (Notes 1, 2)	BHA	5 Ld SC70	P5.049
ISL28133FRUZ-T7 (Notes 1, 3)	T8	6 Ld µTDFN	L6.1.6x1.6
ISL28133ISENS-EV1Z	Evaluation Board		
ISL28133EVAL1Z	Evaluation Board		

NOTES:

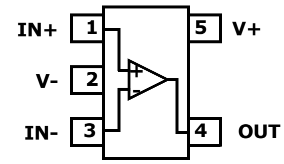
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL28133. For more information on MSL please see techbrief TB363.

Pin Configuration

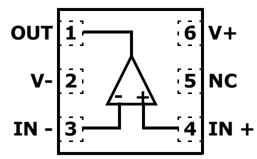
ISL28133
(5 LD SOT-23)
TOP VIEW



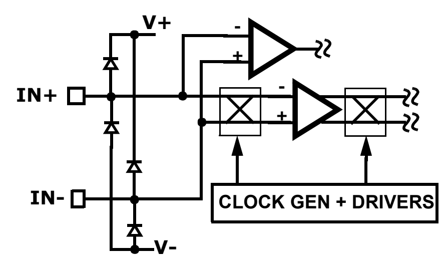
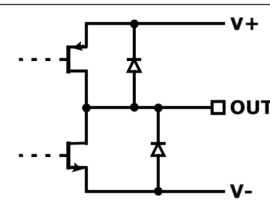
ISL28133
(5 LD SC-70)
TOP VIEW



ISL28133
(6 LD µTDFN)
TOP VIEW



Pin Descriptions

ISL28133 (5 Ld SOT23)	ISL28133 (5 Ld SC70)	ISL28133 (6 Ld µTDFN)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	1	4	IN+	Non-inverting input	 Circuit 1
2	2	2	V-	Negative supply	
4	3	3	IN-	Inverting input	(See Circuit 1)
1	4	1	OUT	Output	 Circuit 2
5	5	6	V+	Positive supply	
		5	NC	Not Connected – This pin is not electrically connected internally.	

Absolute Maximum Ratings

Max Supply Voltage V+ to V- 6.5V
Max Voltage VIN to GND . . . . -0.5V to 6.5V
Max Input Differential Voltage 6.5V
Max Input Current 20mA
Max Voltage VOUT to GND (10s) 6.5V
ESD Rating
  Human Body Model 3000V
  Machine Model 200V
  Charged Device Model 1500V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
5 Ld SOT-23 (Notes 5)	225
5 Ld SC70 (Notes 5)	206
6 Ld µTDFN (Notes 5)	240

Maximum Storage Temperature Range . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . -40°C to +125°C
Maximum Junction Temperature . . . . 140°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_+ = 5V, V_- = 0V, VCM = 2.5V, T_A = +25°C, R_L = Open, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-8	±2	8	µV
			-15.5		**15.5**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient			0.02	**0.075**	µV/°C
I_{OS}	Input Offset Current			-60		pA
I_B	Input Bias Current		-300	±30	300	pA
			-600		**600**	pA
Common Mode Input Voltage Range		V+ = 5.0V, V- = GND	-0.1		5.1	V
CMRR	Common Mode Rejection Ratio	VCM = -0.1V to 5.0V	118	125		dB
			115			dB
PSRR	Power Supply Rejection Ratio	Vs = 2V to 5.5V	110	138		dB
			110			dB
V_{OH}	Output Voltage Swing, High	R_L = 10kΩ	**4.965**	4.981		V
V_{OL}	Output Voltage Swing, Low	R_L = 10kΩ		18	**35**	mV
A_{OL}	Open Loop Gain	R_L = 1MΩ		174		dB
V_+	Supply Voltage	(Note 7)	1.65		5.5	V
I_S	Supply Current	R_L = OPEN		18	25	µA
					35	µA
I_{SC+}	Output Source Short Circuit Current	R_L = Short to ground or V+	13	17	26	mA
I_{SC-}	Output Sink Short Circuit Current		-26	-19	-13	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product f = 50kHz	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}		400		kHz
e_N V_{P-P}	Peak-to-Peak Input Noise Voltage	f = 0.01Hz to 10Hz		1.1		$µV_{P-P}$

Electrical Specifications V_+ = 5V, V_- = 0V, VCM = 2.5V, T_A = +25°C, R_L = Open, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
e_N	Input Noise Voltage Density	f = 1kHz		65		nV/√(Hz)
i_N	Input Noise Current Density	f = 1kHz		72		fA/√(Hz)
		f = 10Hz		79		fA/√(Hz)
C_{in}	Differential Input Capacitance	f = 1MHz		1.6		pF
	Common Mode Input Capacitance			1.12		pF
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V_{OUT} = 1V to 4V, R_L = 10kΩ		0.2		V/µs
	Negative Slew Rate			0.1		V/µs
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = 0.1V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		1.1		µs
	Fall Time, t_f 10% to 90%			1.1		µs
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = 2V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		8		µs
	Fall Time, t_f 10% to 90%			10		µs
t_s	Settling Time to 0.1%, 2V_{P-P} Step	A_V = +1, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		35		µs

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Parts are 100% tested with a minimum operating voltage of 1.65V to a VOS limit of ±15µV.

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open.

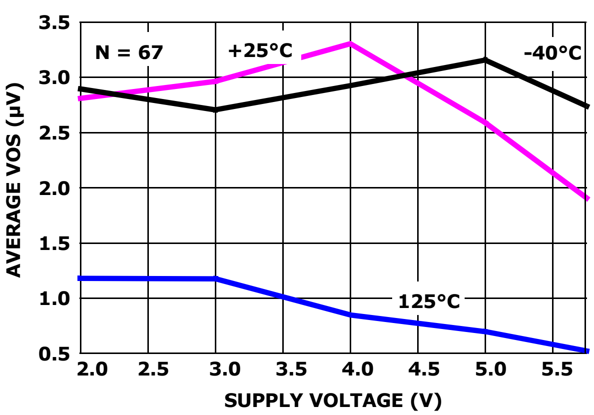


FIGURE 1. AVERAGE INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

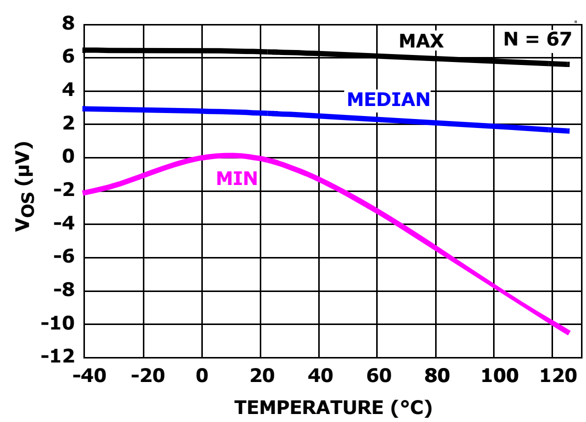


FIGURE 2. V_{OS} vs TEMPERATURE, V_S = ±1.0V, V_{IN} = 0V, R_L = INF

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

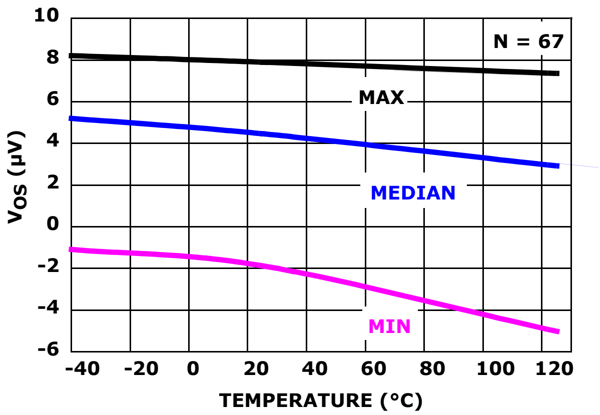


FIGURE 3. V_{OS} vs TEMPERATURE, V_S = ±2.5V, V_{IN} = 0V, R_L = INF

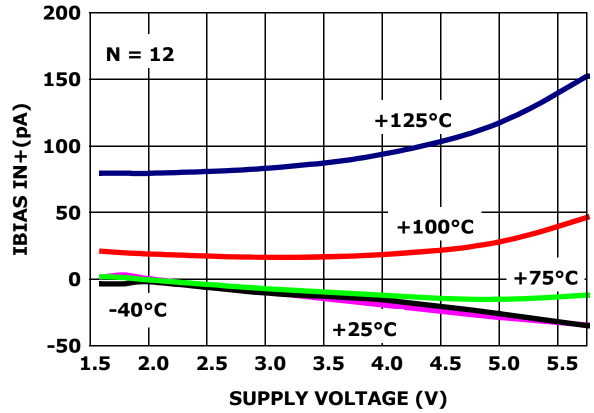


FIGURE 4. I_B+ vs SUPPLY VOLTAGE vs TEMPERATURE

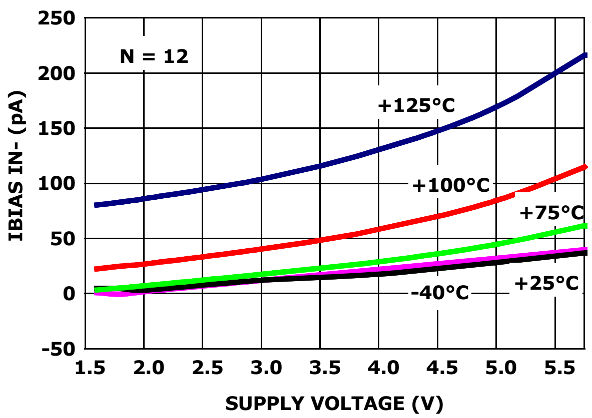


FIGURE 5. I_B- vs SUPPLY VOLTAGE vs TEMPERATURE

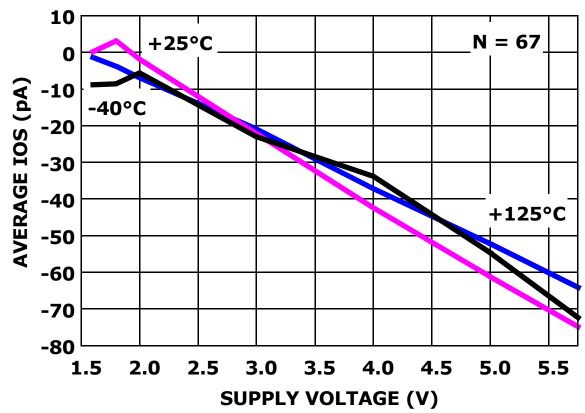


FIGURE 6. IOS vs SUPPLY VOLTAGE vs TEMPERATURE

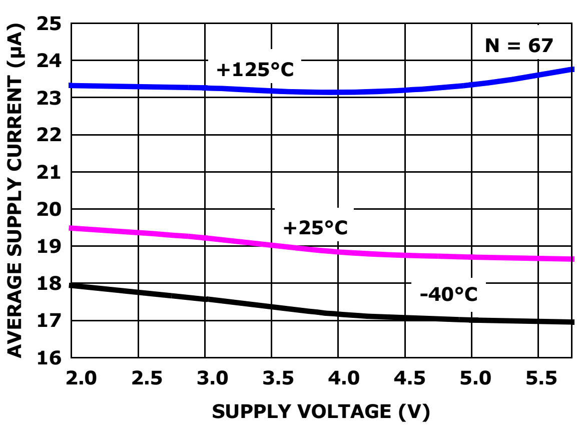


FIGURE 7. AVERAGE SUPPLY CURRENT vs SUPPLY VOLTAGE

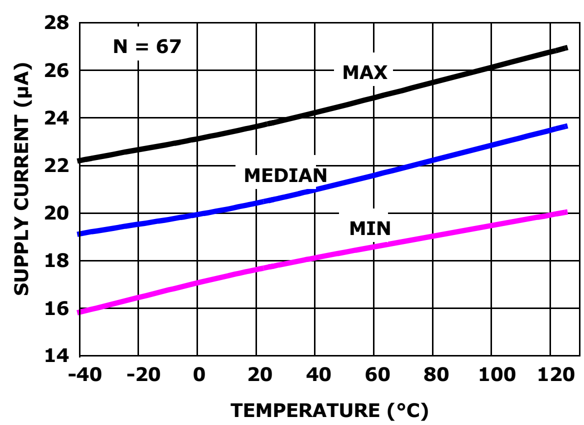


FIGURE 8. MIN/MAX SUPPLY CURRENT vs TEMPERATURE, V_S = ±0.8V, V_{IN} = 0V, R_L = INF

Typical Performance Curves
V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

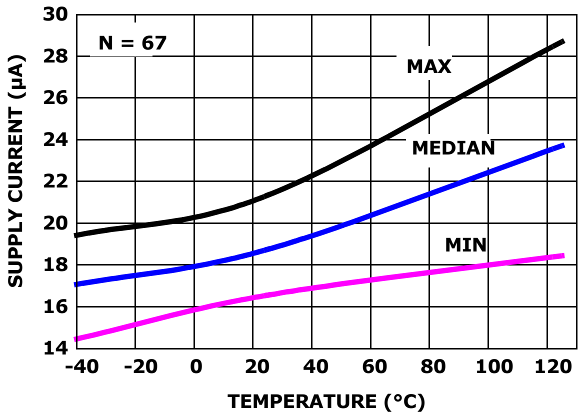


FIGURE 9. MIN/MAX SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V, V_{IN} = 0V, R_L = INF

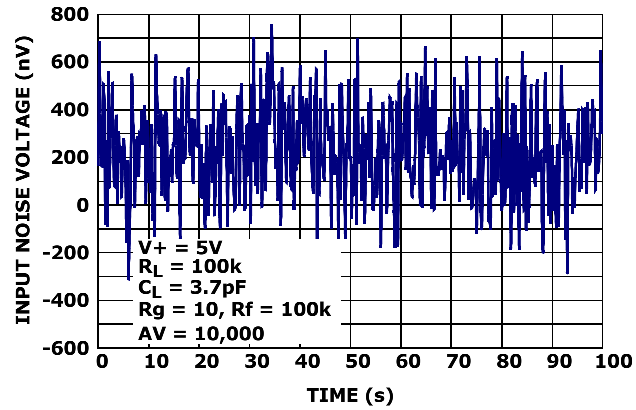


FIGURE 10. INPUT NOISE VOLTAGE 0.01Hz TO 10Hz

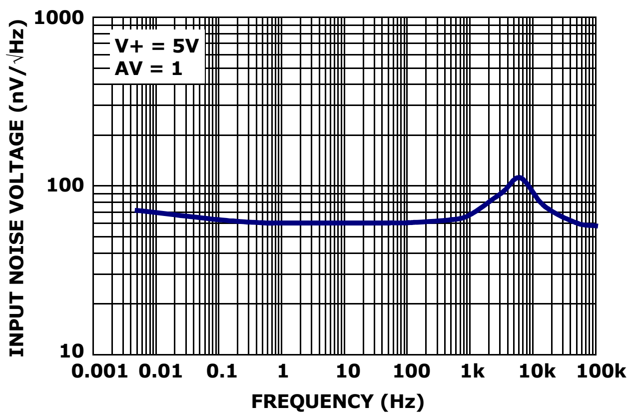


FIGURE 11. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

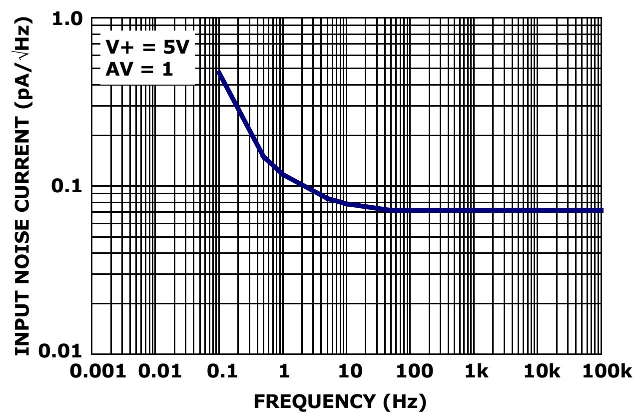


FIGURE 12. INPUT NOISE CURRENT DENSITY vs FREQUENCY

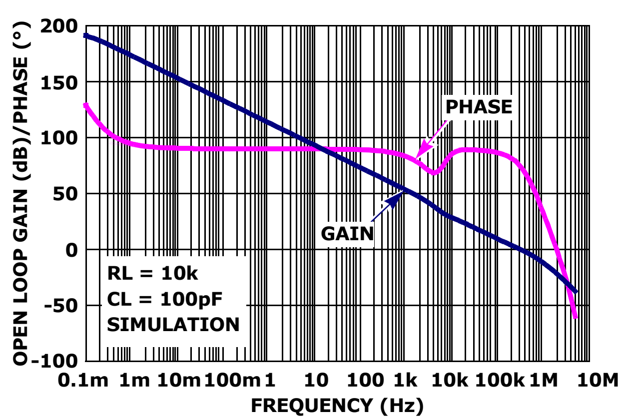


FIGURE 13. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10k

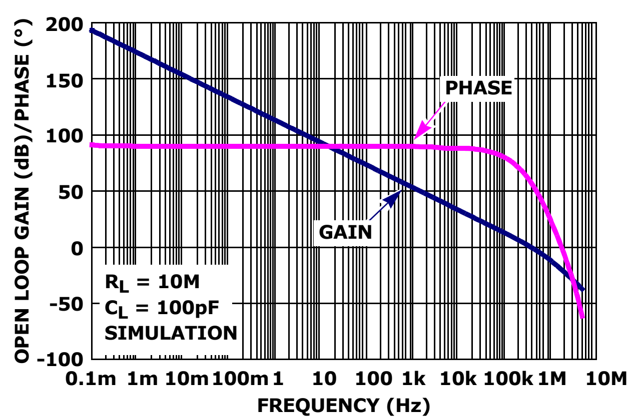


FIGURE 14. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10M

Typical Performance Curves V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. (Continued)

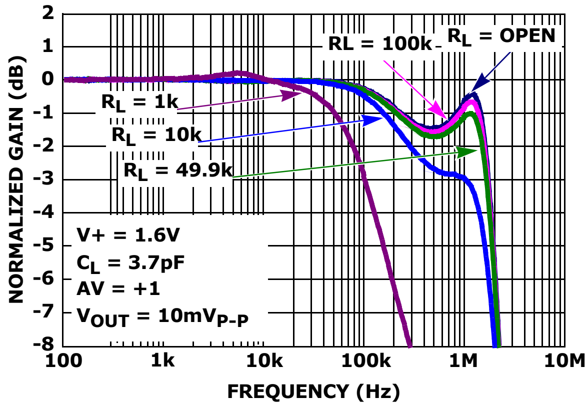


FIGURE 15. GAIN vs FREQUENCY vs R_L, V_S = 1.6V

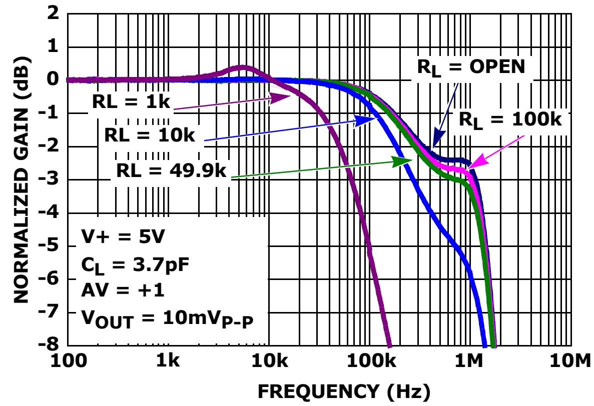


FIGURE 16. GAIN vs FREQUENCY vs R_L, V_S = 5V

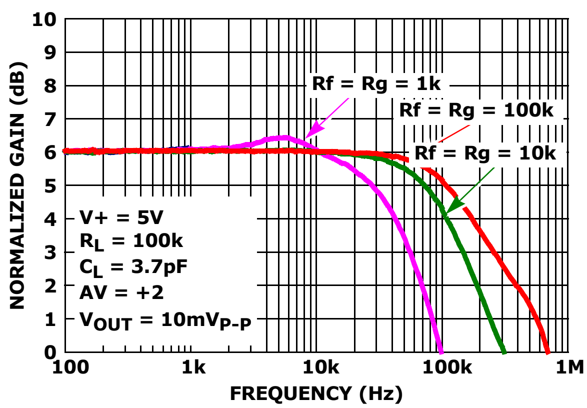


FIGURE 17. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

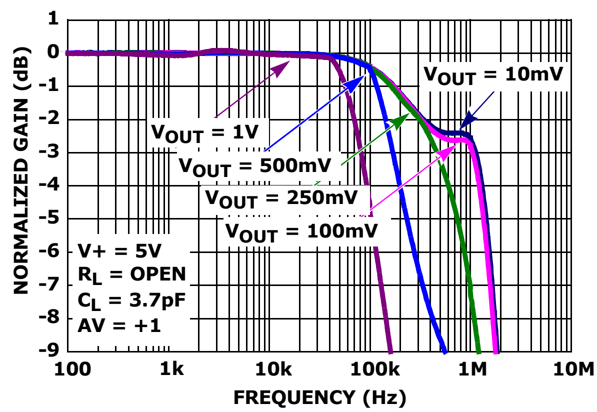


FIGURE 18. GAIN vs FREQUENCY vs V_{OUT}, R_L = OPEN

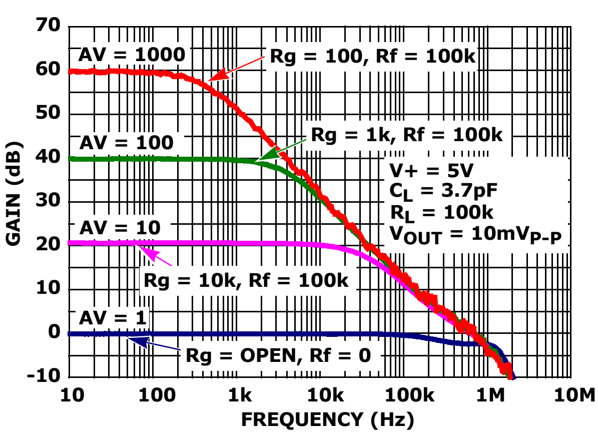


FIGURE 19. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

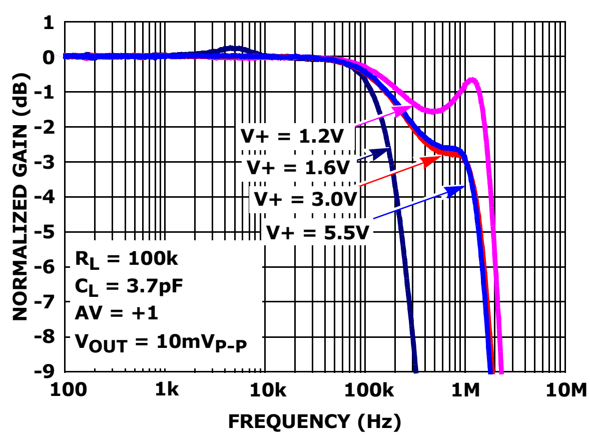


FIGURE 20. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. (Continued)

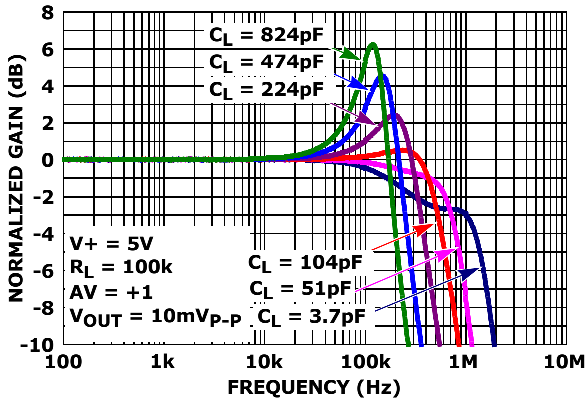


FIGURE 21. GAIN vs FREQUENCY vs C_L

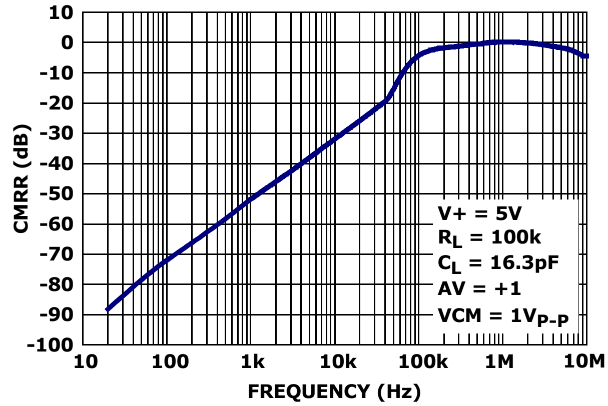


FIGURE 22. CMRR vs FREQUENCY, V_S = 5V

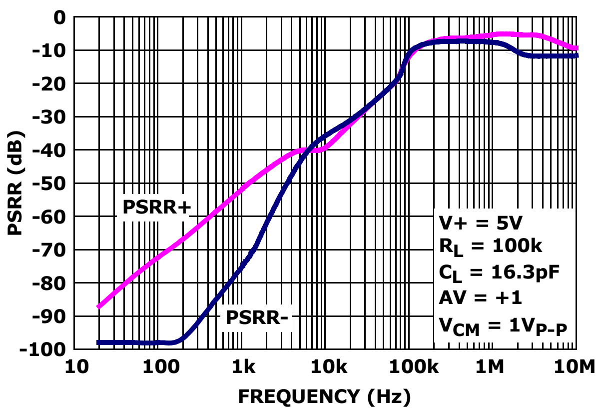


FIGURE 23. PSRR vs FREQUENCY, V_S = 5V

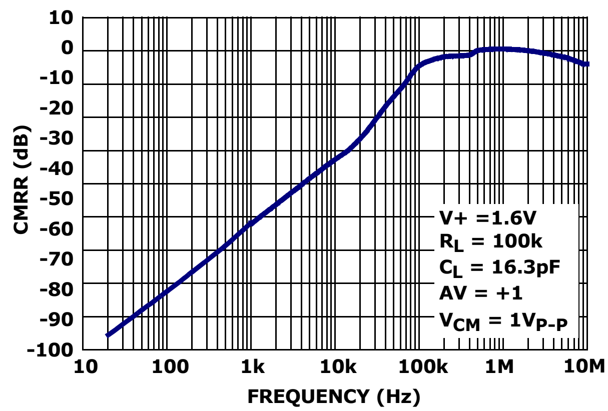


FIGURE 24. CMRR vs FREQUENCY, V_S = 1.6V

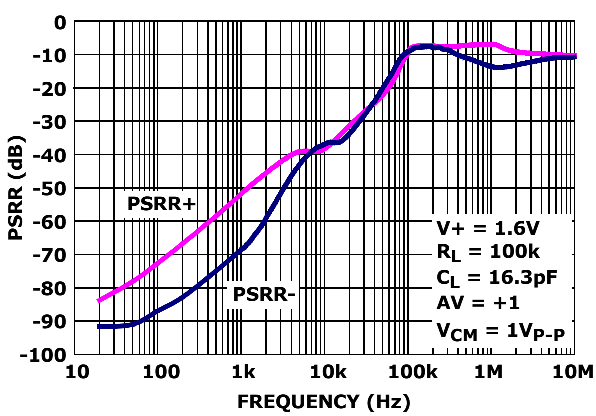


FIGURE 25. PSRR vs FREQUENCY, V_S = 1.6V

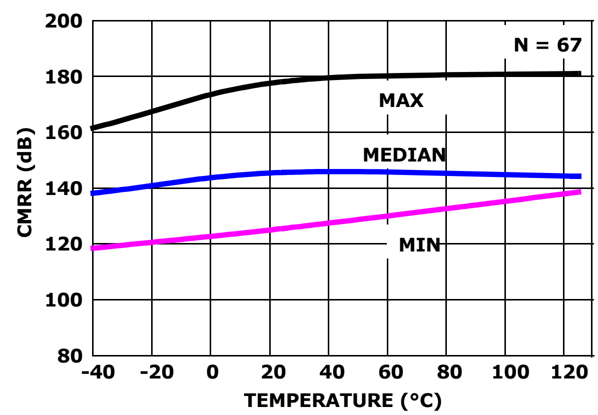


FIGURE 26. CMRR vs TEMPERATURE, VCM = -2.5V TO +2.5V, V+ = ±2.5V

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

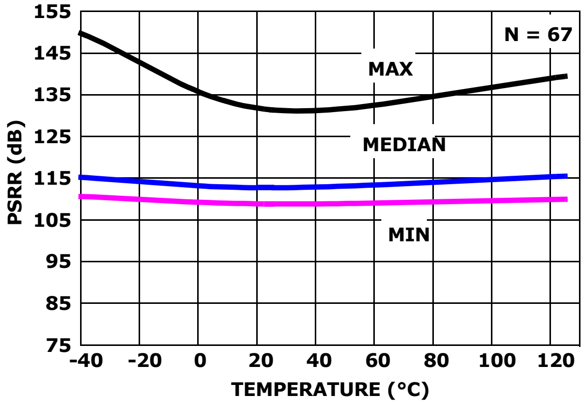


FIGURE 27. PSRR vs TEMPERATURE, V+ = 2V TO 5.5V

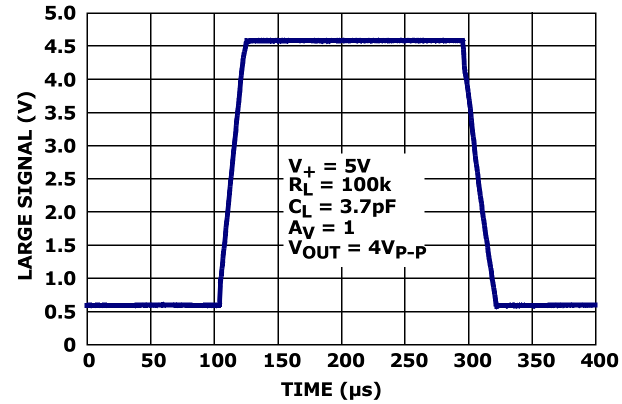


FIGURE 28. LARGE SIGNAL STEP RESPONSE (4V)

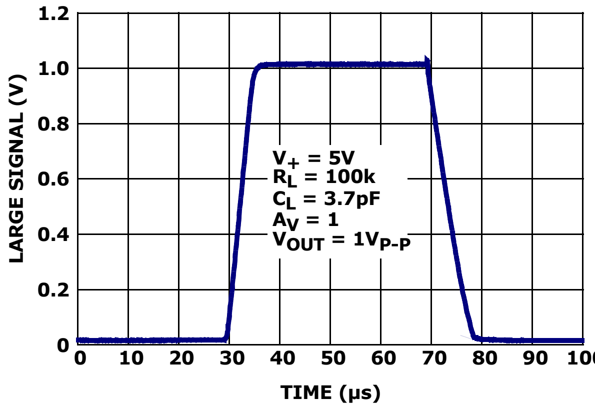


FIGURE 29. LARGE SIGNAL STEP RESPONSE (1V)

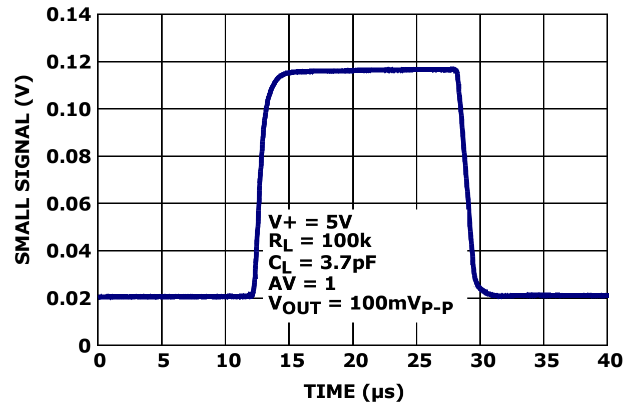


FIGURE 30. SMALL SIGNAL STEP RESPONSE (100mV)

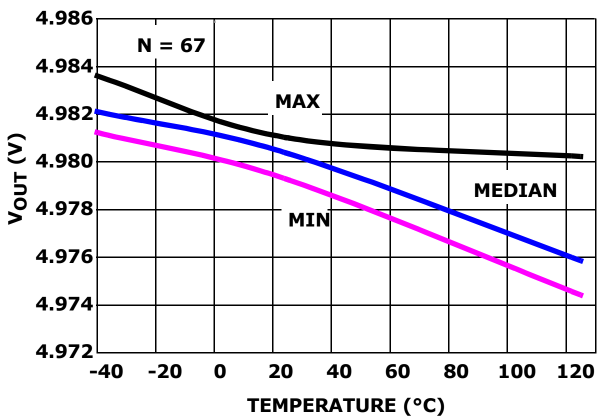


FIGURE 31. V_{OUT} HIGH vs TEMPERATURE, R_L = 10k, V_S +-2.5V

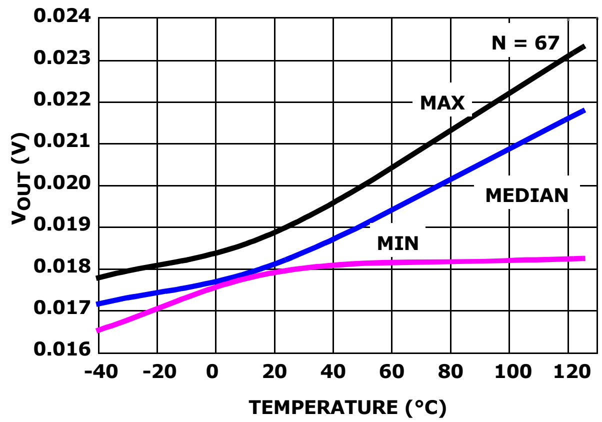


FIGURE 32. V_{OUT} LOW vs TEMPERATURE, R_L = 10k, V_S +-2.5V

Applications Information

Functional Description

The ISL28133 uses a proprietary chopper-stabilized architecture shown in the "Block Diagram" on page 2. The ISL28133 combines a 400kHz main amplifier with a very high open loop gain (174dB) chopper stabilized amplifier to achieve very low offset voltage and drift (2µV, 0.02µV/°C typical) while consuming only 18µA of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to ~5kHz, both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path leaving the main amplifier active out to the 400kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open loop gain, very low DC offset, and low 1/f noise. The noise is virtually flat across the frequency range from a few mHz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency (5kHz).

Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 17mA current limit and the capability to swing to within 20mV of either rail while driving a 10kΩ load.

IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications where either input is expected to exceed the rails by 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 33).

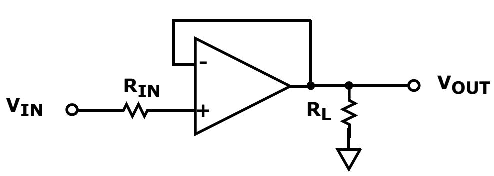


FIGURE 33. INPUT CURRENT LIMITING

Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28133 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 34 implements a single-stage, 10kV/V DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low VOS amplifier with high open loop gain. This circuit is practical down to 1.8V due to it's rail-to-rail input and output capability. Standard high gain DC amplifiers operating from low voltage supplies are not practical at these high gains using typical low offset precision op amps because the input offset voltage and temperature coefficient consume most of the available output voltage swing. For example, a typical precision amplifier in a gain of 10kV/V with a ±100µV VOS and a temperature coefficient of 0.5µV/°C would produce a DC error at the output of >1V with an additional 5mV°C of temperature dependent error. At 3V, this DC error consumes > 30% of the total supply voltage, making it impractical to measure sub-microvolt low frequency signals.

The ±8µV max V_{OS} and 0.075µV/°C of the ISL28133 produces a temperature stable maximum DC output error of only ±80mV with a maximum temperature drift of 0.75mV/°C. The additional benefit of a very low 1/f noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below 100nV to be easily detected with a simple single stage amplifier.

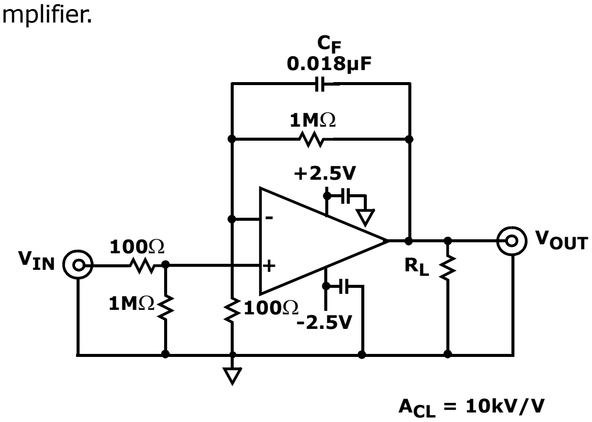


FIGURE 34. HIGH GAIN, PRECISION DC-COUPLED

ISL28133 SPICE Model

Figure 35 shows the SPICE model schematic and Figure 36 shows the net list for the ISL28133 SPICE model. The model is a simplified version of the actual device and simulates important parameters such as noise, **Slew Rate,** Gain and Phase. The model uses typical parameters from the ISL28133. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response. This enables the model to present an accurate AC representation of the actual device. The model is configured for ambient temperature of +25°C.

Figures 37 through 44 show the characterization vs simulation results for the Noise Density, Frequency Response vs Close Loop Gain, Gain vs Frequency vs CL and Large Signal Step Response (4V).

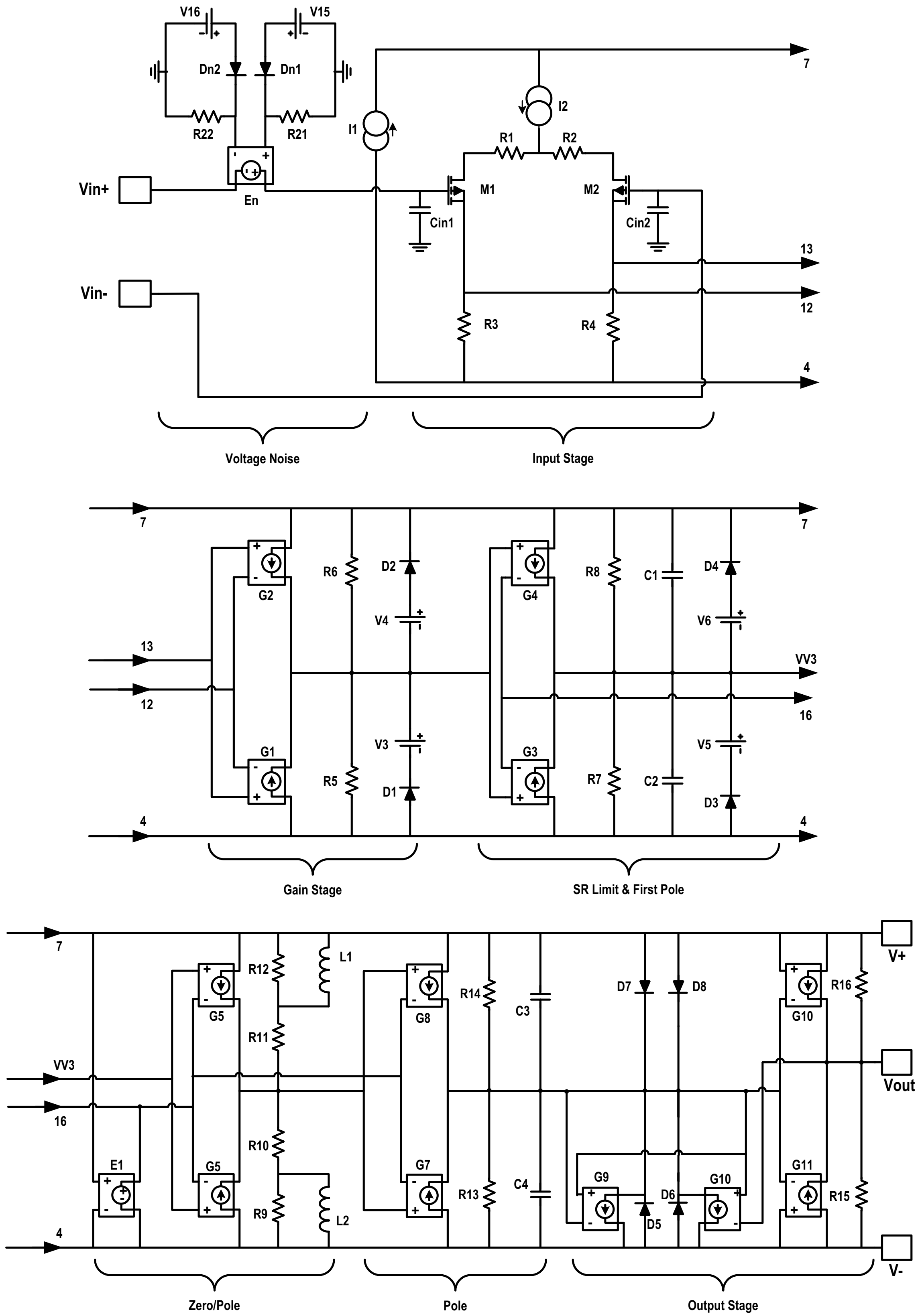


FIGURE 35. SPICE CIRCUIT SCHEMATIC

```
* ISL28133 Macromodel
* Revision B, April 2009
* AC characteristics, Voltage Noise
* Connections:        +input
*                      |    -input
*                      |     |    +Vsupply
*                      |     |     |    -Vsupply
*                      |     |     |     |    output
*                      |     |     |     |     |
.subckt ISL28133       3     2     7     4     6
*
*Voltage Noise
D_DN1      102 101 DN
D_DN2      104 103 DN
R_R21      0 101  120k
R_R22      0 103  120k
E_EN       8 3 101 103 1
V_V15      102 0 0.1Vdc
V_V16      104 0 0.1Vdc
*
*Input Stage
C_Cin1     8 0  0.4p
C_Cin2     2 0  2.0p
R_R1       9  10  10
R_R2       10 11  10
R_R3       4  12  100
R_R4       4  13  100
M_M1       12 8 9 9   pmosisil
+ L=50u
+ W=50u
M_M2       13 2 11 11 pmosisil
+ L=50u
+ W=50u
I_I1       4 7 DC 92uA
I_I2       7 10 DC 100uA
*
*Gain stage
G_G1       4 VV2 13 12 0.0002
G_G2       7 VV2 13 12 0.0002
R_R5       4 VV2  1.3Meg
R_R6       VV2 7  1.3Meg
D_D1       4 14 DX
D_D2       15 7 DX
V_V3       VV2 14 0.7Vdc
V_V4       15 VV2 0.7Vdc
*
*SR limit first pole
G_G3       4  VV3 VV2 16 1
G_G4       7  VV3 VV2 16 1
R_R7       4 VV3  1meg
R_R8       VV3 7  1meg
C_C1       VV3 7  12u
C_C2       4 VV3  12u
D_D3       4 17 DX
D_D4       18 7 DX
V_V5       VV3 17 0.7Vdc
V_V6       18 VV3 0.7Vdc
*
*Zero/Pole
E_E1       16 4 7 4 0.5
G_G5       4  VV4 VV3 16 0.000001
G_G6       7  VV4 VV3 16 0.000001
L_L1       20 7   0.3H
R_R12      20 7  2.5meg
R_R11      VV4 20  1meg
L_L2       4  19  0.3H
R_R9       4  19  2.5meg
R_R10      19 VV4  1meg
*Pole
G_G7       4 VV5 VV4 16 0.000001
G_G8       7 VV5 VV4 16 0.000001
C_C3       VV5 7  0.12p
C_C4       4 VV5  0.12p
R_R13      4 VV5  1meg
R_R14      VV5 7  1meg
*
*Output Stage
G_G9       21 4 6 VV5 0.0000125
G_G10      22 4 VV5 6 0.0000125
D_D5       4 21 DY
D_D6       4 22 DY
D_D7       7  21 DX
D_D8       7  22 DX
R_R15      4 6  8k
R_R16      6 7  8k
G_G11      6 4 VV5 4 -0.000125
G_G12      7 6 7 VV5 -0.000125
*
.model pmosisil pmos (kp=16e-3 vto=10m)
.model DN D(KF=6.4E-16 AF=1)
.MODEL DX D(IS=1E-18 Rs=1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28133
```

FIGURE 36. SPICE NET LIST

Characterization vs Simulation Results

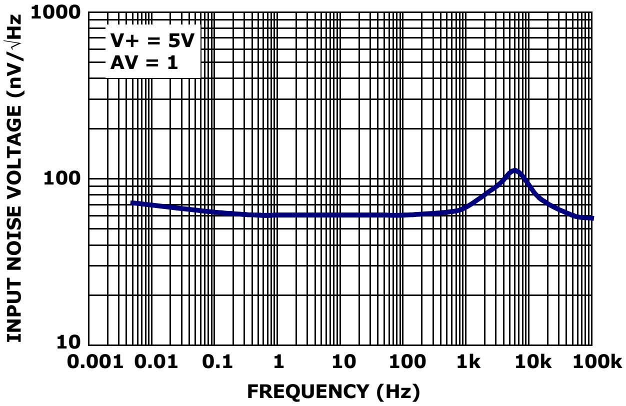


FIGURE 37. CHARACTERIZED INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

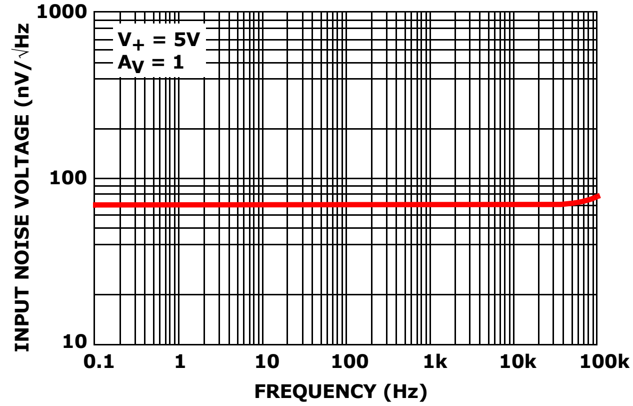


FIGURE 38. SIMULATED INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

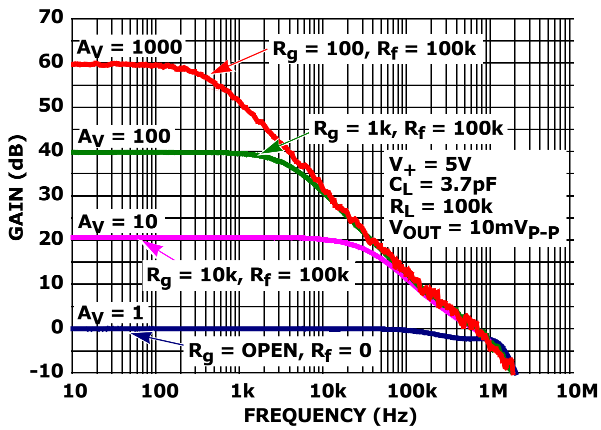


FIGURE 39. CHARACTERIZED FREQUENCY RESPONSE vs CLOSED LOOP GAIN

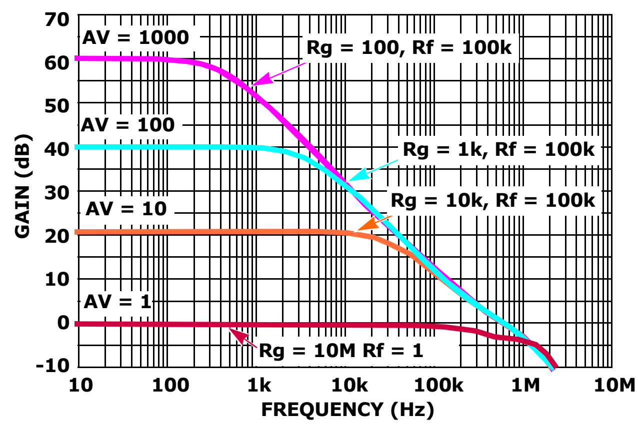


FIGURE 40. SIMULATED FREQUENCY RESPONSE vs CLOSED LOOP GAIN

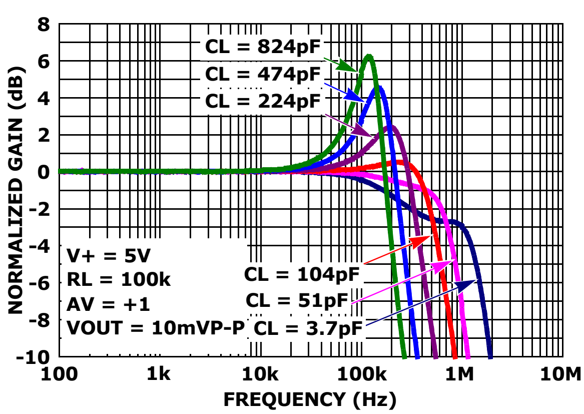


FIGURE 41. CHARACTERIZED GAIN vs FREQUENCY vs C_L

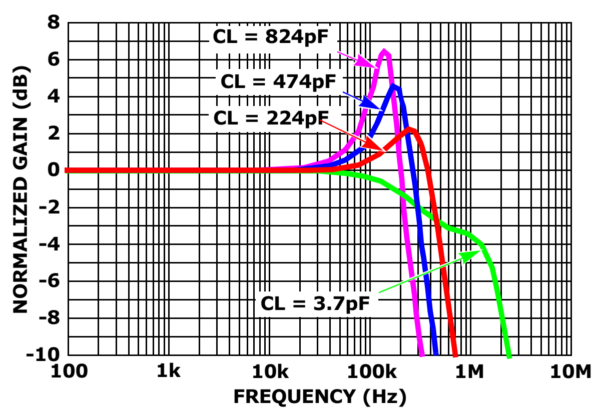


FIGURE 42. SIMULATED GAIN vs FREQUENCY vs C_L

Characterization vs Simulation Results (Continued)

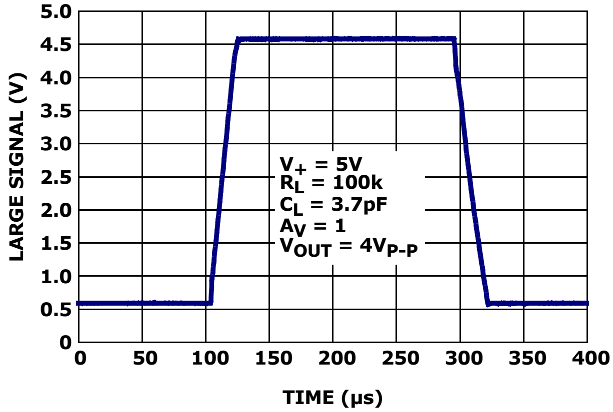


FIGURE 43. CHARACTERIZED LARGE SIGNAL STEP RESPONSE (4V)

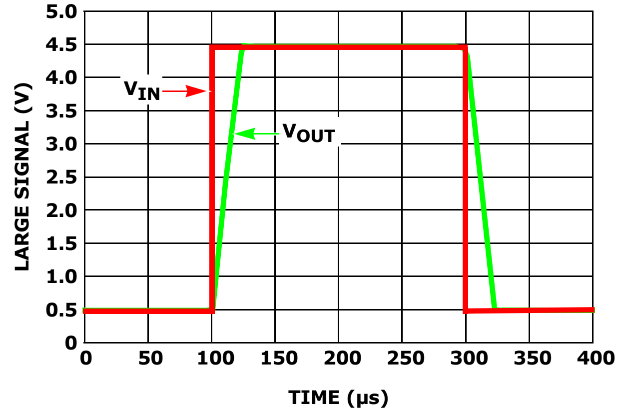


FIGURE 44. SIMULATED LARGE SIGNAL STEP RESPONSE (4V)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/3/10	FN6560.3	Title Page 1: Replaced "Zero-Drift" with "Chopper Stabilized" for title and part description On page 3: Pin Configuration: MTDFN -> uTDFN On page 7: Figure 10: Changed 0.1Hz to 0.01Hz in Figure caption On page 11: In "Functional Description"; Paragraph 1, 2nd sentence: Changed text from "…open loop gain (200dB)…" -to- "…open loop gain (174dB)…" Changed TYP for "Open Loop Gain" on page 4 from 200dB to 174dB. On page 11: In "High Gain, Precision DC-Coupled Amplifier"; Paragraph 2, 1st sentence: Changed text from "...DC output error of only ±80mV with a maximum temperature drift of 0.75µV/°C." to "… DC output error of only ±80mV with a maximum temperature drift of 0.75mV/C."
2/24/10		Removed "Coming Soon" from ISL28133EVAL1Z in the ordering information table on pg 2.
09/24/09	FN6560.2	Converted to new Intersil template. Removed ISL28233 and ISL28433 from data sheet, added Applications, Related Literature, Typical Application Circuit, Performance Curve, updated ordering information by removing "coming soon" on SC70 and uTDFN packages and adding Eval board listed as "coming soon". Added Block Diagram, Changed in Abs Max Rating Voltage from "5.75V" to "6.5V". Removed Tjc from Thermal Information until provided by packaging scheduled for 9-11-09. Changed Low Offset "drift" to Low Offset "TC", added Max Junction Temp 140C, added SPICE model and simulation results, removed supply current graph at +-3V, re-ordered typical performance curves, removed guard ring information from application section. Added Revision History and Products Information
05/29/09	FN6560.1	Page 4: Removed the RL = 100 Curve from Figures 3, 4 and 5. Page 1: Under Features, removed the word "Output" from "Low Output Noise"
03/25/09	FN6560.0	Initial Release to WEB

Products

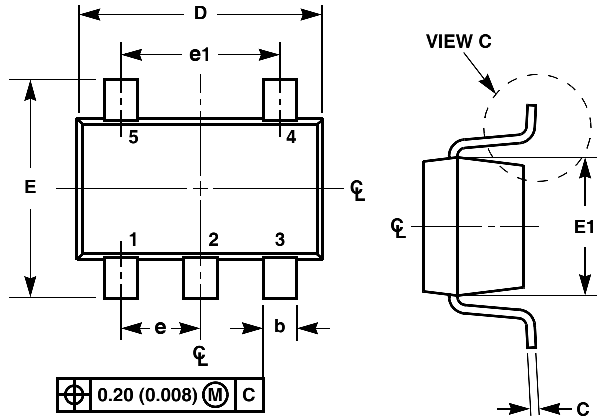
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

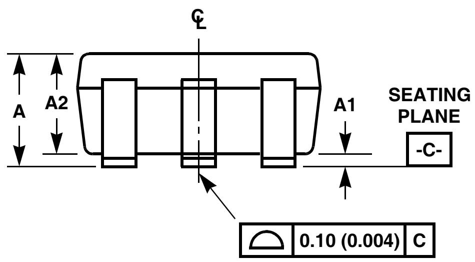
*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28133

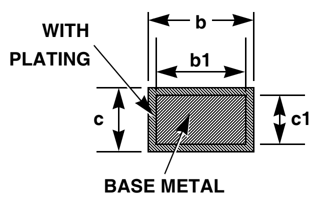
To report errors or suggestions for this data sheet, please go to www.intersil.com/askourstaff

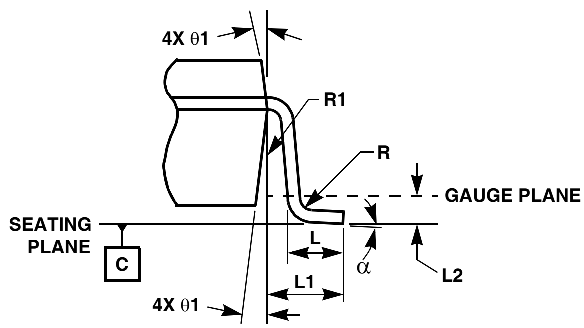
FITs are available from our website at http://rel.intersil.com/reports/search.php

Small Outline Transistor Plastic Packages (SC70-5)

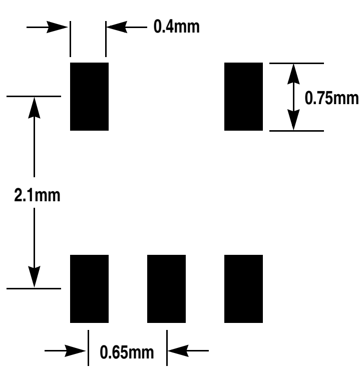








VIEW C



TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^{o}	8^{o}	0^{o}	8^{o}	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 3 7/07

NOTES:

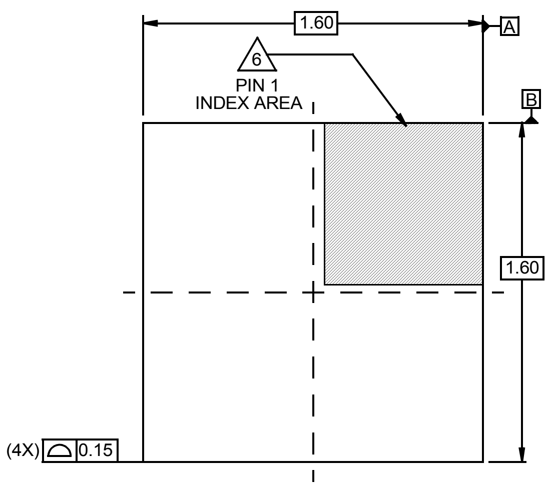
1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Package Outline Drawing

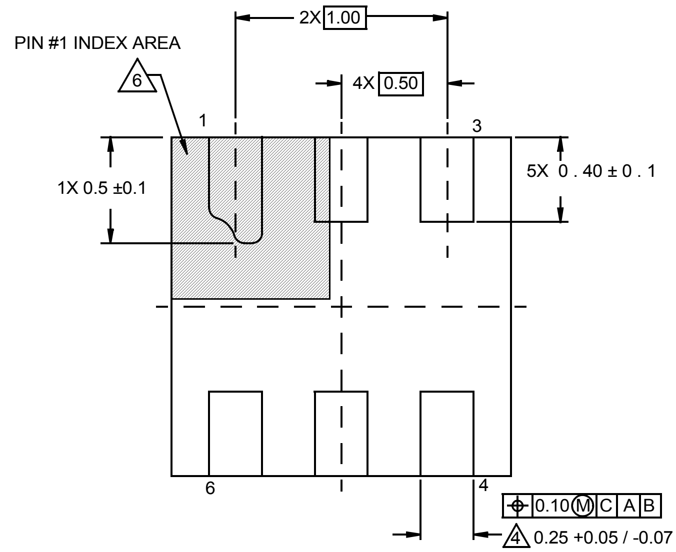
L6.1.6x1.6

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD COL PLASTIC PACKAGE (UTDFN COL)

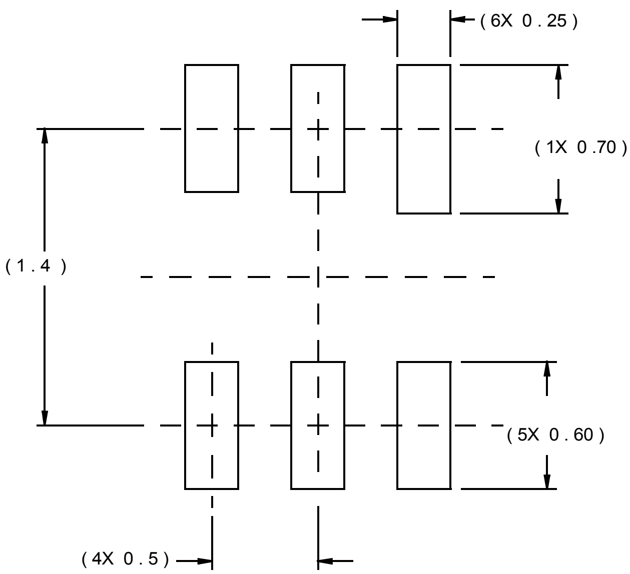
Rev 1, 11/07



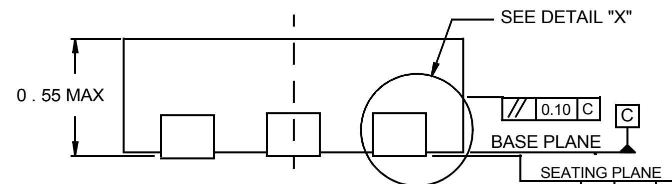
TOP VIEW



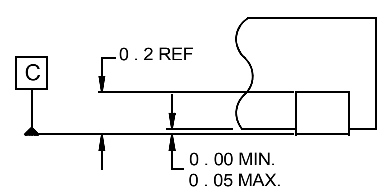
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

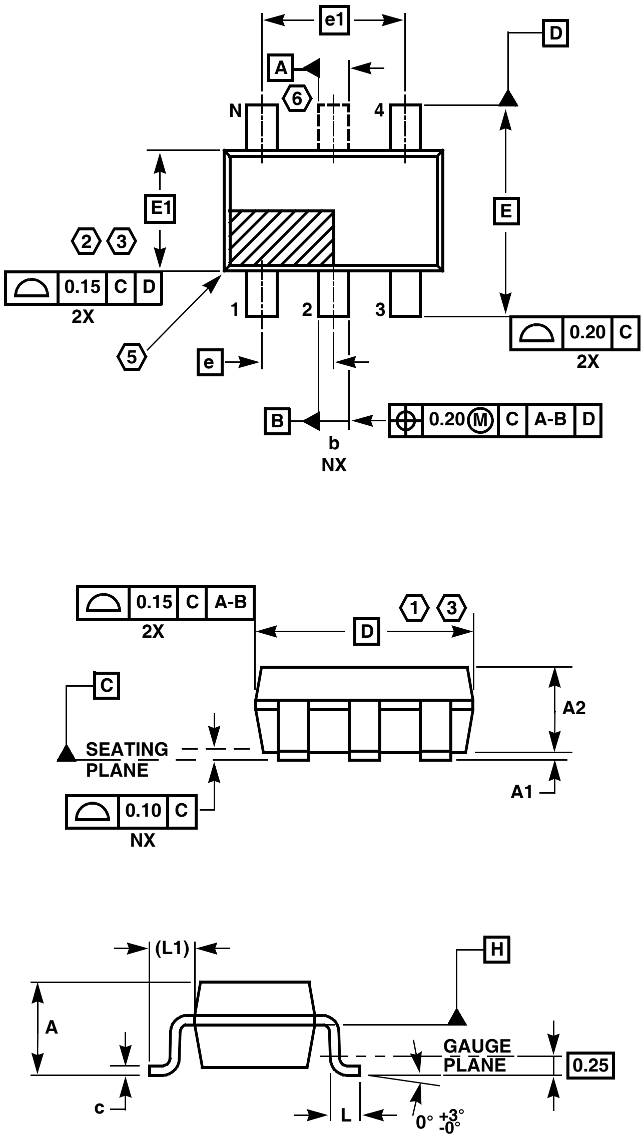


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

SOT-23 Package Family



MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).