Data Sheet | December 20, 2007 | FN6627.0

MP3/USB 2.0 High Speed Switch with Negative Signal Handling and Low Power Shutdown

The Intersil ISL54209 dual SPDT (Single Pole/Double Throw) switch combines low distortion audio and accurate USB 2.0 high speed data (480Mbps) signal switching in the same low voltage device. When operated with a 2.5V to 5.0V single supply, this analog switch allows audio signal swings below ground, allowing the use of a common USB and audio headphone connector in Personal Media Players and other portable battery powered devices.

The ISL54209 logic control pins are 1.8V compatible, which allows for control via a standard µcontroller. With a VDD voltage in the range of 2.5V to 3.6V, the IN pin voltage can exceed the VDD rail allowing the USB 5V V_{BUS} voltage from a computer to directly drive the IN pin to switch between the audio and USB signal sources in the portable device. The part has an audio enable control pin to open all the switches and put the part in a low power state.

The ISL54209 is available in a small 10 Ld 2.1mmx1.6mm ultra-thin µTQFN package and a 10 Ld 3mmx3mm TDFN package. It operates over a temperature range of -40°C to +85°C.

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

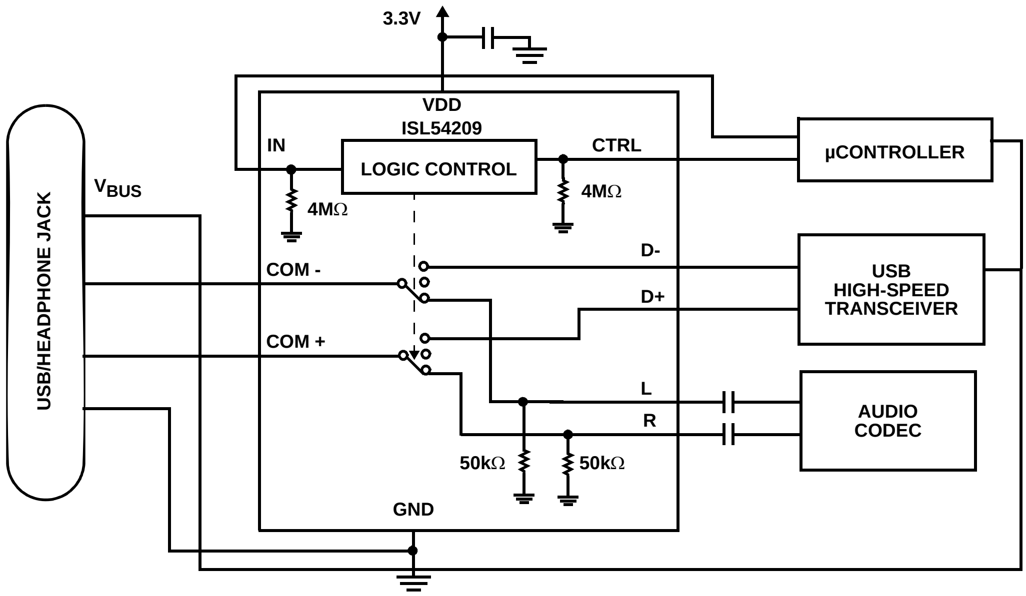
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Low Distortion Negative Signal Capability
- Low Power Shutdown State
- Low Distortion Headphone Audio Signals
  - THD+N at 20mW into 32Ω Load . . . . <0.07%
- Crosstalk (100kHz) . . . . -95dB
- OFF Isolation (100kHz) 95dB
- Single Supply Operation (V_{DD}) . . . . 2.5V to 5.0V
- -3dB Bandwidth USB Switch 736MHz
- Available in µTQFN and TDFN Packages
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components
- Pb-Free (RoHS Compliant)

Applications

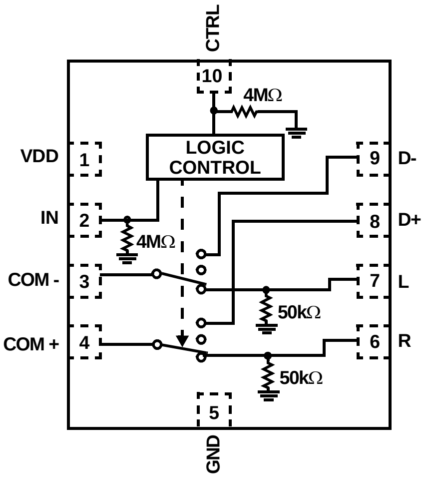
- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDAs
- Audio/USB Switching

Application Block Diagram

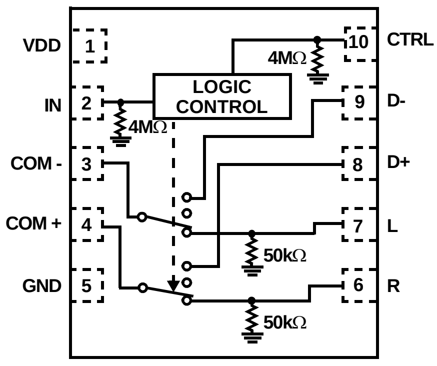


Pinouts (Note 1)

ISL54209
(10 Ld 2.1mmx1.6mm µTQFN)
TOP VIEW



ISL54209
(10Ld 3.0mmx3.0mm TDFN)
TOP VIEW



NOTE:

1. ISL54209 Switches Shown for IN = Logic “0” and CTRL = Logic “1”.

Truth Table

ISL54209			
IN	**CTRL**	**L, R**	**D+, D-**
0	0	OFF	OFF
0	1	ON	OFF
1	X	OFF	ON

IN, CTRL: Logic “0” when ≤ 0.5V or Floating, Logic “1” when ≥ 1.4V with 2.7V to 3.6V Supply.

Pin Descriptions

PIN NUMBER	NAME	FUNCTION
1	VDD	Power Supply
2	IN	Digital Control Input
3	COM-	Voice and Data Common Pin
4	COM+	Voice and Data Common Pin
5	GND	Ground Connection
6	R	Audio Right Input
7	L	Audio Left Input
8	D+	USB Differential Input
9	D-	USB Differential Input
10	CTRL	Digital Control Input (Audio Enable)

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL54209IRUZ-T (Notes 2, 3)	GF	-40 to +85	10 Ld µTQFN	L10.2.1x1.6A
ISL54209IRTZ-T (Notes 2, 3)	4209	-40 to +85	10 Ld TDFN	L10.3x3A
ISL54209IRTZ (Note 2)	4209	-40 to +85	10 Ld TDFN	L10.3x3A

NOTES:

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Please refer to TB347 for details on reel specifications.

Absolute Maximum Ratings

V_{DD} to GND . . . . -0.3V to 5.5V
Input Voltages
D+, D-, L, R (Note 4) . . . . - 2V to 5.5V
L, R (Note 4) . . . . - 2V to ((V_{DD}) + 0.3V)
IN (Note 4). . . . . -2V to 5.5V
CTRL (Note 4) . . . . -0.3V to ((V_{DD}) + 0.3V)
Output Voltages
COM-, COM+ (Note 4) . . . . -2V to 5.5V
Continuous Current (Audio Switches). . . . . ±150mA
Peak Current (Audio Switches)
(Pulsed 1ms, 10% Duty Cycle, Max). . . . . ±300mA
Continuous Current (USB Switches). . . . . ±40mA
Peak Current (USB Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . ±100mA
ESD Ratings
Human Body Model. . . . . >2kV
Machine Model . . . . >200V
Charged Device Model . . . .>1.5kV

Thermal Information

Thermal Resistance (Typical, Notes 5 and 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 2.1mmx1.6mm µTQFN Package	154	48.3
10 Ld 3mmx3mm TDFN	89	25

Maximum Junction Temperature (Plastic Package) . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Signals on D+, D-, L, R, COM-, COM+, CTRL and IN exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{INH} = V_{CTRLH} = 1.4V, V_{INL} = V_{CTRLL} = 0.5V, (Note 7), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 8, 9)	TYP	MAX (Notes 8, 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Audio Switches (L, R)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.3V, IN = 0.5V, CTRL = 1.4V	Full	-1.5	-	1.5	V
ON-Resistance, r_{ON}	V_{DD} = 5.0V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V (see Figure 3)	25	-	2.3	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 4.2V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V (see Figure 3)	25	-	2.35	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.85V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V (see Figure 3)	25	-	2.72	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V , I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V (see Figure 3, Note 11)	+25	-	2.5	2.8	Ω
		Full	-	-	3.4	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V , I_{COMx} = 40mA, V_L or V_R = Voltage at max r_{ON} over signal range of -0.85V to 0.85V (Notes 11 and 12)	+25	-	0.09	0.25	Ω
		Full	-	-	0.26	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V , I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V (Notes 10 and 11)	+25	-	0.02	0.05	Ω
		Full	-	-	0.07	Ω
Discharge Pull-Down Resistance, R_L, R_R	V_{DD} = 3.6V, IN = 0V, CTRL = 1.4V , V_{COM-} or V_{COM+} = -0.85V, 0.85V, V_L or V_R = -0.85V, 0.85V, V_{D+} and V_{D-} = floating; measure current through the discharge pull-down resistor and calculate resistance value.	+25	-	50	-	kΩ

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{INH} = V_{CTRLH} = 1.4V, V_{INL} = V_{CTRLL} = 0.5V, (Note 7), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 8, 9)	TYP	MAX (Notes 8, 9)	UNITS
USB Switches (D+, D-)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 2.7V to 3.6V, IN = 1.4V, CTRL = 1.4V	Full	0	-	V_{DD}	V
ON-Resistance, r_{ON}	V_{DD} = 5.0V, IN = V_{DD}, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 5V (see Figure 4)	+25	-	20	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 4.2V, IN = V_{DD}, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 4.2V (see Figure 4)	25	-	22	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.85V, IN = V_{DD}, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 2.85V (see Figure 4)	25	-	28	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 1mA, V_{D+} or V_{D-} = 3.3V (see Figure 4, Note 11)	25	-	25	30	Ω
		Full	-	-	35	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV (see Figure 4, Note 11)	25	-	5	6.5	Ω
		Full	-	-	7	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = Voltage at max r_{ON} (Notes 11 and 12)	25	-	0.05	0.25	Ω
		Full	-	-	0.55	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV (Notes 10 and 11)	25	-	0.45	0.55	Ω
		Full	-	-	1.0	Ω
OFF-Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V, V_{COM-} or V_{COM+} = 0.5V, 0V, V_{D+} or V_{D-} = 0V, 0.5V, V_L and V_R = float	25	-5	0.5	5	nA
		Full	-60	-	60	nA
ON-Leakage Current, I_{DX}	V_{DD} = 3.6V, IN = V_{DD}, CTRL = 0V or V_{DD}, V_{D+} or V_{D-} = 2.7V, V_{COM-} or V_{COM+} = Float, V_L and V_R = float	25	-10	2	10	nA
		Full	-70	-	70	nA
DYNAMIC CHARACTERISTICS						
USB Turn-ON Time, t_{ON}	V_{DD} = 3.0V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	52	-	ns
USB Turn-OFF Time, t_{OFF}	V_{DD} = 3.0V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	20	-	ns
Audio Turn-ON Time, t_{ON}	V_{DD} = 3.0V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	2.5	-	µs
Audio Turn-OFF Time, t_{OFF}	V_{DD} = 3.0V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	50	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.0V, R_L = 50Ω, C_L = 10pF (see Figure 2)	25	-	44	-	ns
Skew, t_{SKEW}	V_{DD} = 3.0V, IN = 3V, CTRL = 3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 720ps at 480Mbps, (Duty Cycle = 50%) (see Figure 7)	25	-	50	-	ps
Total Jitter, t_J	V_{DD} =3.0V, IN = 3V, CTRL = 3V, R_L = 50Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps	25	-	210	-	ps
Propagation Delay, t_{PD}	V_{DD} = 3.0V, IN = 3V, CTRL = 3V, R_L = 45Ω, C_L = 10pF (see Figure 7)	25	-	250	-	ps
Audio Crosstalk R to COM-, L to COM+	V_{DD} = 3.0V, IN = 0V, CTRL = 3.0V, R_L = 32Ω, f = 20Hz to 20kHz, V_R or V_L = 0.707V_{RMS} (2V_{P-P}) (see Figure 6)	25	-	-110	-	dB
Crosstalk (Audio to USB, USB to Audio)	V_{DD} = 3.0V, R_L = 50Ω, f = 100kHz (see Figure 6)	25	-	-95	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 100kHz	25	-	95	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 32Ω, f = 20Hz to 20kHz	25	-	114	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, IN = 0V, CTRL = 3.0V, V_L or V_R = 0.707V_{RMS} (2V_{P-P}), R_L = 32 Ω	25	-	0.06	-	%
USB Switch -3dB Bandwidth	Signal = 0dBm, 0.2V_{DC} offset, R_L = 50Ω, C_L = 5pF	25	-	736	-	MHz
D+/D- OFF-Capacitance, C_{DxOFF}	f = 1MHz, V_{DD} = 3.0V, IN = 0V, CTRL = 3.0V, V_{D-} or V_{D+} = V_{COMx} = 0V (see Figure 5)	25	-	3	-	pF

Electrical Specifications - 2.7V to 3.6V Supply

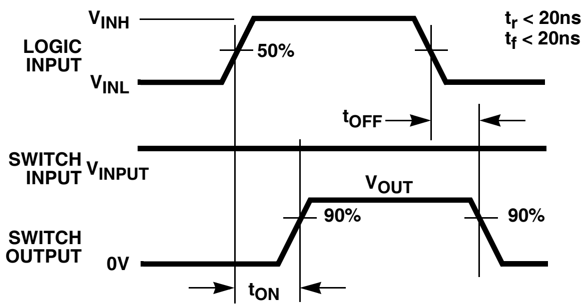
Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{INH} = V_{CTRLH} = 1.4V, V_{INL} = V_{CTRLL} = 0.5V, (Note 7), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 8, 9)	TYP	MAX (Notes 8, 9)	UNITS
L/R OFF-Capacitance, C_{LOFF}, C_{ROFF}	f = 1MHz, V_{DD} = 3.0V, IN = 3.0V, CTRL = 0V or 3V, V_L or V_R = V_{COMx} = 0V (see Figure 5)	25	-	5	-	pF
COM ON-Capacitance, $C_{COMx(ON)}$	f = 1MHz, V_{DD} = 3.0V, IN = 3.0V, CTRL = 0V or 3V, V_{D-} or V_{D+} = V_{COMx} = 0V (see Figure 5)	25	-	8	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	2.5		5.0	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, IN = 0V or 3.6V, CTRL = 3.6V	25	-	7	13	µA
		Full	-	-	15	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.6V, IN = 0V, CTRL = 0V or float	25	-	1	10	nA
		Full	-	-	150	nA
Power OFF-Current, I_{Dx} I_{COMx}	V_{DD} = 0V, V_{Dx} = V_{COMx} = 5.25V, IN = CTRL = Float	25	-	7	-	µA
DIGITAL INPUT CHARACTERISTICS						
Voltage Low, V_{INL}, V_{CTRLL}	V_{DD} = 2.7V to 3.6V	Full	-	-	0.5	V
Voltage High, V_{INH}, V_{CTRLH}	V_{DD} = 2.7V to 3.6V	Full	1.4	-	-	V
Input Current, I_{INL}, I_{CTRLL}	V_{DD} = 3.6V, IN = 0V, CTRL = 0V	Full	-50	20	50	nA
Input Current, I_{INH}	V_{DD} = 3.6V, IN = 3.6, CTRL = 0V	Full	-2	0.9	2	µA
Input Current, I_{CTRLH}	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V	Full	-2	0.9	2	µA
CTRL Pull-Down Resistor, R_{CTRL}	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V; measure current through the internal pull-down resistor and calculate resistance value.	Full	-	4	-	MΩ
IN Pull-Down Resistor, R_{IN}	V_{DD} = 3.6V, IN = 3.6V, CTRL = 3.6V; measure current through the internal pull-down resistor and calculate resistance value.	Full	-	4	-	MΩ

NOTES:

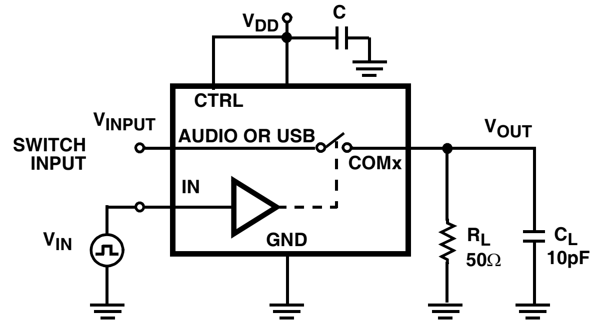
7. V_{logic} = Input voltage to perform proper function.
8. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
9. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.
10. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
11. Limits established by characterization and are not production tested.
12. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between L and R or between D+ and D-.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

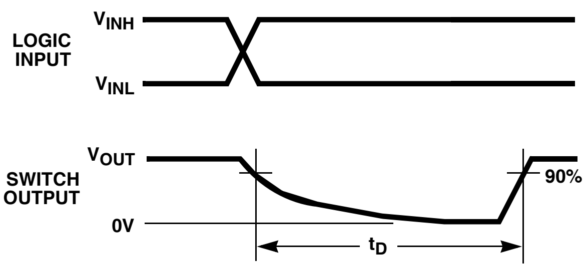
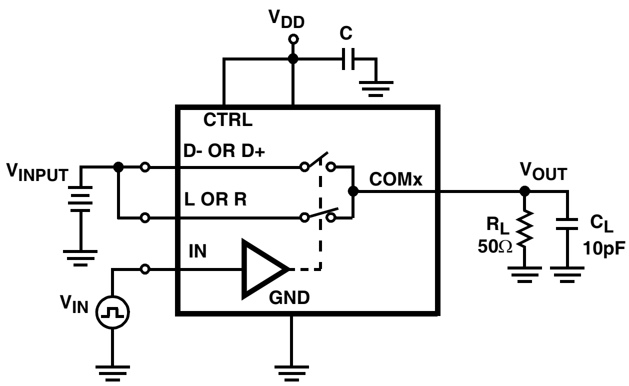


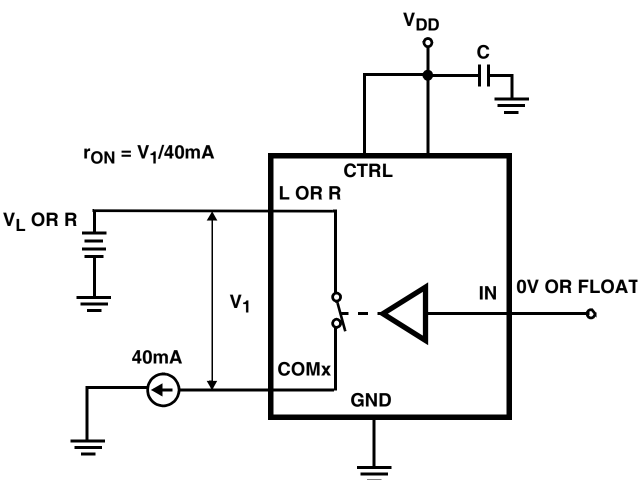
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

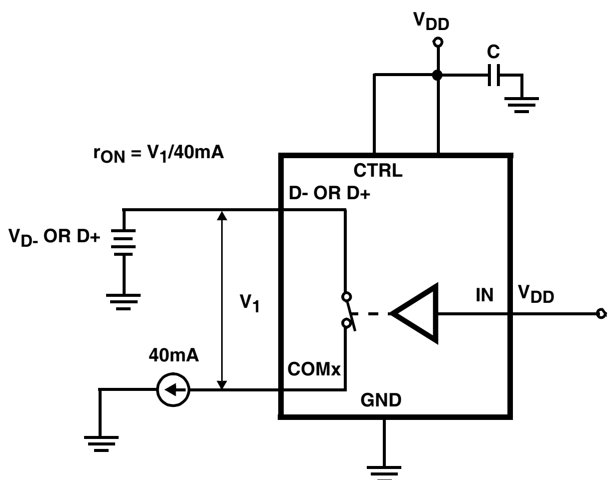
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

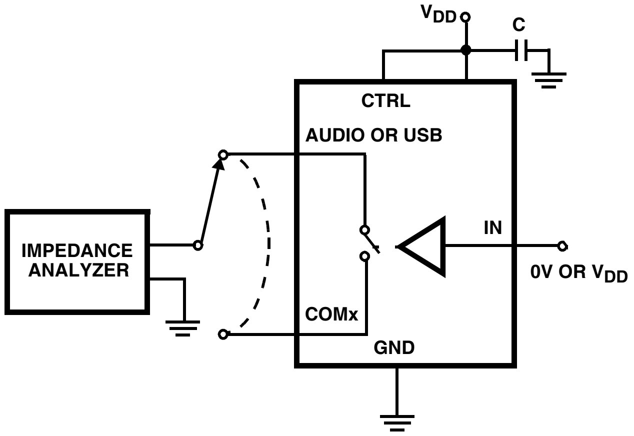
FIGURE 3. AUDIO r_{ON} TEST CIRCUIT



Repeat test for all switches.

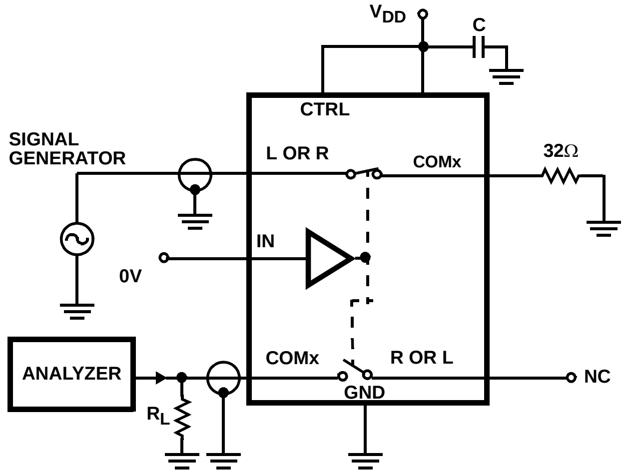
FIGURE 4. USB r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. AUDIO CROSSTALK TEST CIRCUIT

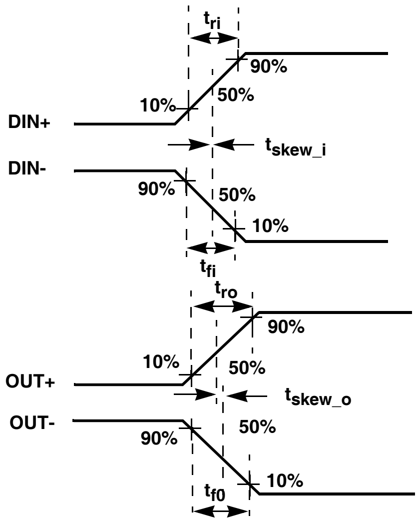
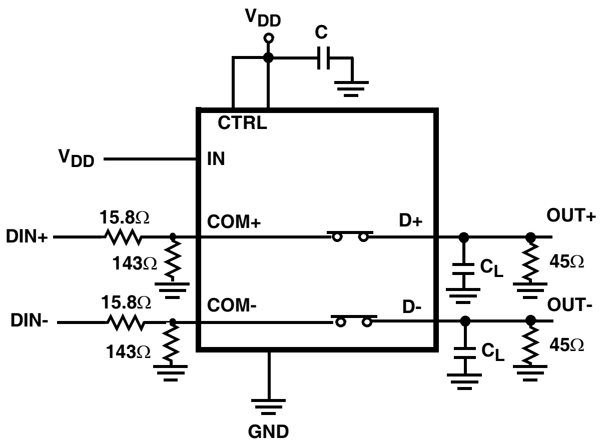


FIGURE 7A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 7B. TEST CIRCUIT

FIGURE 7. SKEW TEST

Application Block Diagrams

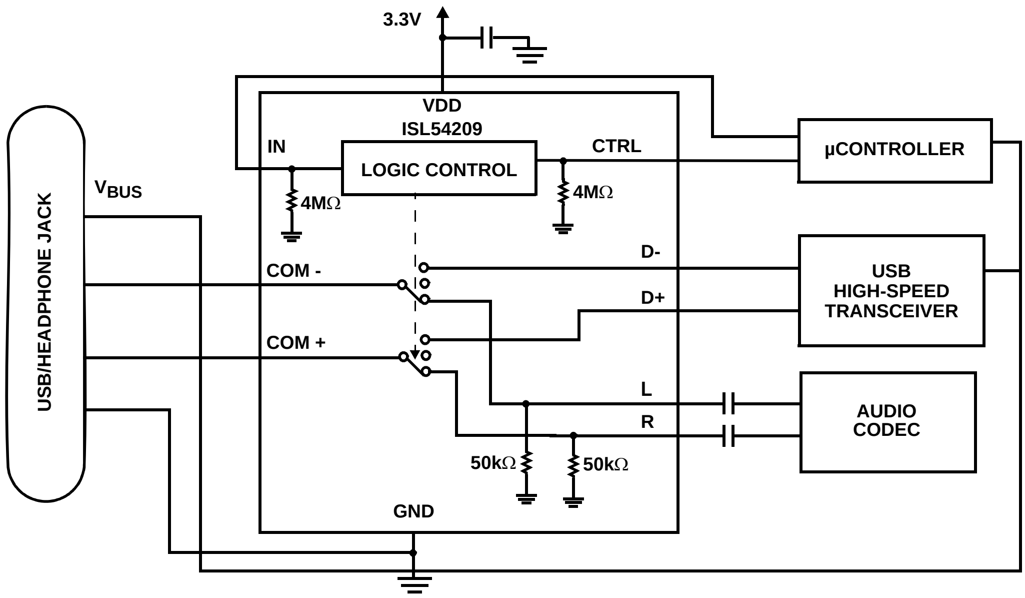


FIGURE 8. LOGIC CONTROL VIA MICRO-PROCESSOR

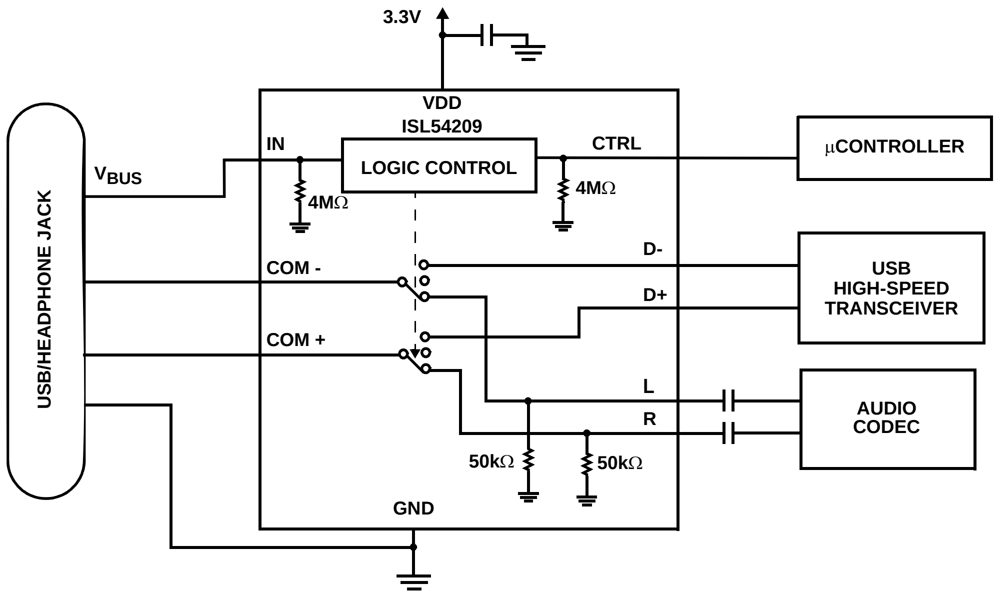


FIGURE 9. LOGIC CONTROL VIA V_{BUS} VOLTAGE FROM COMPUTER OR USB HUB

Detailed Description

The ISL54209 device is a dual single pole/double throw (SPDT) analog switch that operates from a single DC power supply in the range of 2.5V to 5.0V. It was designed to function as a dual 2 to 1 multiplexer to select between USB differential data signals and audio L and R stereo signals. It comes in tiny µTQFN and TDFN packages for use in MP3 players, PDAs, cellular phones and other personal media players.

The part consists of two 2.5Ω audio switches and two 5Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54209 was specifically designed for MP3 players, personal media players and cellular phone applications that need to combine the audio headphone jack and the USB data connector into a single shared connector, thereby saving space and component cost. Typical Application Block Diagrams of this functionality are shown in Figures 8 and 9.

The ISL54209 has a single logic control pin (IN) that selects between the audio switches and the USB switches. This pin can be driven Low or High to switch between the audio CODEC drivers and USB transceiver of the MP3 player or cellular phone. The ISL54209 also contains a logic control pin (CTRL) that when driven Low while IN is Low, opens all switches and puts the part into a low power state, drawing typically 1nA of I_{DD} current.

A detailed description of the two types of switches are provided in the following sections.

Audio Switches

The two audio switches (L, R) are 2.5Ω switches that can pass signals that swing below ground by as much as 1.5V. They were designed to pass ground reference stereo signals with minimal insertion loss and very low distortion over a ±1V signal range.

Crosstalk between the audio channels is -110dB over the audio band. Crosstalk between the audio channel and USB channel is -95dB at 100kHz. These switches have excellent off-isolation, 114dB, over the audio band with a 32Ω load.

Over a signal range of ±1V (0.707V_{RMS}) with VDD > 2.7V, these switches have an extremely low r_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion (<0.06% THD+N) when delivering 15.6mW into a 32Ω headphone speaker load. See Figures 10 and 11.

These switches are bi-directional switches. In typical applications, the audio drivers would be connected at the L and R side of the switch (pins 7 and 8) and the speaker loads would be connected at the COM side of the switch (pins 3 and 4).

The audio switches are active (turned ON) whenever the IN voltage is ≤ 0.5V or floating and the CTRL voltage ≥ to 1.4V.

USB Switches

The two USB switches (D+, D-) are bidirectional switches that can pass rail-to-rail signals. When powered with a 3.3V supply, these switches have a nominal r_{ON} of 5Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.45Ω. The r_{ON} matching between the D+ and D- switches over this signal range is only 0.05Ω ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases, the r_{ON} resistance increases. At signal level of 3.3V, the switch resistance is nominally 25Ω.

The USB switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See Figure 12.

The USB switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See Figure 13 for Full-speed Eye Pattern taken with switch in the signal path.

The maximum signal range for the USB switches is from -1.5V to V_{DD}. The signal voltage at D- and D+ should not be allow to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

The USB switches are active (turned ON) whenever the IN voltage is ≥ to 1.4V.

ISL54209 Operation

The following will discuss using the ISL54209 in the Typical Application Block Diagrams shown in Figures 8 and 9.

VDD SUPPLY

The DC power supply connected at VDD (pin 1) provides the required bias voltage for proper switch operation. The part can operate with a supply voltage in the range of 2.5V to 5.0V.

In a typical USB/Audio application for portable battery powered devices, the V_{DD} voltage will come from a battery or an LDO and be in the range of 2.7V to 3.6V. For best possible USB full-speed operation (12Mbps), it is recommended that the V_{DD} voltage be ≥2.5V in order to get a USB data signal level above 2.5V.

LOGIC CONTROL

The state of the ISL54209 device is determined by the voltage at the IN pin (pin 2) and the CTRL pin (pin 10). These logic pins are 1.8V logic compatible when V_{DD} is in the range of 2.7V to 3.6V and can be controlled by a standard µprocessor. The part has three states or modes of operation. The Audio Mode, USB Mode and the Low Power Mode. Refer to the “Truth Table” on page 2.

The IN and CTRL pins are internally pulled low through a 4MΩ resistor to ground and can be left floating or tri-stated by the µprocessor. The CTRL control pin is only active when IN is logic “0”.

The voltage at the IN pin can exceed the V_{DD} voltage by as much as 2.55V when VDD ≤ 3.6V. This allows the V_{BUS} voltage from a computer or USB hub (4.4V to 5.25V) to drive the IN pin while the VDD voltage is in the range of 2.5V to 3.6V. See “USING THE COMPUTER V_{BUS} VOLTAGE TO DRIVE THE “IN” PIN” page 10

Logic control voltage levels:

IN = Logic “0” (Low) when V_{IN} ≤ 0.5V or Floating.
IN = Logic “1” (High) when V_{IN} ≥ 1.4V
CTRL = Logic “0” (Low) when ≤ 0.5V or Floating.
CTRL = Logic “1” (High) when ≥ 1.4V

Audio Mode

If the IN pin = Logic “0” and CTRL pin = Logic “1”, the part will be in the Audio mode. In Audio mode, the L (left) and R (right) 2.5Ω audio switches are ON and the D- and D+ 5Ω switches are OFF (high impedance).

When nothing is plugged into the common connector or a headphone is plugged into the common connector, the µprocessor will sense that there is no voltage at the V_{BUS} pin of the connector and will drive and hold the IN control pin of the ISL54209 low. As long as the CTRL = Logic “1,” the ISL54209 part will be in the audio mode and the audio drivers of the media player can drive the headphones and play music.

USB Mode

If the IN pin = Logic “1” and CTRL pin = Logic “0” or Logic “1”, the part will go into USB mode. In USB mode, the D- and D+ 5Ω switches are ON and the L and R 2.5Ω audio switches are OFF (high impedance).

When a USB cable from a computer or USB hub is connected at the common connector, the µprocessor will sense the presence of the 5V V_{BUS} and drive the IN pin voltage high. The ISL54209 part will go into the USB mode. In USB mode, the computer or USB hub transceiver and the MP3 player or cell phone USB transceiver are connected and digital data will be able to be transmitted back and forth.

When the USB cable is disconnected, the µprocessor will sense that the 5V VBUS voltage is no longer connected and will drive the IN pin low and put the part back into the Audio or Low Power Mode.

Low Power Mode

If the IN pin = Logic “0” and CTRL pin = Logic “0”, the part will be in the Low Power mode. In the Low Power mode, the audio switches and the USB switches are OFF (high impedance). In this state, the device draws typically 1nA of current.

In Low Power mode, the off-isolation and crosstalk between switch cells is minimal for negative swinging signals. Care should be taken to avoid negative swinging signals in this mode of operation. In typical applications, the Low Power state will be applied to the ISL54209 part when the portable media player is in its sleep or hibernate mode to conserve battery power. In the sleep mode, no audio or USB signals are applied to the part.

USING THE COMPUTER V_{BUS} VOLTAGE TO DRIVE THE “IN” PIN

External IN Pull-Down Resistor

Rather than using a micro-processor to control the IN logic pin, one can directly drive the IN pin using the V_{BUS} voltage from the computer or USB hub.

When a headphone or nothing is connected at the common connector, the internal 4Ω pull-down will pull the IN pin low putting the ISL54209 in the Audio mode or Low Power mode, depending on the condition of the CTRL pin.

When a USB cable is connected at the common connector, the voltage at the IN pin will be driven to 5V and the part will automatically go into the USB mode.

When the USB cable is disconnected from the common connector, the voltage at the IN pin will be pulled low by the pull-down resistor and return to the Audio Mode or Low Power Mode, depending on the condition of the CTRL pin.

Note: The voltage at the IN pin can exceed the VDD voltage by as much as 2.55V when VDD ≤ 3.6V. This allows the VBUS voltage from a computer or USB hub (4.4V to 5.25V) to drive the IN pin while the V_{DD} voltage is in the range of 2.5V to 3.6V.

FN6627.0
December 20, 2007

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified.

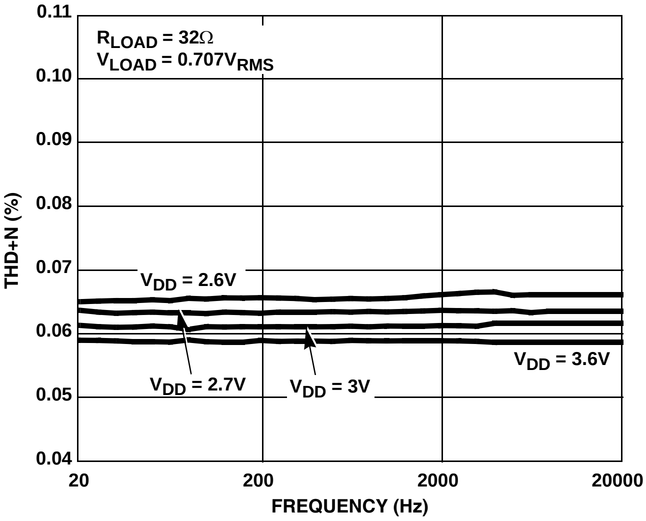


FIGURE 10. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

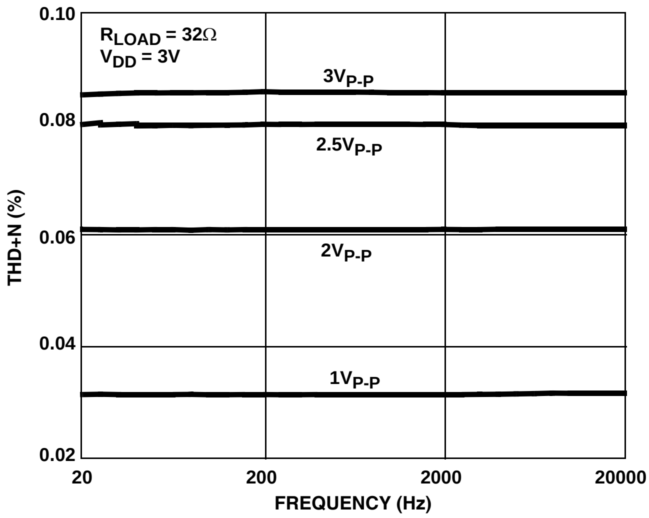


FIGURE 11. THD+N vs SIGNAL LEVELS vs FREQUENCY

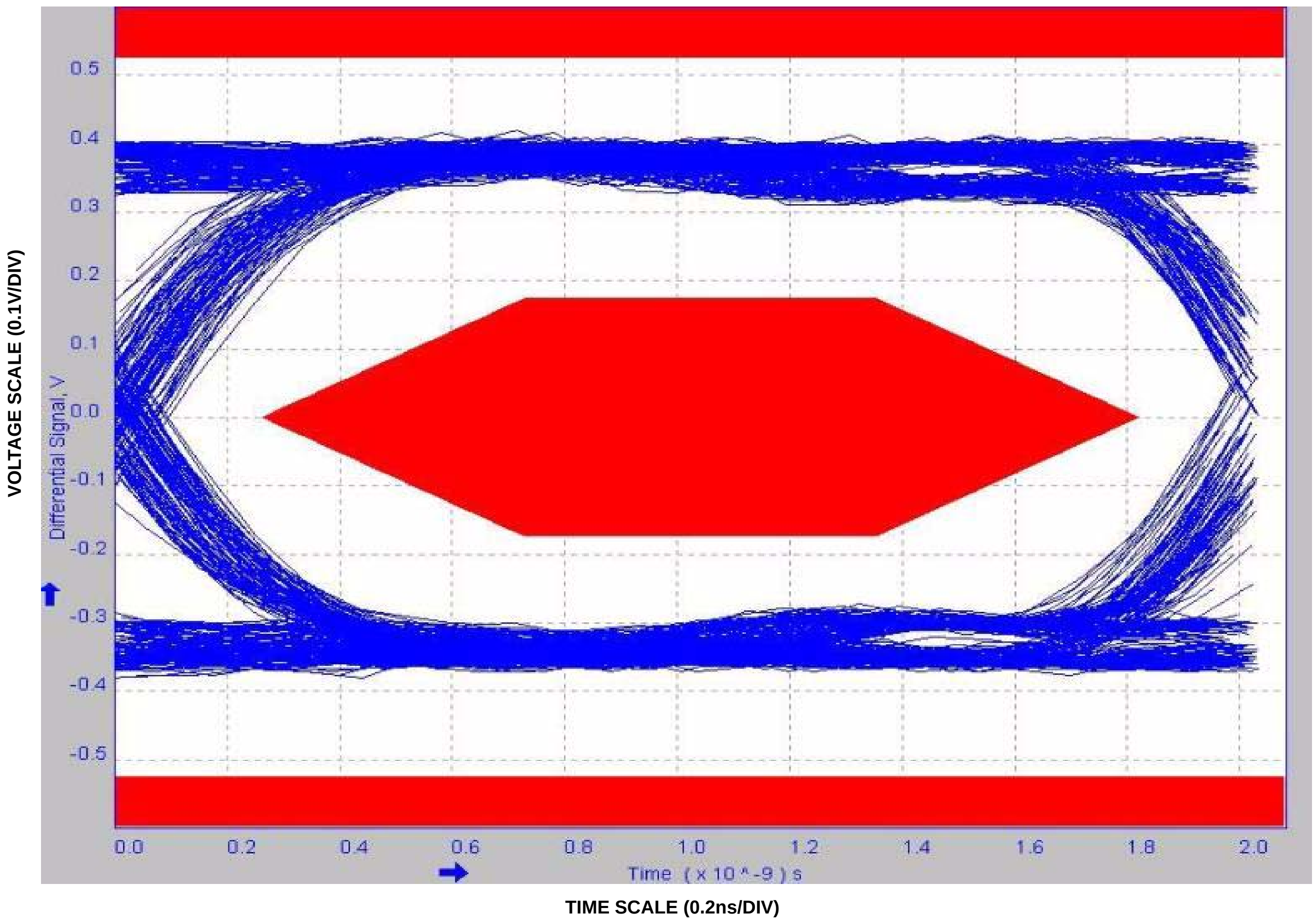
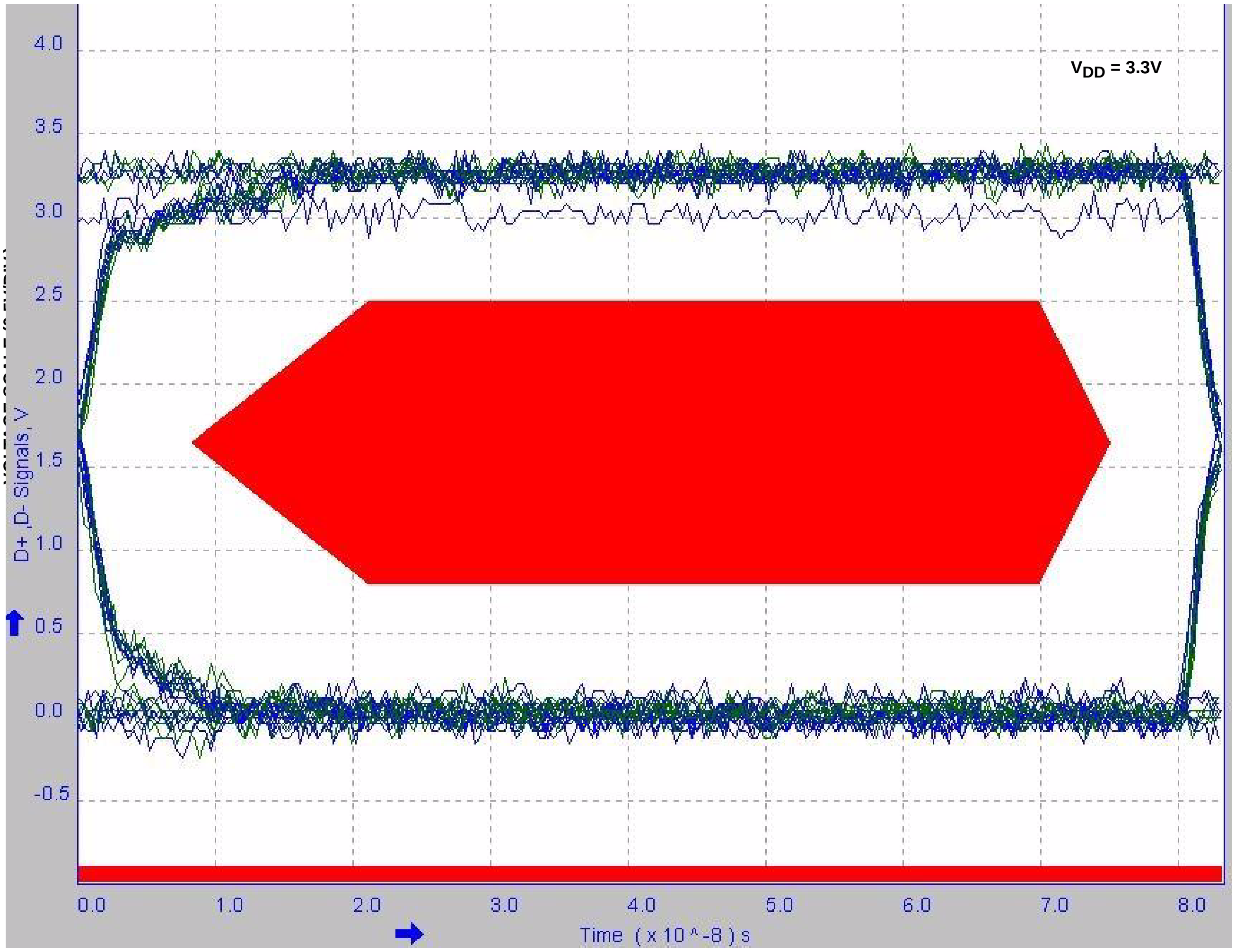


FIGURE 12. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**



TIME SCALE (10ns/DIV)

FIGURE 13. EYE PATTERN: 12Mbps USB SIGNAL WITH USB SWITCHES IN THE SIGNAL PATH

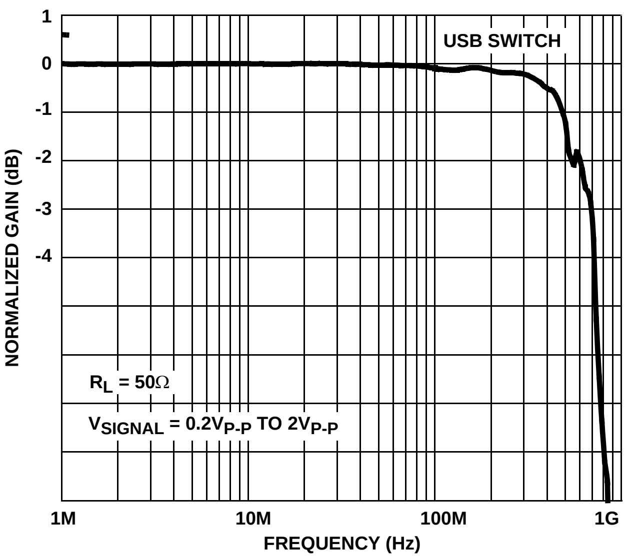


FIGURE 14. FREQUENCY RESPONSE

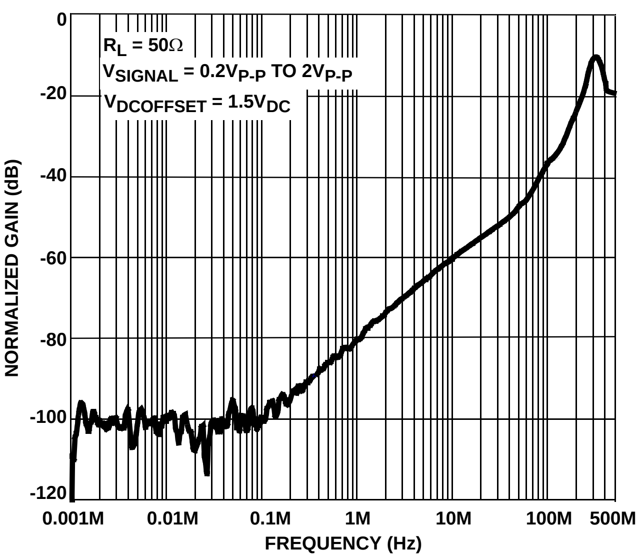


FIGURE 15. OFF-ISOLATION USB SWITCHES

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

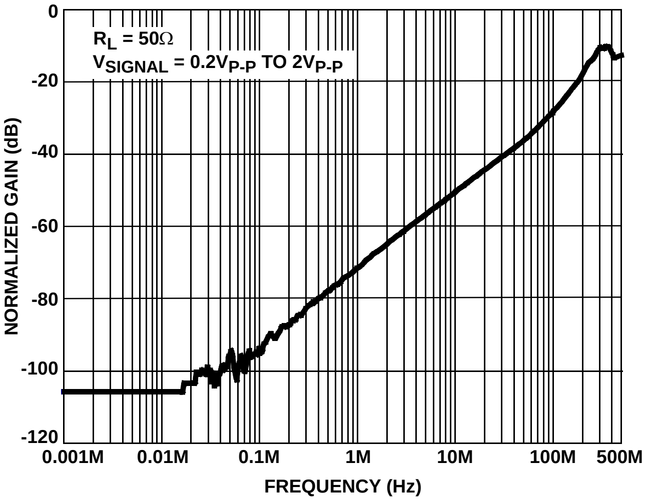


FIGURE 16. OFF-ISOLATION AUDIO SWITCHES

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

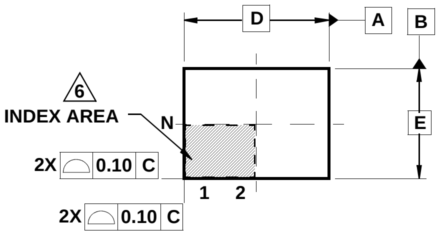
TRANSISTOR COUNT:

98

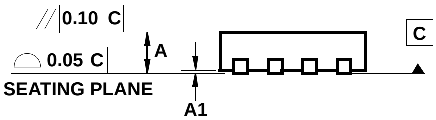
PROCESS:

Submicron CMOS

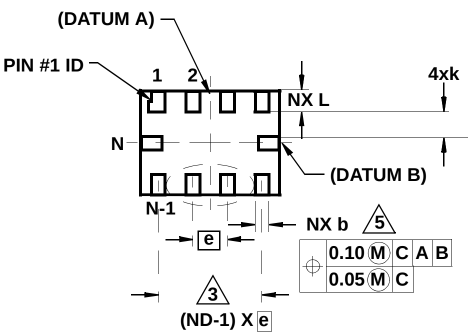
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



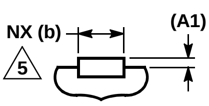
TOP VIEW



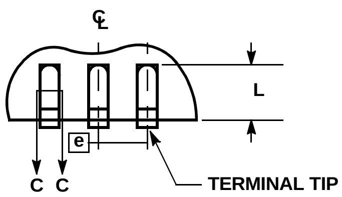
SIDE VIEW



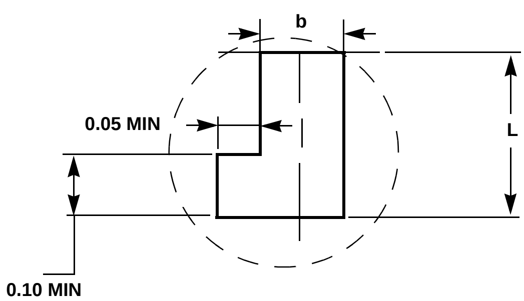
BOTTOM VIEW



SECTION "C-C"



FOR ODD TERMINAL/SIDE



DETAIL “A” PIN 1 ID

L10.2.1x1.6A

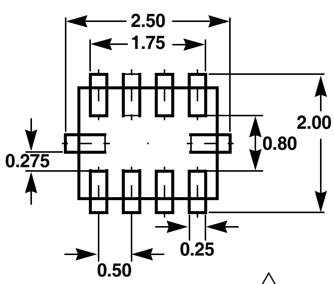
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N	10			2
Nd	4			3
Ne	1			3
θ	0	-	12	4

Rev. 3 6/06

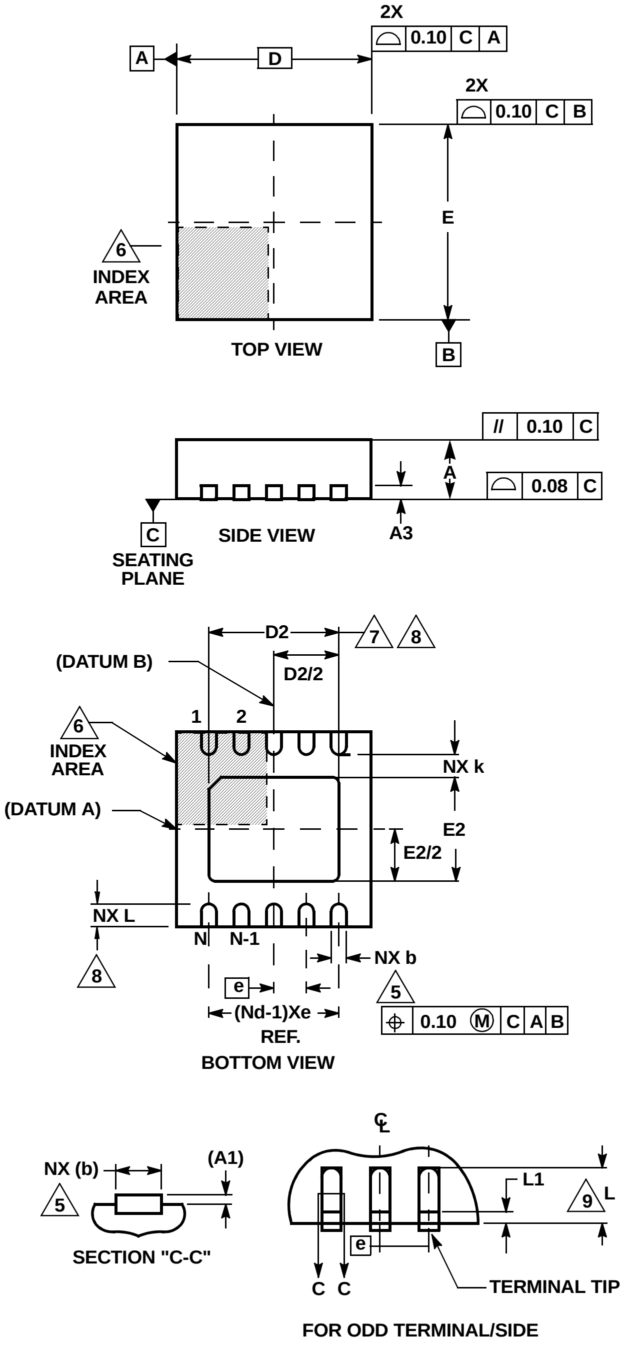
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN 10

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS MIN	NOMINAL	MAX	NOTES
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N	10			2
Nd	5			3

Rev. 3 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.