Data Sheet | September 11, 2008 | FN6346.0

400MHz Slew Rate Enhanced Rail-to-Rail Output Gain Block

The ISL55033 is a triple rail-to-rail output gain block with a -3dB bandwidth of 400MHz and slew rate of 2350V/µs into a 150Ω load. The ISL55033 has a fixed gain of +2. The inputs are capable of sensing ground. The outputs are capable of swinging to 0.45V to either rail through a 150Ω resistor connected to V+/2.

The ISL55033 is designed for general purpose video applications. The part includes a fast-acting global disable/power-down circuit.

The ISL55033 is available in a 12 Ld TQFN package. Operation is specified over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (C°)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55033IRTZ	5033	-40 to +85	12 LdTQFN	L12.3x3A
ISL55033IRTZ-T13*	5033	-40 to +85	12 LdTQFN	L12.3x3A
ISL55033EVAL1Z	***Coming Soon***			

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Features

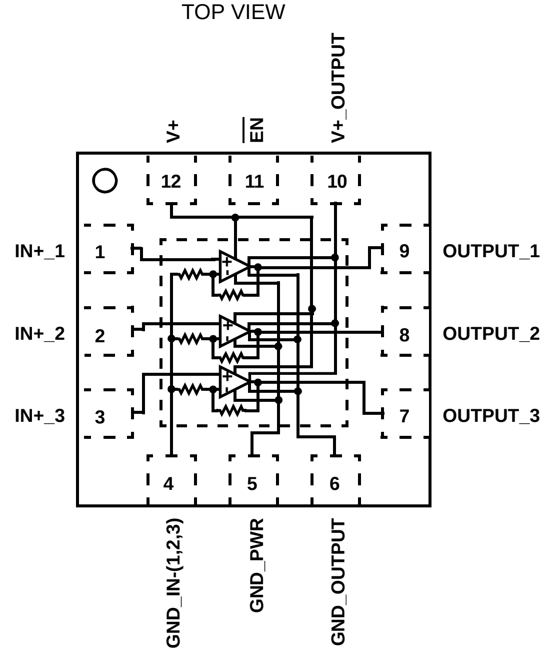
- 400MHz -3dB Bandwidth
- 2350V/µsTyp Slew Rate, R_L = 150Ω to V+/2
- Single-Supply Operation From +3V to +5.5V
- Rail-to-Rail Output
- Input Ground Sensing
- Fast 25ns Disable Time
- Pb-Free (RoHS compliant)

Applications

- Video Amplifiers
- Set-Top Boxes
- Video Distribution

Pinout

ISL55033
(12 LD TQFN)
TOP VIEW



A_V EACH CHANNEL EQUALS +2

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V+ to GND 5.75V
Supply Turn-On Voltage Slew Rate 1V/µs
EN Input Current 4mA
Input Voltage . . . . V+ + 0.3V to GND - 0.3V
Continuous Output Current 40mA
ESD Rating:
Human Body Model 2,500V
Machine Model. 300V
Charge Device Model. 1,500V

Thermal Information

Thermal Resistance (Note 1) θ_{JA} (°C/W)
12 Ld TQFN Package . . . . +57
Storage Temperature . . . .-65°C to +125°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature . . . .-40°C to +85°C
Operating Junction Temperature . . . .+125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, T_A = +25°C, R_L = 1kΩ to $V_+/2$, V_{IN} = 0.1VDC, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Output Offset Voltage	(Note 2)	-9	-1	9	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from -40°C to +85°C		-3		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-8.5	-6		µA
R_{IN}	Input Resistance			7		MΩ
C_{IN}	Input Capacitance			0.5		pF
OUTPUT CHARACTERISTICS						
A_{CL}	Closed Loop Gain	V_{OUT} = 0.5V to 4V, R_L = 150Ω	1.97	1.99	2.014	V/V
R_{OUT}	Output Resistance	A_V = +2		30		mΩ
V_{OH}	Positive Output Voltage Swing	R_L = 1kΩ to 2.5V	4.7	4.75		V
		R_L = 150Ω to 2.5V	4.5	4.55		V
V_{OL}	Negative Output Voltage Swing	R_L = 1kΩ to 2.5V		27	50	mV
		R_L = 150Ω to 2.5V		130	200	mV
I_{SC} (source)	Output Short Circuit Current	R_L = 10Ω to GND, V_{IN} = 1.5V	50			mA
I_{SC} (sink)	Output Short Circuit Current	R_L = 10Ω to + 2.5V, V_{IN} = 0V	50			mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	V+ = 3V to 5.5V, R_L = Open	65	83		dB
I_{S-ON}	Supply Current - Enabled	V_{IN} = 0.1V, R_L = Open	18.5	21.3	24.5	mA
I_{S-OFF}	Supply Current - All Amplifiers Disabled	R_L = Open	275	486	900	µA
ENABLE						
t_{EN}	Enable Time	R_L = 150Ω, V_{IN} = 0.5V		250		ns
t_{DS}	Disable Time	R_L = 150Ω, V_{IN} = 0.5V		25		ns
V_{IH-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Power-Up			0.8		V
V_{IL-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Shut-Down			2		V

Electrical Specifications

V_+ = 5V, T_A = +25°C, R_L = 1kΩ to V_+/2, V_{IN} = 0.1VDC, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
I_{IH-ENB}	$\overline{ENABLE}$ Pin Input Current High	$V_{\overline{EN}}$ = 5V	1	7	15	µA
I_{IL-ENB}	$\overline{ENABLE}$ Pin Input for Current Low	$V_{\overline{EN}}$ = 0V	-10	2	10	µA
AC PERFORMANCE						
BW	-3dB Bandwidth	V_{OUT} = 100mV$_{P-P}$, R_L = 150Ω, C_L = 2pF, V_{IN} = 1.0 VDC		400		MHz
BW	±0.1dB Bandwidth	V_{OUT} = 100mV$_{P-P}$, R_L = 150Ω, C_L = 2pF		60		MHz
Peak	Peaking	V_{OUT} = 100mV$_{P-P}$, R_L = 150Ω, C_L = 3.2pF		1.5		dB
dG	Differential Gain	V_{IN} = 0.1V to 2.0V, V_{OUT} = 100mV$_{P-P}$, f = 3.58MHz, R_L = 150Ω		0.012		%
dP	Differential Phase			0.11		°
e_{N-OUT}	Output Voltage Noise Density	f = 10kHz		35		nV/√Hz
i_N	Input Current Noise Density	f = 10kHz		2.9		pA/√Hz
ISO	Off-State Isolation f_O = 10MHz	V_{IN} = 0.8VDC + 1V$_{P-P}$, C_L = 2pF, R_L = 150Ω		-80		dB
X-TALK	Channel-to-Channel Crosstalk, f_O = 10MHz	V_{IN} = 0.8VDC + 1V$_{P-P}$, C_L = 2pF, R_L = 150Ω		-65		dB
PSRR	Power Supply Rejection Ratio f_O = 10MHz	V_{IN} = 0.2VDC, V_{SOURCE} = 1V$_{P-P}$, C_L = 2pF, R_L = 150Ω		-55		dB
TRANSIENT RESPONSE						
SR	Slew Rate 25% to 75%	R_L = 150Ω, V_{OUT} = 0.5V to 3.5V		2350		V/µs
t_r, t_f Large Signal	Rise Time, t_r 20% to 80%	V_{OUT} = 3V$_{P-P}$, R_L = 150Ω, C_L = 2pF		0.8		ns
	Fall Time, t_f 80% to 20%			0.7		ns
	Rise Time, t_r 20% to 80%	V_{OUT} = 2V$_{P-P}$, R_L = 150Ω, C_L = 2pF		0.6		ns
	Fall Time, t_f 80% to 20%			0.6		ns
t_r, t_f, Small Signal	Rise Time, t_r 20% to 80%	V_{OUT} = 100mV$_{P-P}$, R_L = 150Ω, C_L = 2pF		0.55		ns
	Fall Time, t_f 80% to 20%			0.55		ns
OS	Overshoot	100mV step		13		%
t_{PD}	Propagation Delay	100mV step; R_L = 150Ω		1		ns
t_S	0.1% Settling Time	2V step		65		ns

NOTES:

2. V_{OS} is extrapolated from 2 output voltage measurements, with V_{IN} = 62.5mV and V_{IN} = 125mV, R_L = 1k.
3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

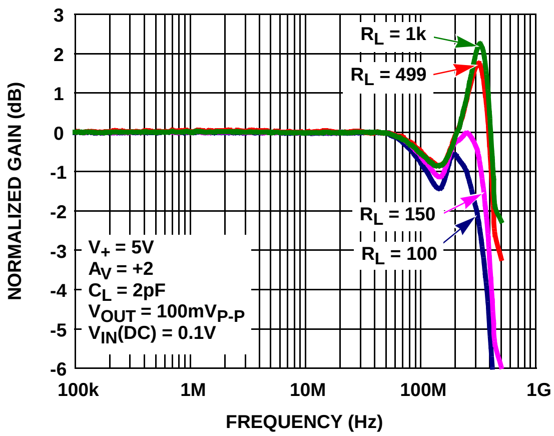


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

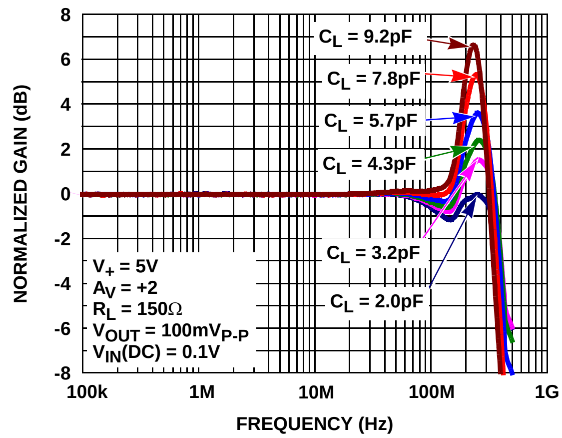


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

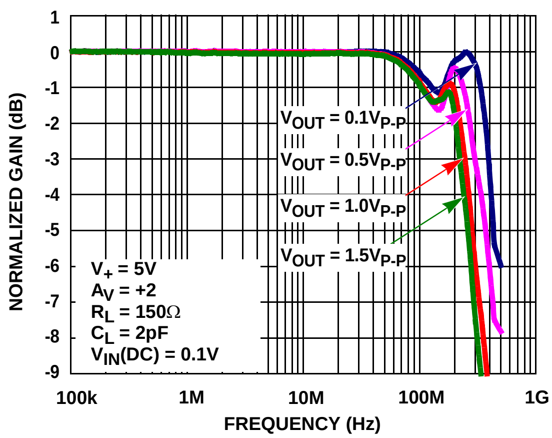


FIGURE 3. -3dB BANDWIDTH vs V_{OUT}

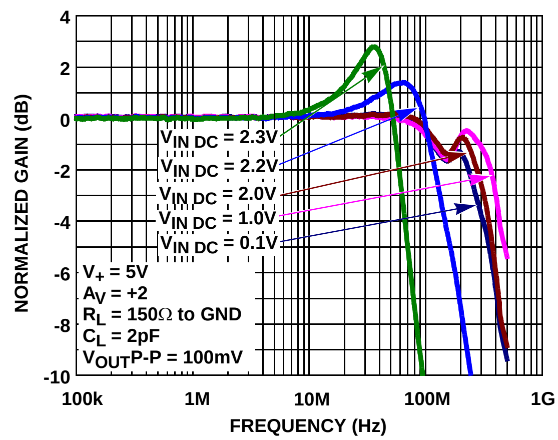


FIGURE 4. GAIN vs FREQUENCY vs DC INPUT VOLTAGE

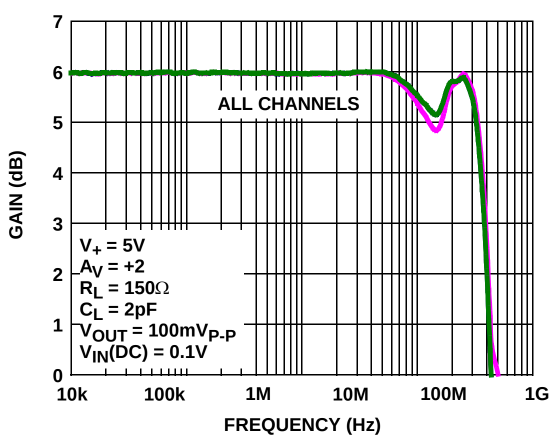


FIGURE 5. GAIN vs FREQUENCY - ALL CHANNELS

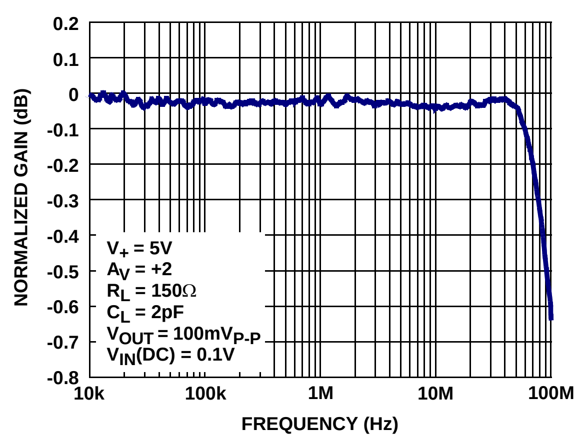


FIGURE 6. 0.1 dB GAIN FLATNESS

Typical Performance Curves (Continued)

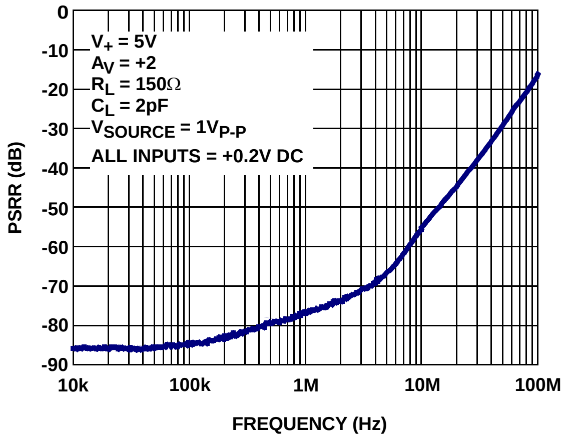


FIGURE 7. PSRR vs FREQUENCY

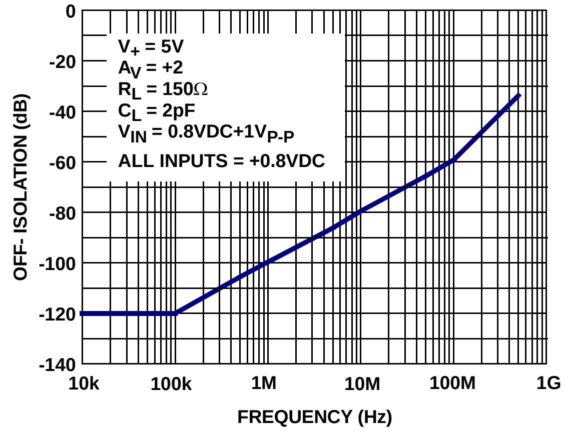


FIGURE 8. OFF-ISOLATION vs FREQUENCY

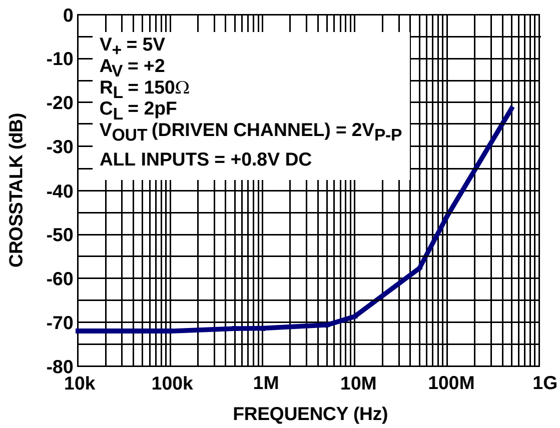


FIGURE 9. CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY

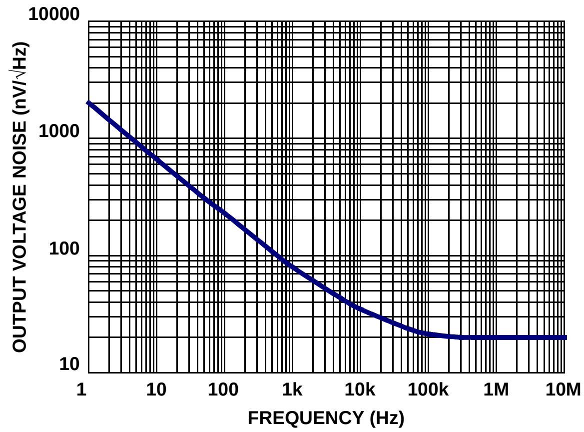


FIGURE 10. OUTPUT VOLTAGE NOISE DENSITY vs FREQUENCY

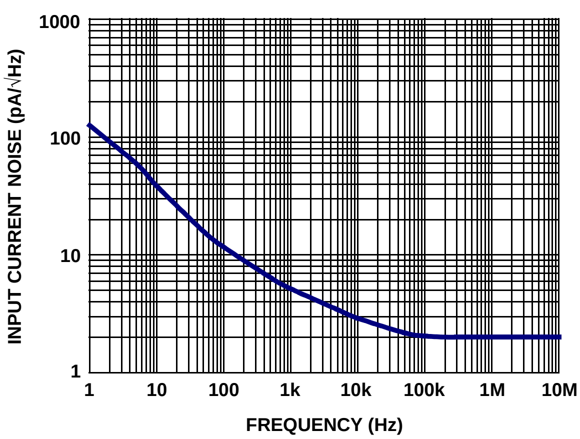


FIGURE 11. INPUT CURRENT NOISE DENSITY vs FREQUENCY

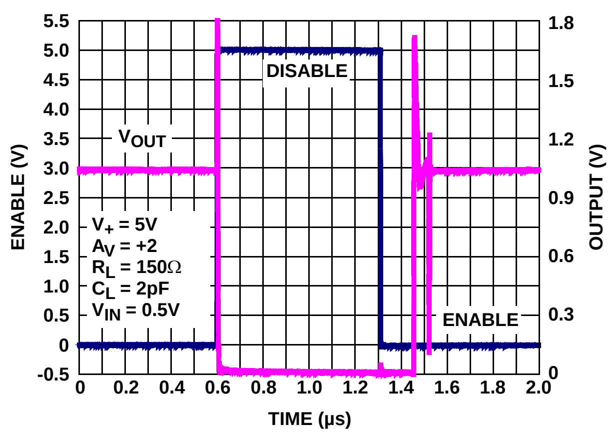


FIGURE 12. ENABLE/DISABLE TIMING

Typical Performance Curves (Continued)

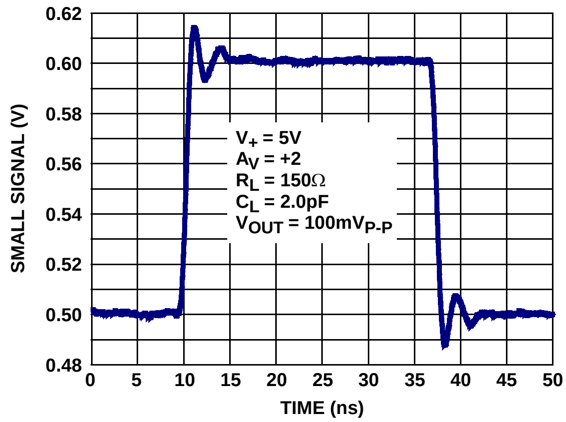


FIGURE 13. SMALL SIGNAL STEP RESPONSE

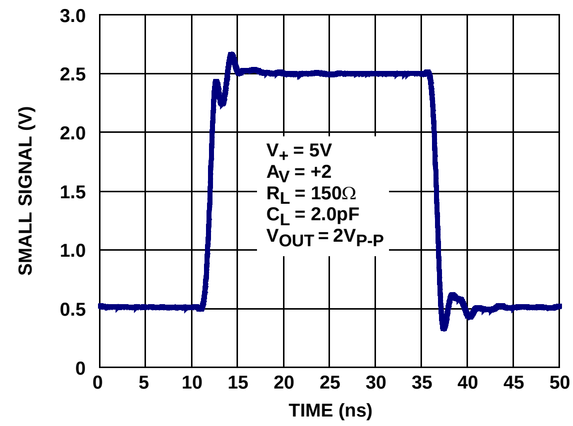


FIGURE 14. LARGE SIGNAL ($2V_{P-P}$) STEP RESPONSE

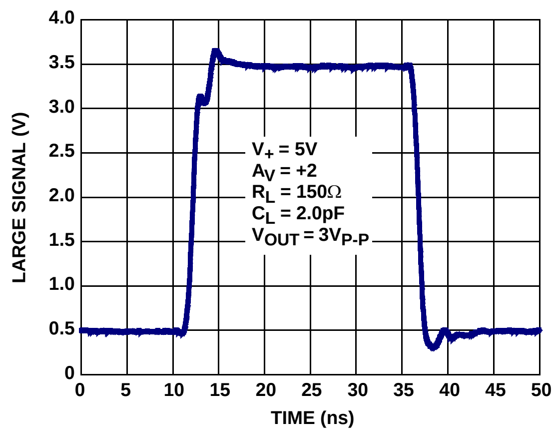


FIGURE 15. LARGE SIGNAL ($3V_{P-P}$) STEP RESPONSE

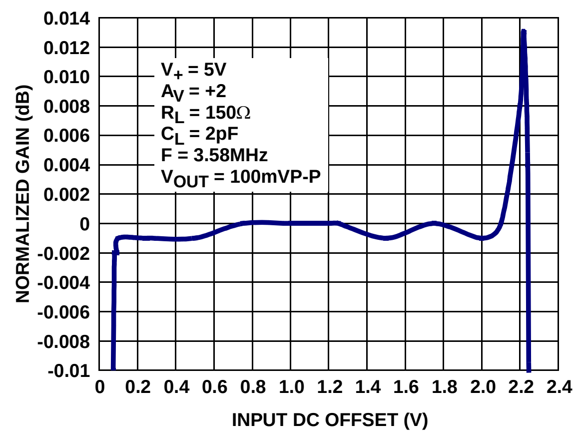


FIGURE 16. DIFFERENTIAL GAIN

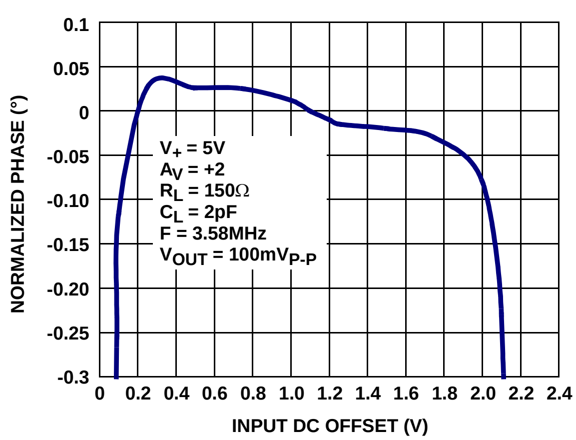


FIGURE 17. DIFFERENTIAL PHASE

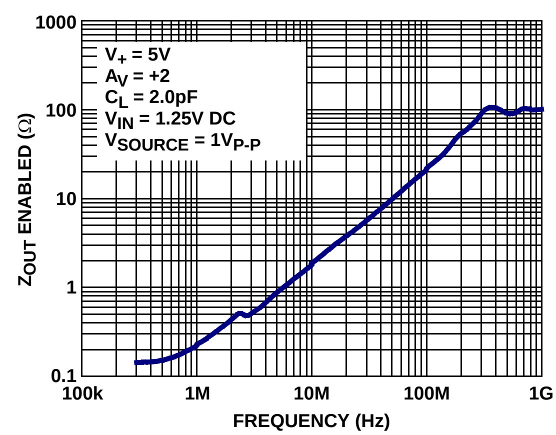


FIGURE 18. Z_{OUT} (ENABLED) vs FREQUENCY

Typical Performance Curves (Continued)

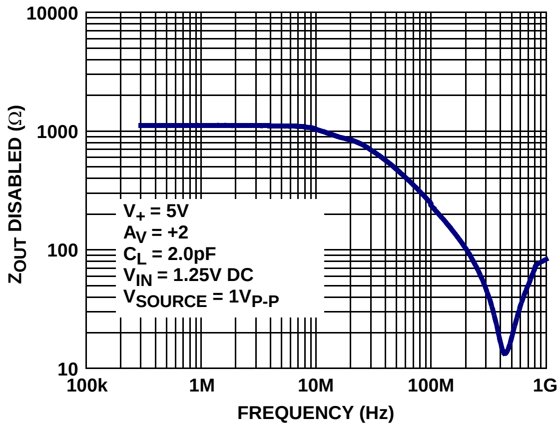


FIGURE 19. Z_{OUT} (DISABLED) vs FREQUENCY

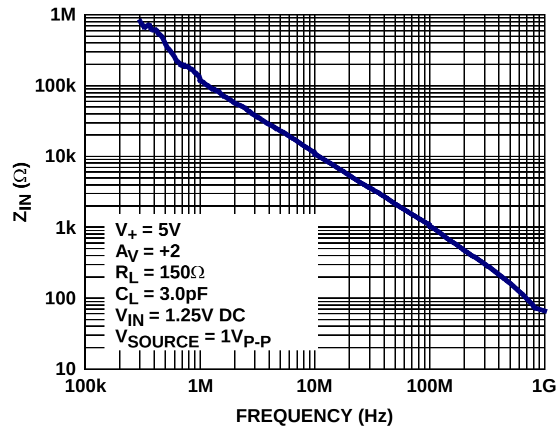


FIGURE 20. Z_{IN} vs FREQUENCY

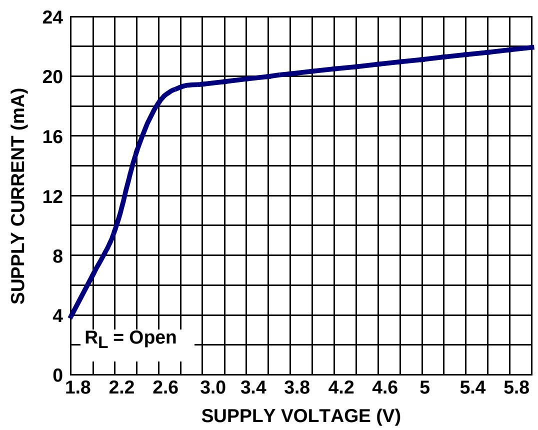


FIGURE 21. SUPPLY CURRENT vs SUPPLY VOLTAGE

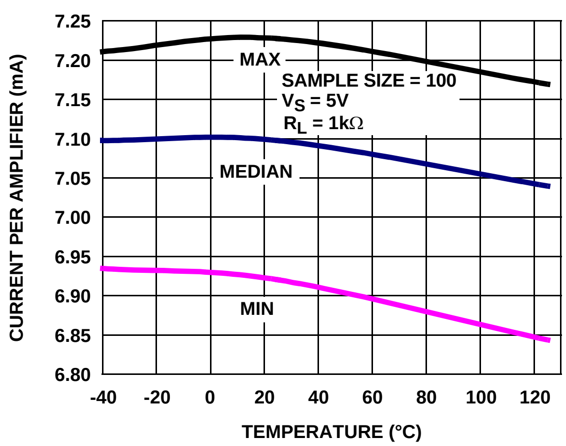


FIGURE 22. ENABLED SUPPLY CURRENT vs TEMPERATURE

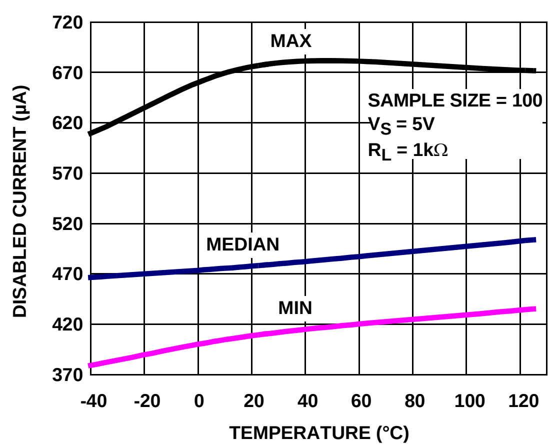


FIGURE 23. DISABLED SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

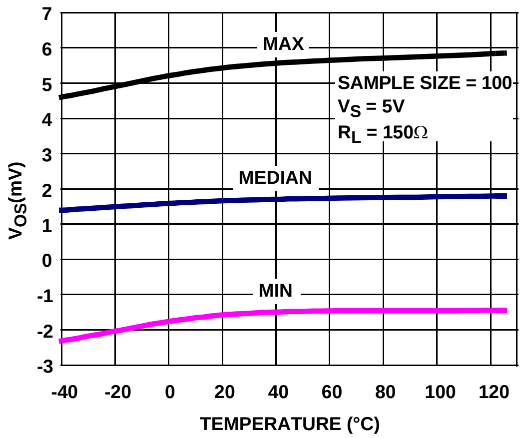


FIGURE 24. OUTPUT OFFSET VOLTAGE V_{OS} vs TEMPERATURE

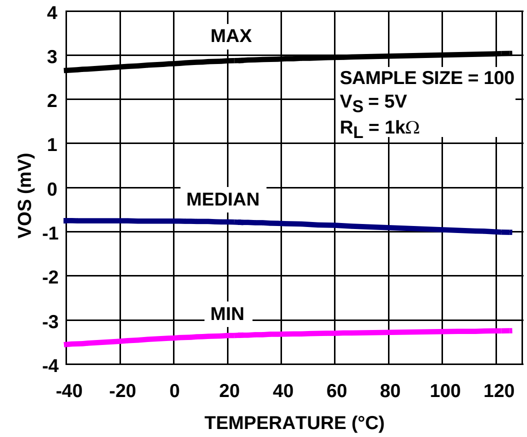


FIGURE 25. OUTPUT OFFSET VOLTAGE V_{OS} vs TEMPERATURE

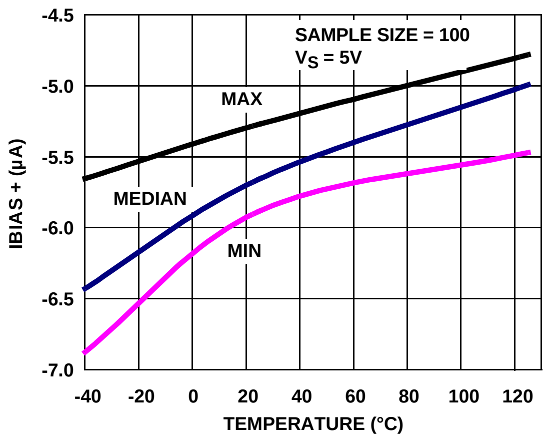


FIGURE 26. I_{BIAS} vs TEMPERATURE

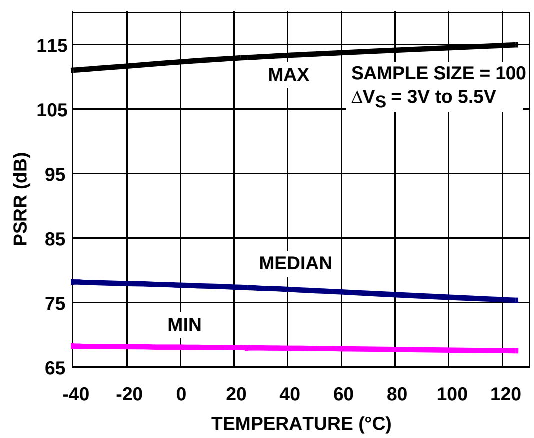


FIGURE 27. PSRR vs TEMPERATURE

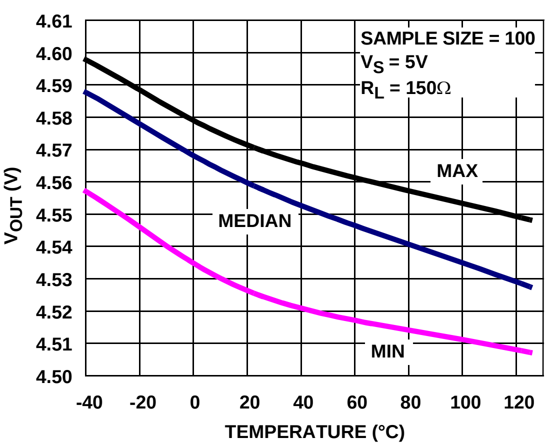


FIGURE 28. V_{OUT} HIGH vs TEMPERATURE

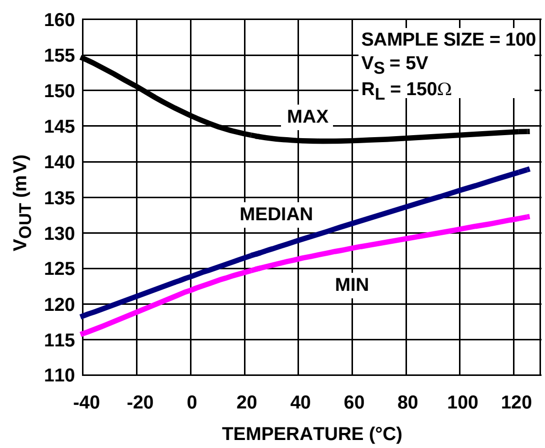


FIGURE 29. V_{OUT} LOW vs TEMPERATURE

Typical Performance Curves (Continued)

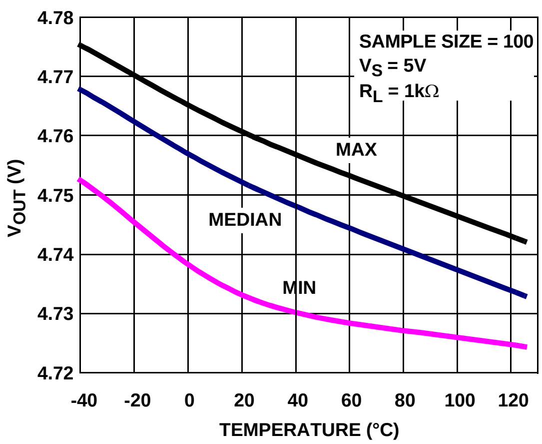


FIGURE 30. V_{OUT} HIGH vs TEMPERATURE

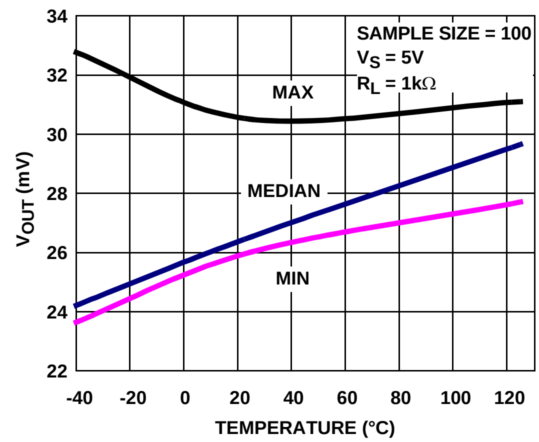
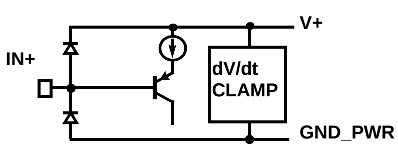


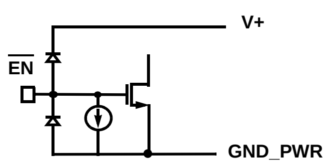
FIGURE 31. V_{OUT} LOW vs TEMPERATURE

Pin Descriptions

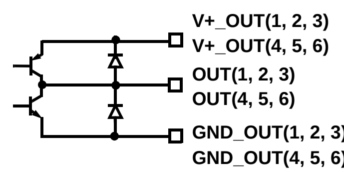
ISL55033 12 LD TQFN	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	IN+_1	Circuit 1	Amplifier 1 Non-inverting Input
2	IN+_2	Circuit 1	Amplifier 2 Non-inverting Input
3	IN+_3	Circuit 1	Amplifier 3 Non-inverting Input
4	GND IN-(1, 2, 3)	Circuit 1	Common input for Amplifiers 1, 2, 3 Inverting Inputs
5	GND_PWR	Circuit 4	Power Supply Ground
6	GND_OUTPUT	Circuit 4	Output Power Supply Ground
7	OUTPUT_3	Circuit 3	Amplifier 3 Output
8	OUTPUT_2	Circuit 3	Amplifier 2 Output
9	OUTPUT_1	Circuit 3	Amplifier 1 Output
10	V+_OUTPUT	Circuit 4	Output Power Supply
11	$\overline{EN}$	Circuit 2	$\overline{\text{Enable}}$ pin internal pull-down: Logic "1" selects the disabled state; Logic "0" selects the enabled state
12	V+	Circuit 4	Positive Power Supply



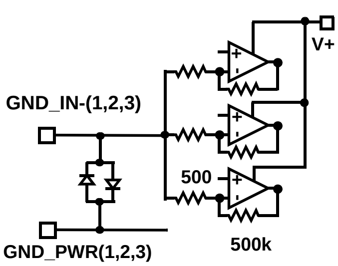
CIRCUIT 1



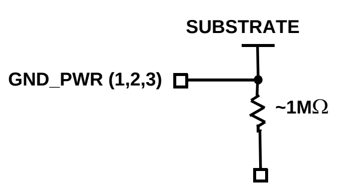
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4



CIRCUIT 5

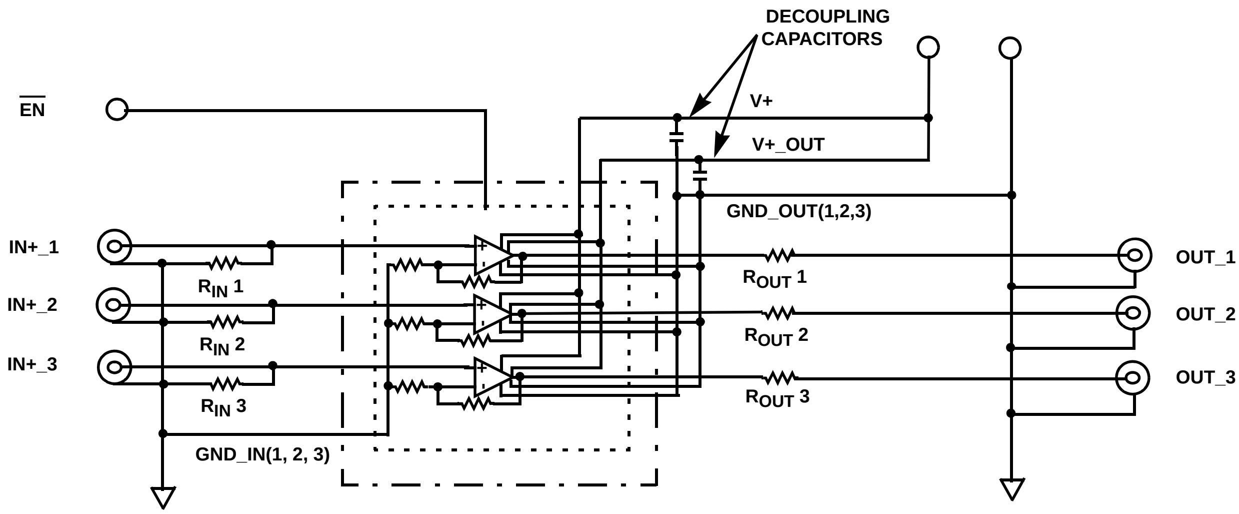


FIGURE 32. BASIC APPLICATION CIRCUIT

Application Information

General

The ISL55033 single supply, fixed gain, triple amplifier is intended for use in a variety of video and other high speed applications. The device features a ground-sensing PNP input stage and a bipolar rail-to-rail output stage. The three amplifiers have an internally fixed gain of 2, and share a single enable pin as shown in Figure 32.

Ground Connections

For the best isolation performance and crosstalk rejection, all GND pins must connect directly to the GND plane. In addition, the electrically conductive thermal pad must also connect directly to ground.

Power Considerations

Separate V+ power supply and GND pins for the input and output stages are provided to maximize PSRR. Providing separate power pins provides a way to prevent high speed transient currents in the output stage from bleeding into the sensitive amplifier input and gain stages. To maximize crosstalk isolation, each power supply pin should have its own de-coupling capacitors connected as close to the pin as possible as shown in Figure 30 (0.1µF in parallel with 1nF recommended).

The ESD protection circuits use internal diodes from all pins to the V_+ and ground pins. In addition, a dV/dt-triggered clamp is connected between the V_+ and V_- pins, as shown in the Equivalent Circuits 1 through 4 in Figure 32. The dV/dt triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the maximum rates-of-rise is not exceeded.

Single Supply Input/Output Considerations

For best performance, the input signal voltage range should be maintained between 0.1V to 2.1V. These input limits correspond to an output voltage range of 0.2V to 4.2V and define the limits of linear operation. Figure 4 shows the frequency response versus the input DC voltage level. Figures 16 and 17 show the differential gain-phase performance over the input range of 0V to 2.4V operating into a 150Ω load. The 0.1V to 2.1V input levels corresponds to a 0.2V to 4.2V output levels, which define the minimum and maximum range of output linear operation.

Composite video with sync requires care to ensure that the negative sync tip voltage (typically -300mV) is properly level-shifted up into the ISL55033 input linear operating region of +0.1V to 2.1V. The high input impedance enables AC coupling using low values of coupling capacitance with relatively high input voltage divider resistances.

$\overline{EN}$ and Power-Down States

The $\overline{EN}$ pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{EN}$ pin. The power-down state is established within approximately 25ns, if a logic high (>2V) is placed on the $\overline{EN}$ pin. In the power-down state, supply current is reduced significantly by shutting the three amplifiers off. The output presents a relatively high impedance (~2kΩ) to the output pin. Multiplexing several outputs together is possible using the enable/disable function as long as the application can tolerate the limited power-down output impedance.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 40mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners. Use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless controlled impedance (50Ω or 75Ω) strip lines or microstrips are used.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC decoupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Input termination resistors should be as close to the input terminal as possible and output termination resistors as close to the receiving device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- A minimum of 2 power supply decoupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible. Avoid vias between the capacitor and the device because vias add unwanted inductance. Larger capacitors can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to power supply ground through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the power ground pins through the substrate, the thermal pad must be tied to the power supply ground to prevent unwanted current flow through the thermal pad. Maximum AC performance is achieved if the thermal pad has good contact to the IC ground pins. Heat sinking requirements can be satisfied using thermal vias directly beneath the thermal pad to a heat dissipating layer of a square at least 1” on a side.

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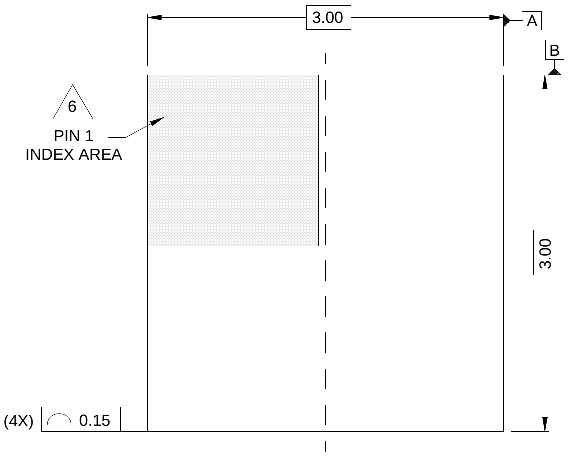
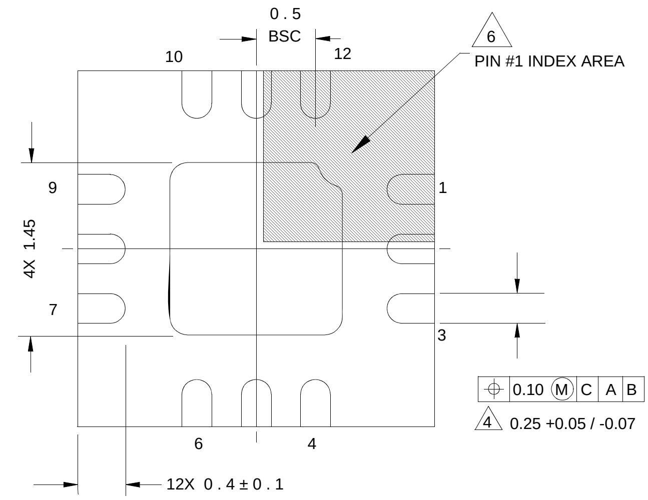
Package Outline Drawing

L12.3x3A

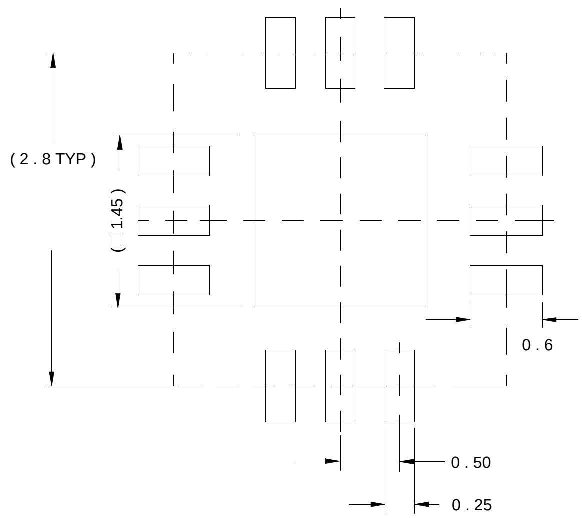
12 LEAD THIN QUAD FLAT NO LEAD PLASTIC PACKAGE
Rev 0, 09/07



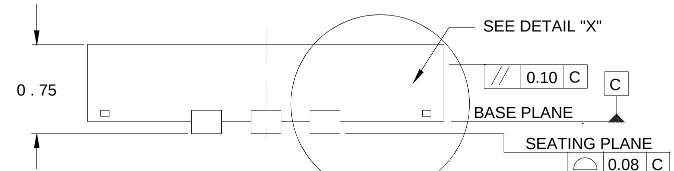
TOP VIEW



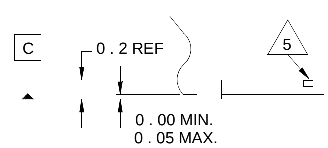
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.