



LA6569

Monolithic Linear IC
For Optical Disk Applications
5-channel Driver

Overview

The LA6569 is a 5-channel driver for optical disc drives that includes a regulator on/off circuit.

Functions

- Power amplifier 5-channel built-in. (Bridge-connection (BTL) : 4-channel, H bridge : 1-channel)
- I_O max 1A.
- Level shift circuit built-in (except H bridge).
- Mute circuit (output ON/OFF) built-in.
(Operable with BTL AMP with MUTE1 : CH1 and MUTE2 : CH2 to 4 and not operable for the H bridge of 3.3VREG.)
- 3.3V regulator built-in (external PNP transistor).
- With a function to set the loading output voltage.
- Overheat protection circuit (thermal shutdown) built-in.
- Regulator ON/OFF circuit built-in.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	Each output for H bridge, channel 1 to 4	1	A
Maximum input voltage	V_{INB} max		13	V
Mute pin voltage	V_{MUTE}		13	V
Allowable operation	P_d max	Independent IC	0.8	W
		Mounted on a specified board*	2.0	W
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

*Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

LA6569

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	Same for V_{CC} -VREG	4.5 to 13	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{REF} = 1.65\text{V}$, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All blocks						
No-load current drain ON	I_{CC-ON}	FWD = REV = 0, All outputs ON *1		30	50	mA
No-load current drain OFF	I_{CC-OFF}	FWD = REV = 0, All outputs OFF *1		10	20	mA
VREF input voltage range	V_{REF-IN}		1		$V_{CC}-1.5$	V
Thermal shutdown temperature	TSD	*2	150	175	200	$^\circ\text{C}$
BTL AMP block (CH1 to CH4)						
Output offset voltage	V_{OFF}	Voltage difference between outputs for BTL AMP, each channel. *3	-60		+60	mV
Input voltage range	V_{IN}	Input voltage range for input for OP-AMP.	0		$V_{CC}-1.5$	V
Output voltage	V_O	Each voltage between V_{O^+} and V_{O^-} when $R_L = 8\Omega$. *4	5.7	6.5		V
Closed-circuit voltage gain	VG	Input and output gain. *3	5.4	6	6.6	Times
Slew rate	SR	AMP Independent. Multiply 2 between outputs. *2		0.5		$\text{V}/\mu\text{s}$
MUTE ON voltage	$V_{MUTE-ON}$	Each MUTE *5	2			V
MUTE OFF voltage	$V_{MUTE-OFF}$	Each MUTE *5			0.5	V
Input AMP block (CH1 to CH4)						
Input voltage range	V_{IN-OP}		0		$V_{CC}-1.5$	V
Output current (SINK)	SINK-OP		2			mA
Output current (SOURCE)	SOURCE-OP	*6	300	500		μA
Output offset voltage	V_{OFF-OP}		-10		+10	mV
Loading block (CH5, H bridge)						
Output voltage	V_{O-LOAD}	Forward, reverse, $R_L = 8\Omega$ *4	5.7	6.5		V
Break output saturation voltage	$V_{CE-BREAK}$	Output voltage at braking *7			0.3	V
Input low level	V_{IN-L}				1	V
Input high level	V_{IN-H}		2			V
Output set voltage	VCONT	$I_O = 200\text{mA}$ (Between outputs), VCONT = 3V	2.9	3.15	3.4	V
Power supply block (PNP transistor : 2SB632K-use)						
3.3V supply output	V_{OUT}	$I_O = 200\text{mA}$	3.15	3.3	3.45	V
REG-IN SINK current	REG-IN-SINK	Base current to external PNP *8		10		mA
Line regulation	ΔV_{OLN}	$6\text{V} \leq V_{CC} \leq 12\text{V}$		20	150	mV
Load regulation	ΔV_{OLD}	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	200	mV
Regulator ON	REG-EN-ON	Regulator ON *9	2			V
Regulator OFF	REG-EN-OFF	Regulator OFF *9			0.5	V

*1. Current dissipation that is a sum of V_{CC1} and V_{CC2} at no load.

*2. Design guarantee value.

*3. Input AMP is a BUFFER AMP.

*4. Voltage difference between both ends of load (8Ω). Output saturated.

*5. Output ON with MUTE : [H] and OFF with MUTE : [L] (HI impedance).

*6. The source of input OP-AMP is a constant current. As the $11\text{k}\Omega$ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.

*7. Short (GND) brake used. SINK side output ON.

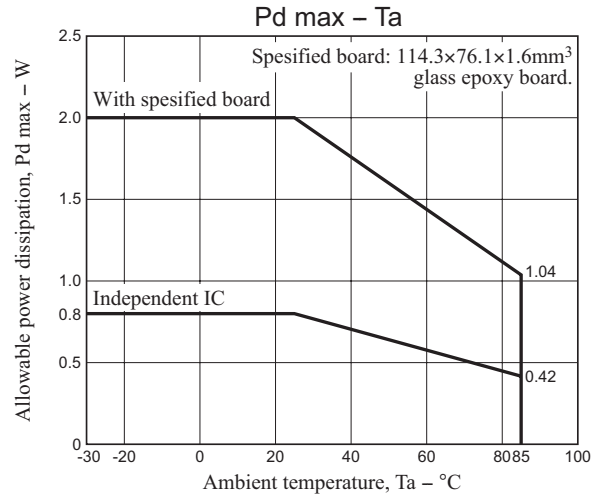
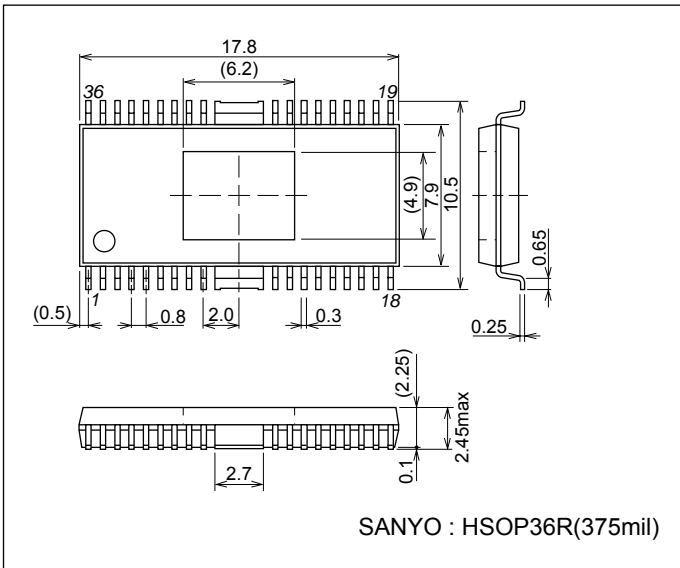
*8. 3.3VREG incorporates a drooping protection circuit and operated when the base current is 10mA (TYP).

*9. The output is 3.3V when the REG-EN pin is HIGH.

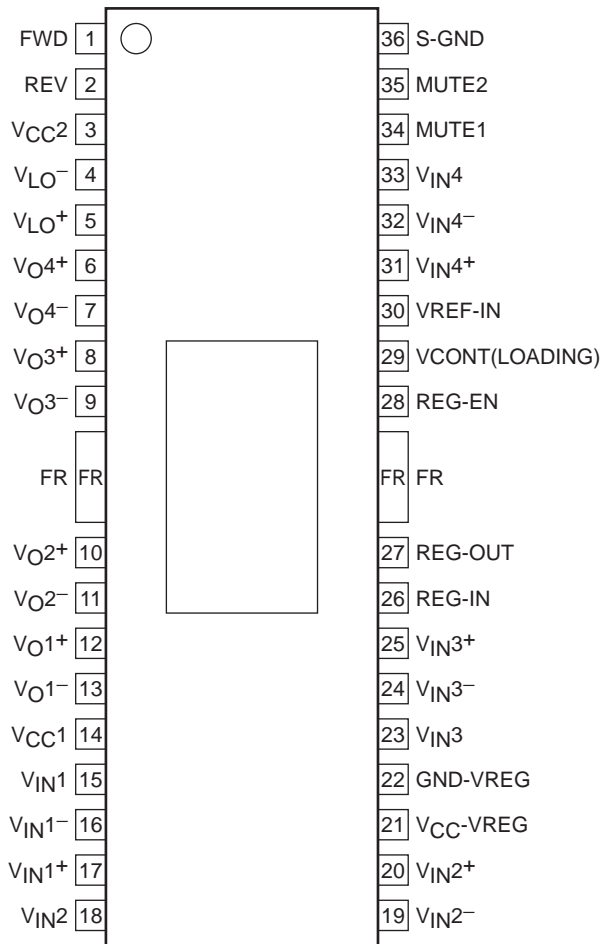
Package Dimensions

unit : mm (typ)

3251

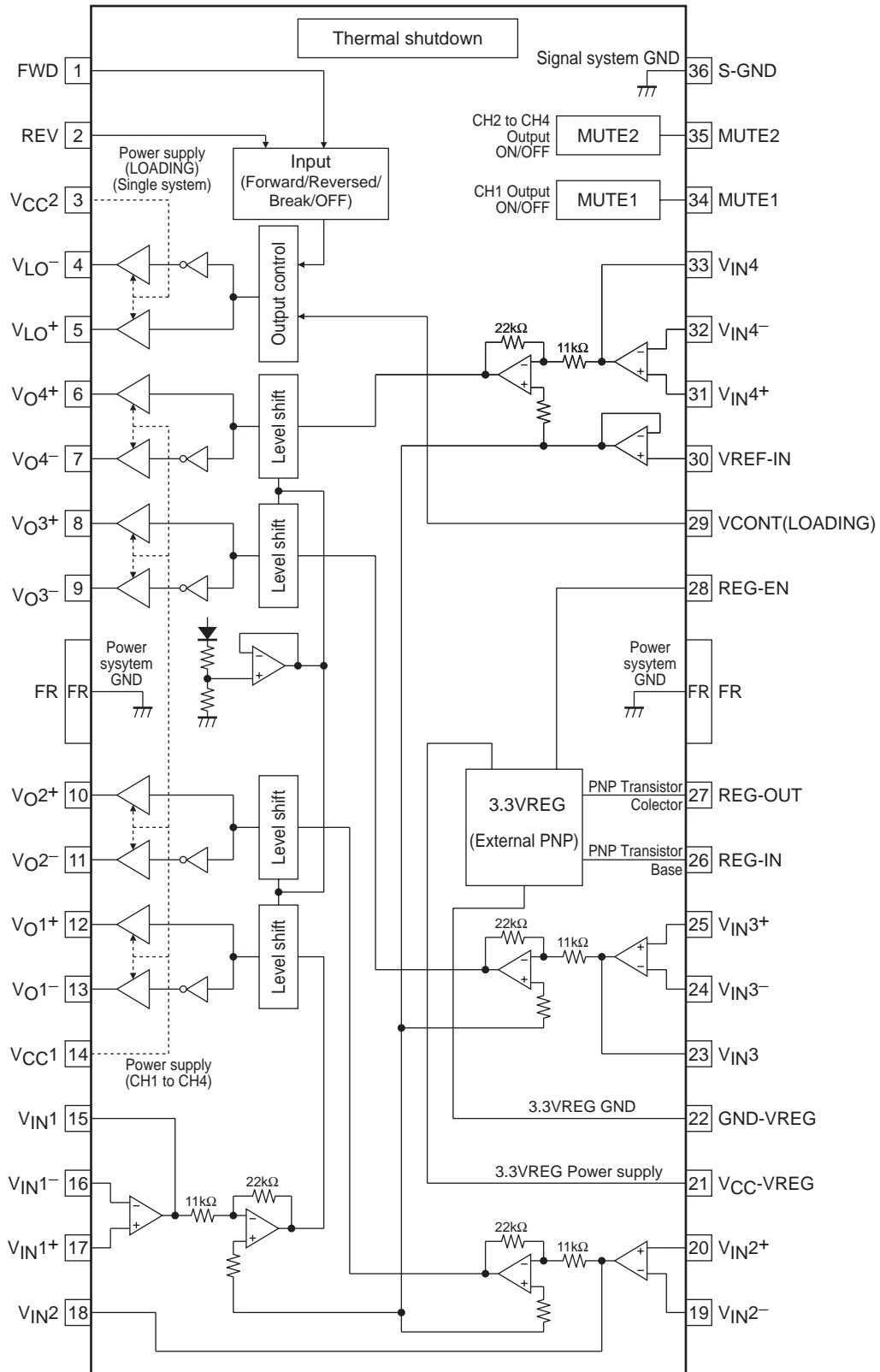


Pin Assignment



Top View

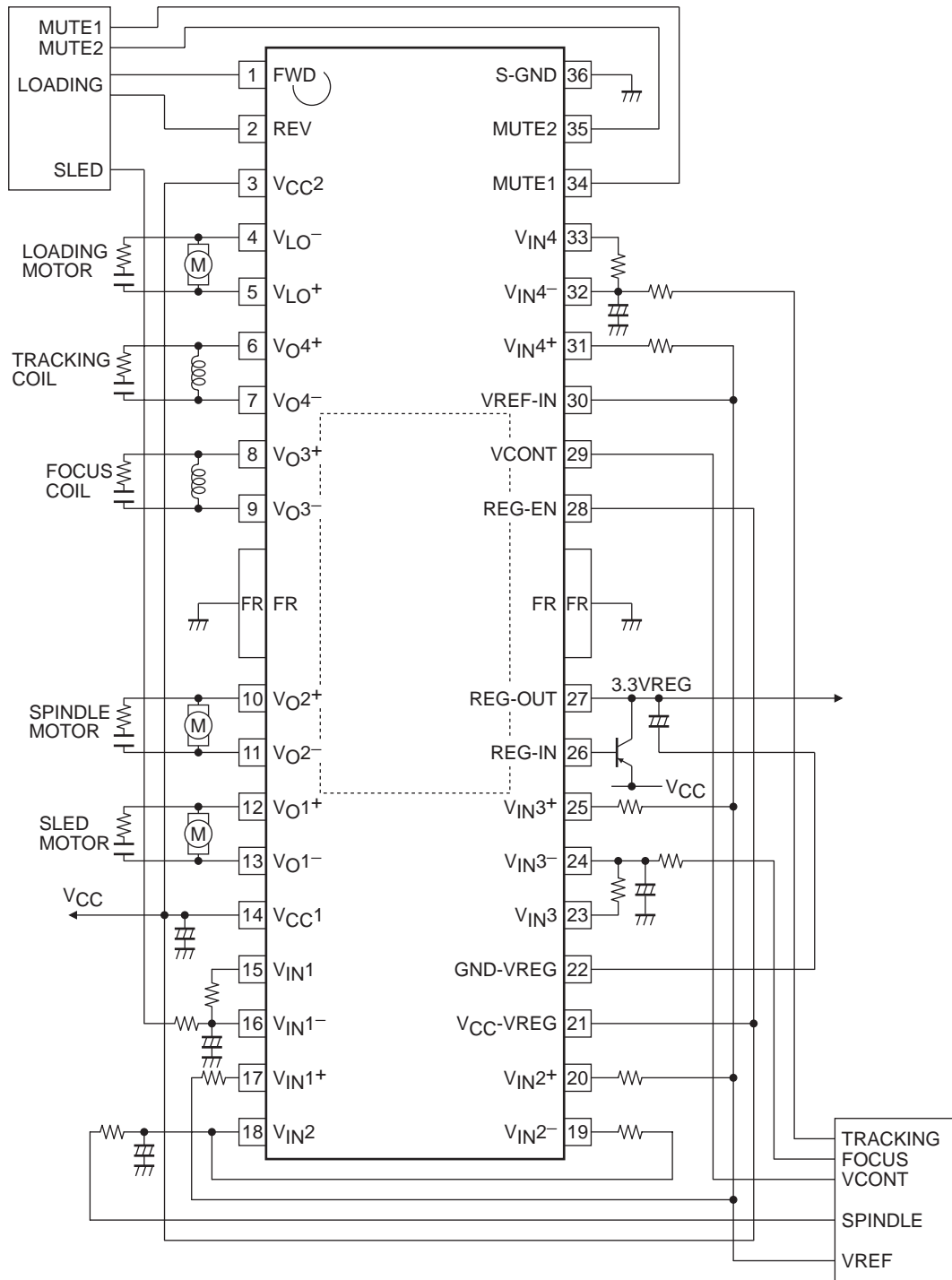
Block Diagram



Pin Description

Pin No.	Pin name	Function	Discription	Equivalent circuit
17 16 15 20 19 18 25 24 23 31 32 33	V_{IN1}^+ V_{IN1}^- V_{IN1} V_{IN2}^+ V_{IN2}^- V_{IN2} V_{IN3}^+ V_{IN3}^- V_{IN3} V_{IN4}^+ V_{IN4}^- V_{IN4}	Input (CH1 to 4)	Input pin (CH1 to 4).	
1 2	FWD REV	Input (LOADING)	Logic input pin. By combining H and L of this pin, any one of four modes (forward/reversed/brake/idling) can be selected.	
12 13 10 11 8 9 6 7	V_{O1}^+ V_{O1}^- V_{O2}^+ V_{O2}^- V_{O3}^+ V_{O3}^- V_{O4}^+ V_{O4}^-	Output (CH1 to 4)	Output for channel 1 to 4.	
34 35	MUTE1 MUTE2	MUTE	BTL AMP output. Output ON/OFF for CH1 to CH4. MUTE: H output ON MUTE: L output OFF	
5 4	V_{LO}^+ V_{LO}^-	Output (LOADING)	Output voltage set pin for loading block.	

Application Circuit Example



Note : Add CR between outputs or to a circuit to GND when oscillation occurs in the output.
Apply 4.5V or more to the external PNP Transistor emitter pin.

Truth Table (loading (H bridge) section)

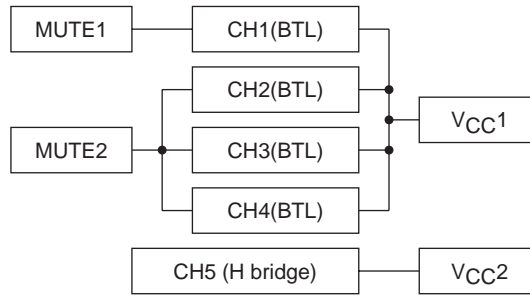
FWD	REV	Loading output
L	L	OFF *1
	H	Forward
H	L	Reversed
	H	(Short) brake *2

*1 The output has a high impedance.

*2 At brake, the SINK side transistor is ON (short brake).

V_{LO}^+ and V_{LO}^- are approximately on the GND level.

Relation of MUTE and Power (V_{CC}^*)



■ SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.

■ SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

■ In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.

■ Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of March, 2009 Specifications and information herein are subject to change without notice.