All Bond Pads ≥ 0.004" Sq.
Substrate is also Gate.

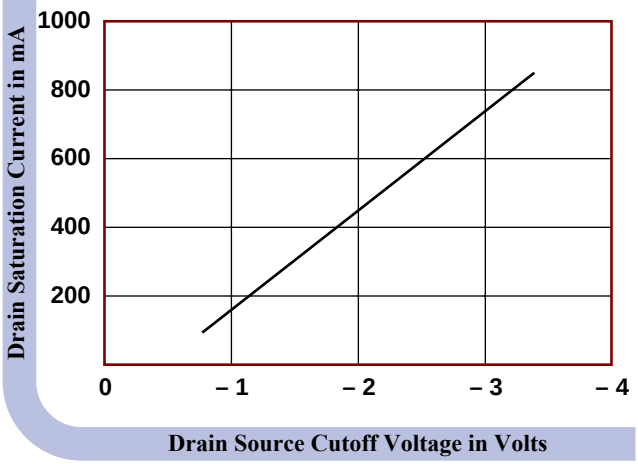
At 25°C free air temperature:		NJ1800DL Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 30	– 100	pA	V_{GS} = – 10V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	50		800	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.1		– 4	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance (Pulsed)	g_{fs}		350		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		160		pF	I_D = 1 mA, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		50		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		0.7		nV/√HZ	V_{DG} = 4V, I_D = 5 mA	f = 1 kHz

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375
www.interfet.co

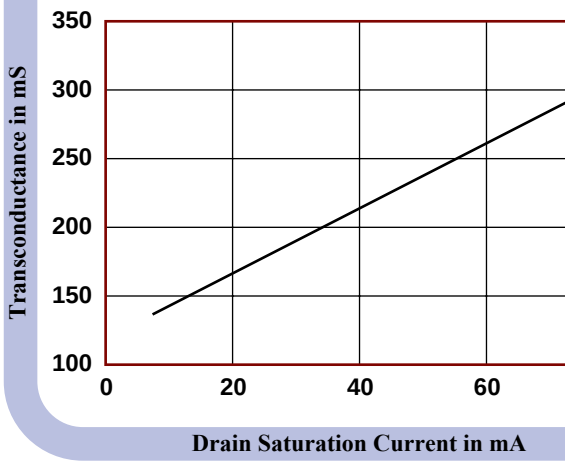
Drain to Source Voltage in Volts

Gate Source Cutoff Voltage in Volts

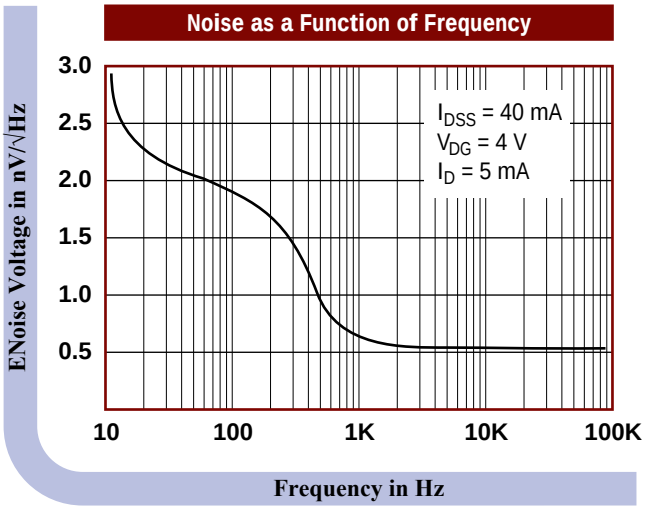
Drain Saturation Current as a Function of $V_{GS(OFF)}$



G_{fs} as a Function of I_{DSS}



Noise as a Function of Frequency



Input Capacitance as a Function of V_{GS}