

# MOS FIELD EFFECT TRANSISTOR NP100P04PLG

## SWITCHING P-CHANNEL POWER MOSFET

### DESCRIPTION

The NP100P04PLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

### <R> ORDERING INFORMATION

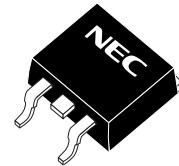
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP100P04PLG-E1-AY <sup>Note</sup>	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZP)
NP100P04PLG-E2-AY <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in external electrode.)

### FEATURES

- Super low on-state resistance  
 $R_{DS(on)1} = 3.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -50 \text{ A)}$   
 $R_{DS(on)2} = 5.1 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -50 \text{ A)}$
- High current rating:  $I_{D(DC)} = \mp 100 \text{ A}$
- Built-in gate protection diode

(TO-263)



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	-40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>c</sub> = 25°C)	I <sub>D(DC)</sub>	±100	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±300	A
Total Power Dissipation (T <sub>c</sub> = 25°C)	P <sub>T1</sub>	200	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Single Avalanche Current <sup>Note2</sup>	I <sub>AS</sub>	74	A
Single Avalanche Energy <sup>Note2</sup>	E <sub>AS</sub>	550	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = -20 → 0 V

### THERMAL RESISTANCE

Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	0.75	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	83.3	°C/W

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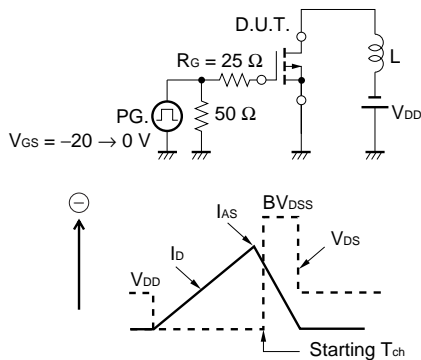
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

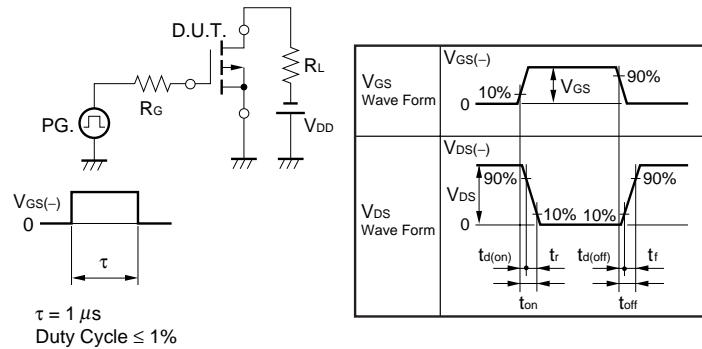
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -50 A	43	88		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A		2.8	3.7	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -50 A		3.4	5.1	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V,		15100		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		2400		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		1130		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -50 A,		38		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V,		30		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		300		ns
Fall Time	t <sub>f</sub>			100		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -32 V,		320		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V,		37		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -100 A		85		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = -100 A, V <sub>GS</sub> = 0 V		0.91	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -100 A, V <sub>GS</sub> = 0 V,		70		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100 A/μs		123		nC

**Note** Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

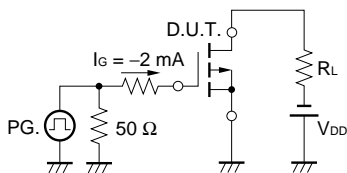
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



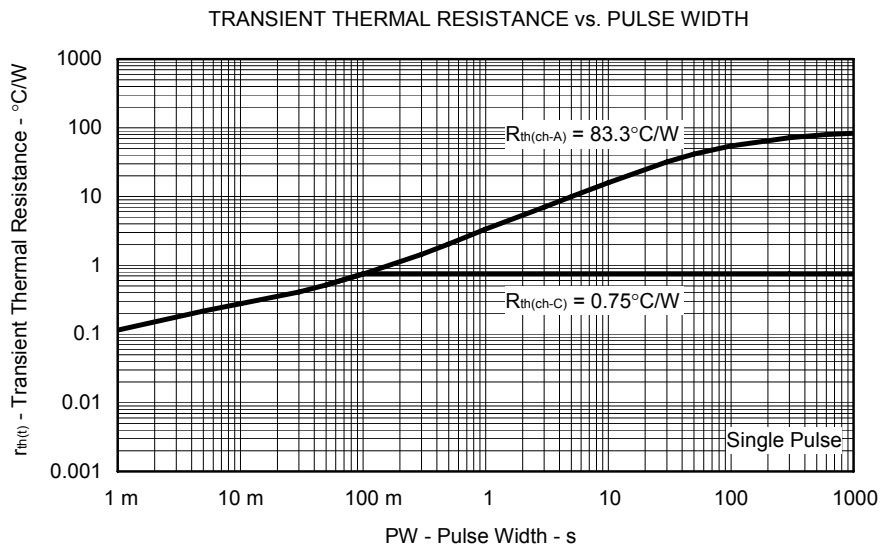
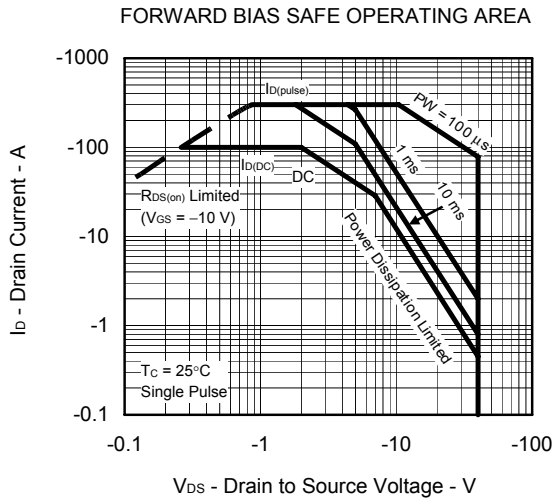
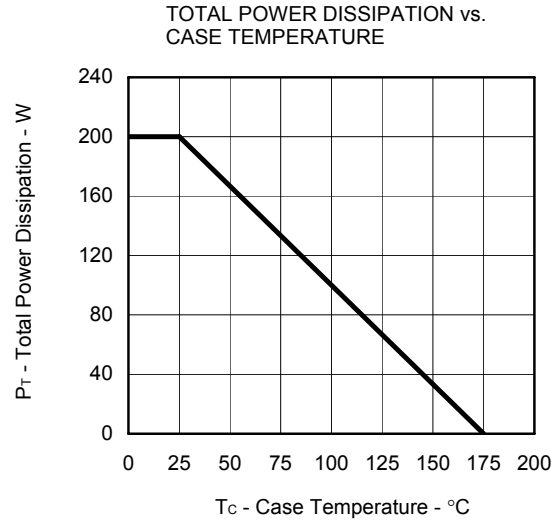
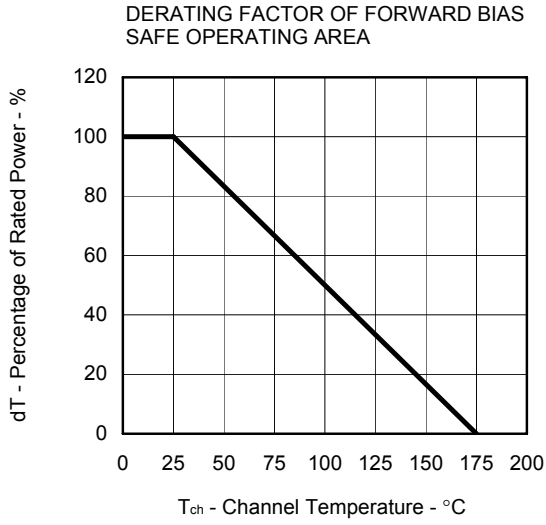
**TEST CIRCUIT 2 SWITCHING TIME**



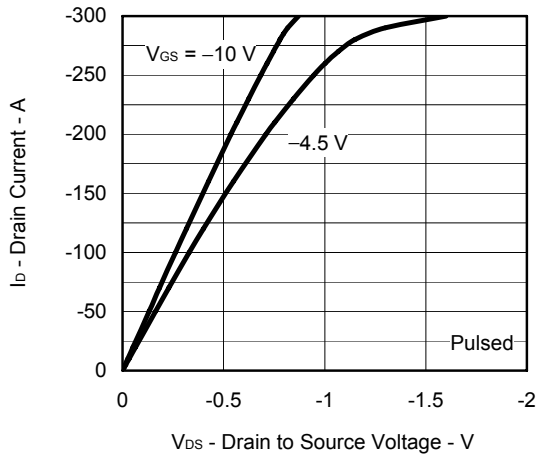
**TEST CIRCUIT 3 GATE CHARGE**



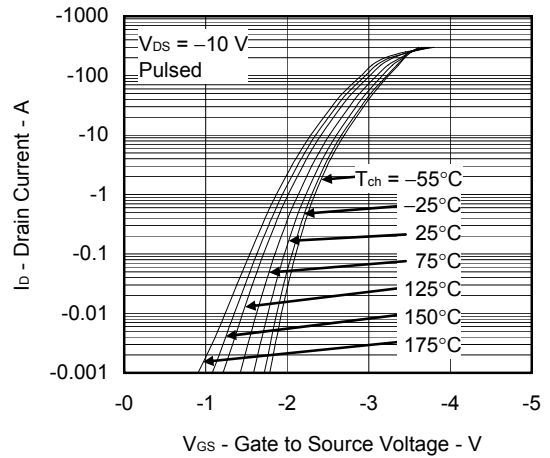
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



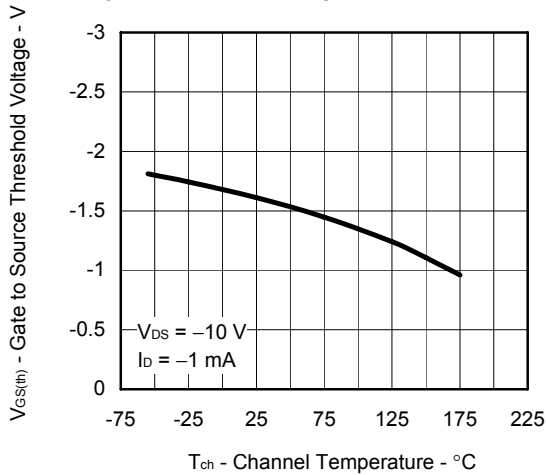
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



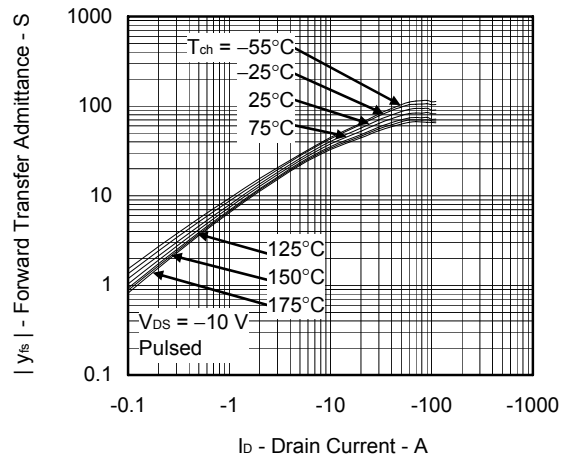
FORWARD TRANSFER CHARACTERISTICS



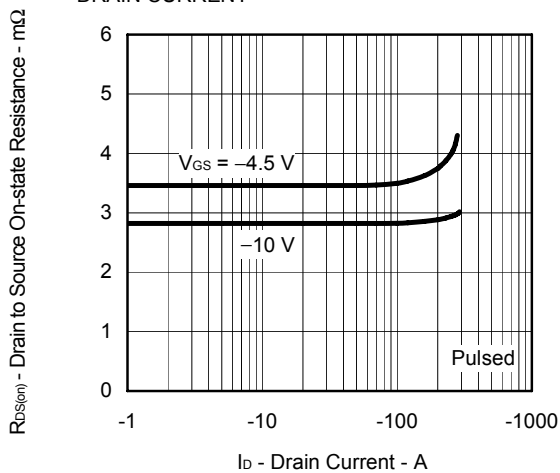
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



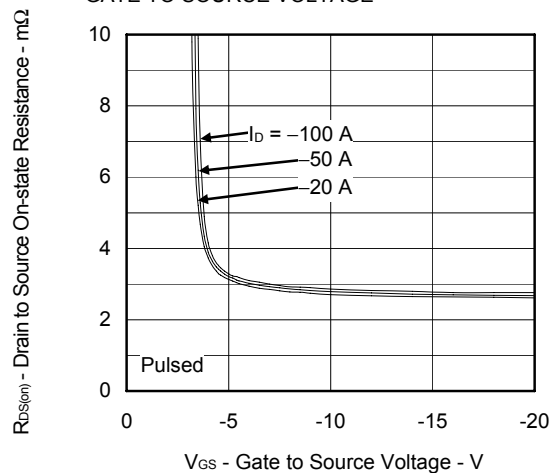
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



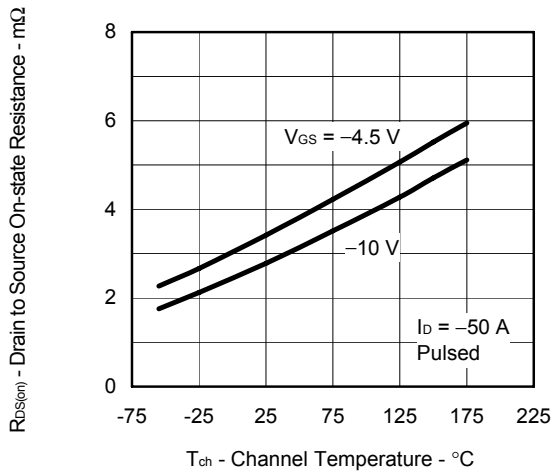
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



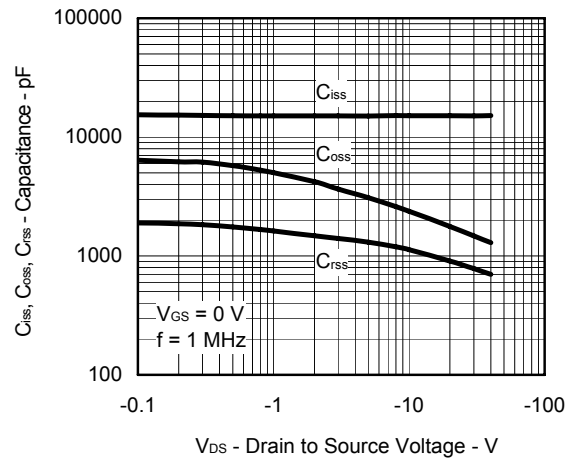
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



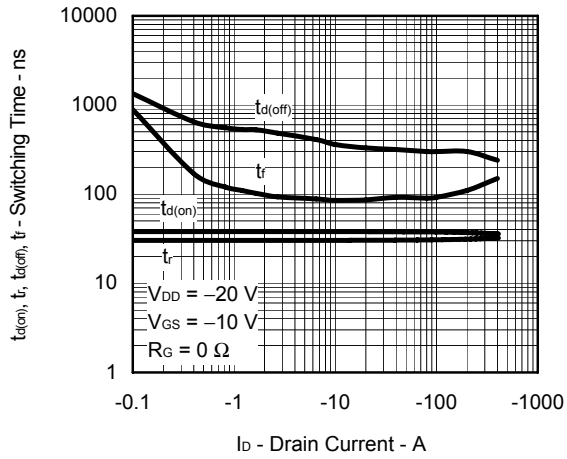
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



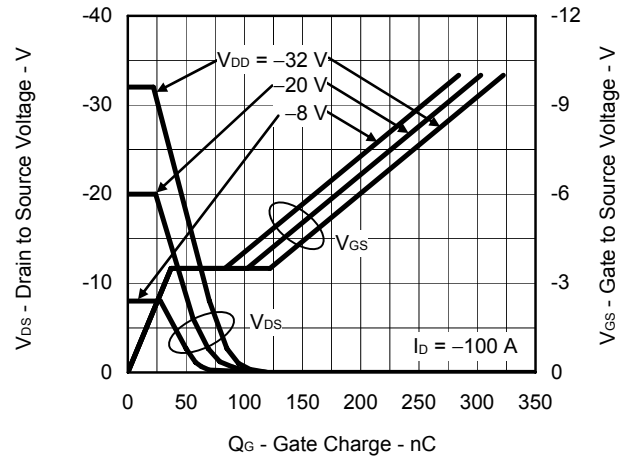
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



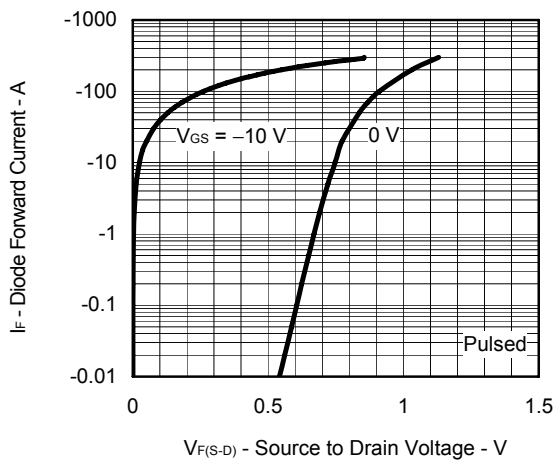
SWITCHING CHARACTERISTICS



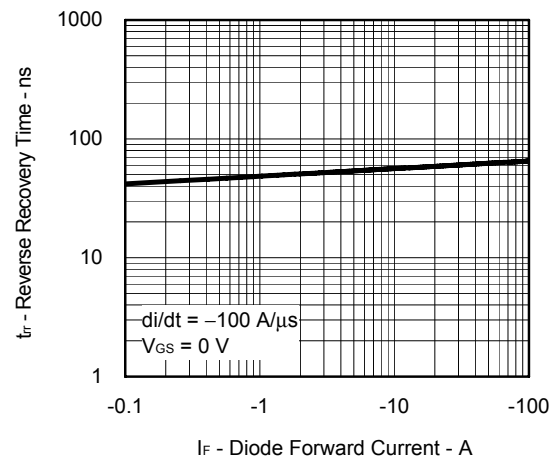
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

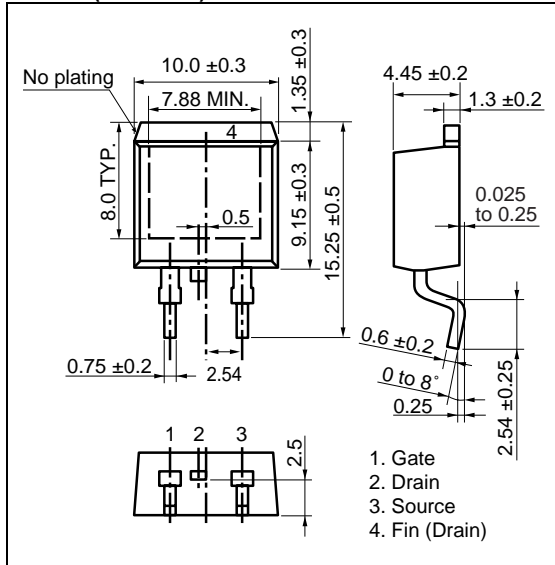


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

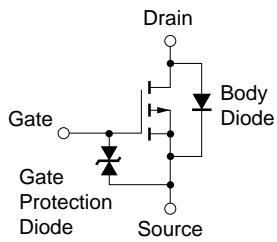


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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