



BUK9M120-100E

N-channel 100 V, 120 mΩ logic level MOSFET in LPAK33

19 September 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in an LPAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

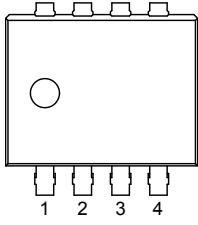
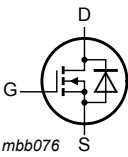
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	11.5	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	44	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	100	120	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	3.9	-	nC



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source	 LPAK33 (SOT1210)	 mbb076
2	S	Source		
3	S	Source		
4	G	Gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M120-100E	LPAK33	Plastic single ended surface mounted package (LPAK33); 8 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M120-100E	912010

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1][2]	-15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	44	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2		-	11.5	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	8.1	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	46	A

Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	11.5	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	46	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 11.5 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[3][4]	-	13.2	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm.
 [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
 [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
 [4] Refer to application note AN10273 for further information.

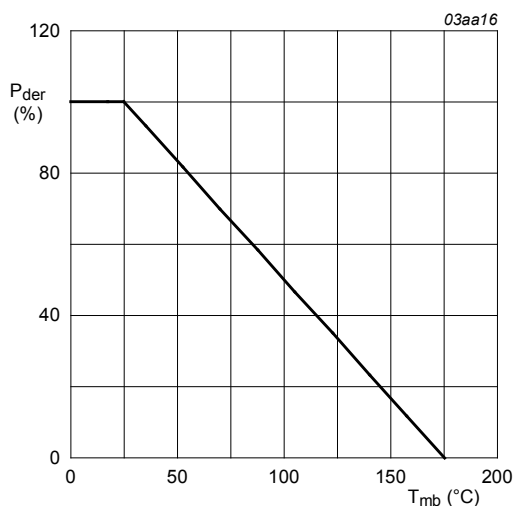
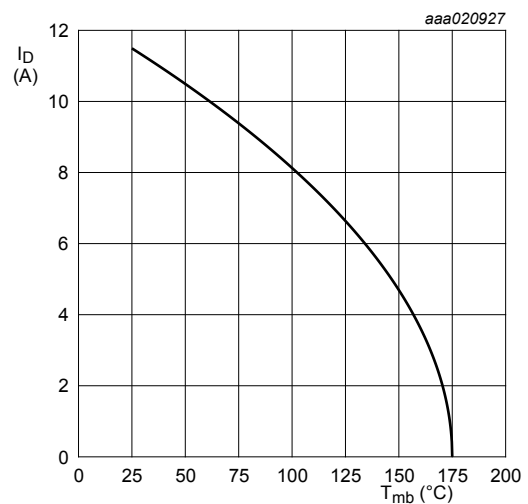


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

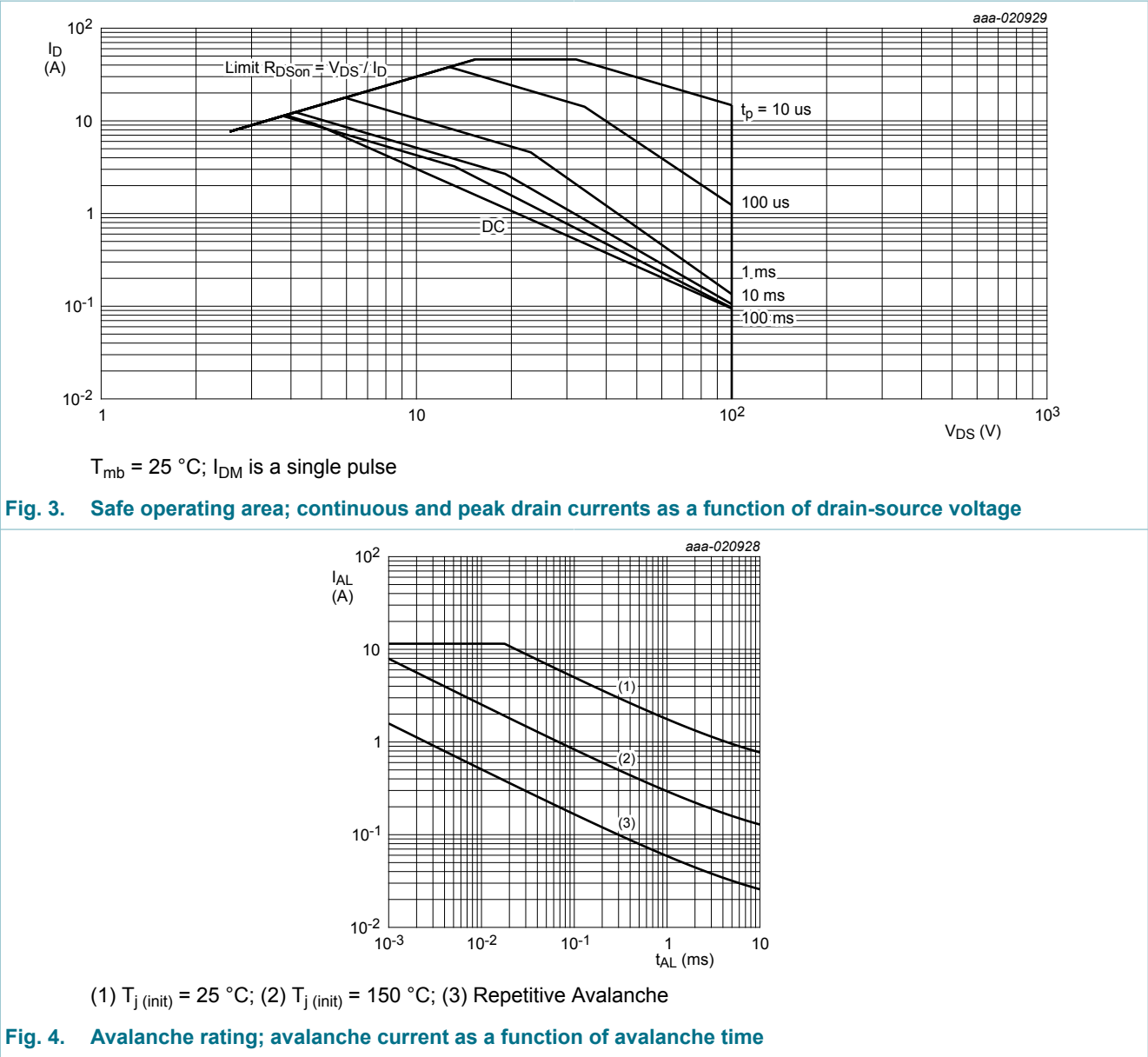
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$



$$V_{GS} \geq 5 \text{ V}$$

Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_D = 11.5 \text{ A} \times \sqrt{\frac{175^{\circ}\text{C} - T_{mb}}{150^{\circ}\text{C}}} \text{ for } T_{mb} \geq 25^{\circ}\text{C}$$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.77	3.4	K/W

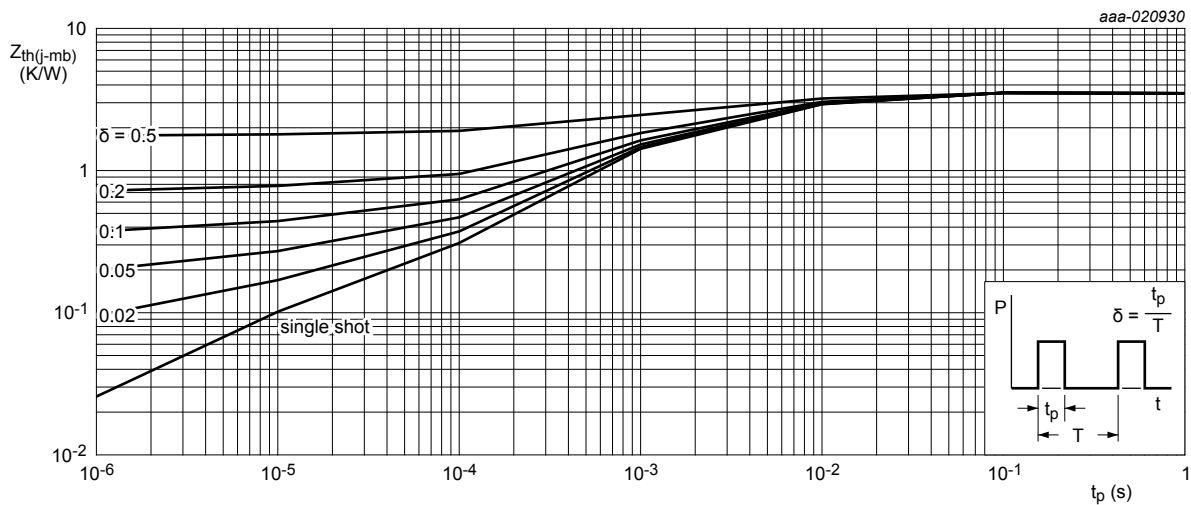


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		100	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ }^\circ\text{C}$		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10		1.4	1.7	2.05	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55\text{ }^\circ\text{C}$; Fig. 10		-	-	2.45	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 10		0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	0.01	1	μA
		$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11		-	100	120	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11		-	96	119	m Ω
		$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 12		-	-	340	m Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 5\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13 ; Fig. 14		-	8.8	-	nC
Q_{GS}	gate-source charge			-	1.7	-	nC
Q_{GD}	gate-drain charge			-	3.9	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	663	882	pF
C _{oss}	output capacitance			-	52	63	pF
C _{rss}	reverse transfer capacitance			-	35	48	pF
t _{d(on)}	turn-on delay time	V _{DS} = 80 V; R _L = 15 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6.1	-	ns
t _r	rise time			-	9.1	-	ns
t _{d(off)}	turn-off delay time			-	14.1	-	ns
t _f	fall time			-	8.3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.84	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C		-	27.4	-	ns
Q _r	recovered charge			-	35.5	-	nC

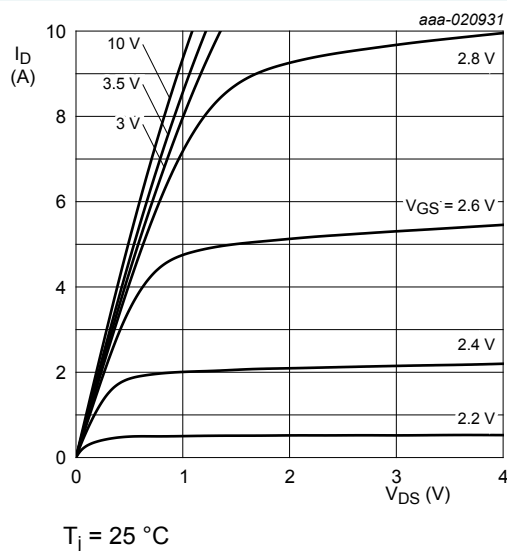


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

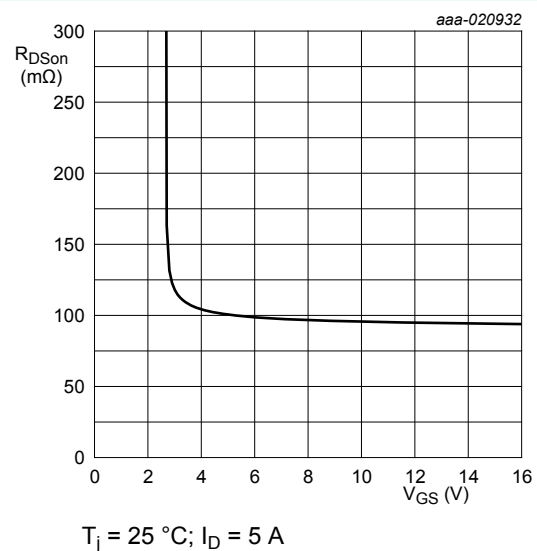


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

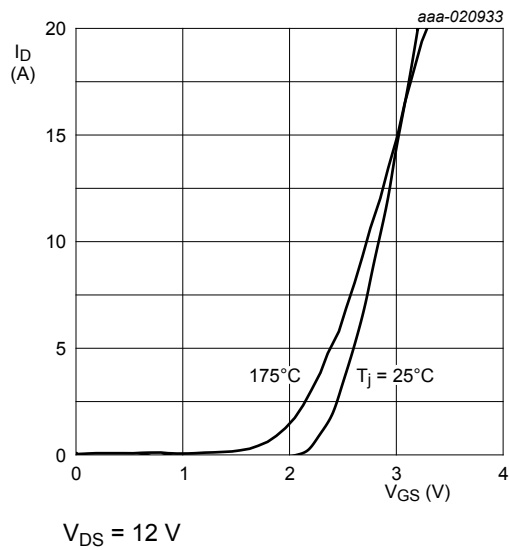


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

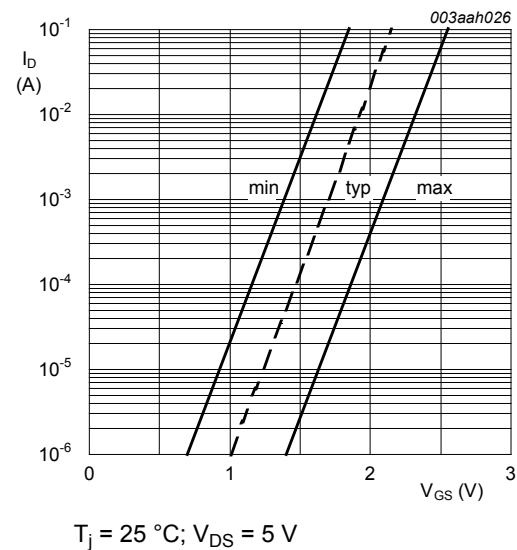


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

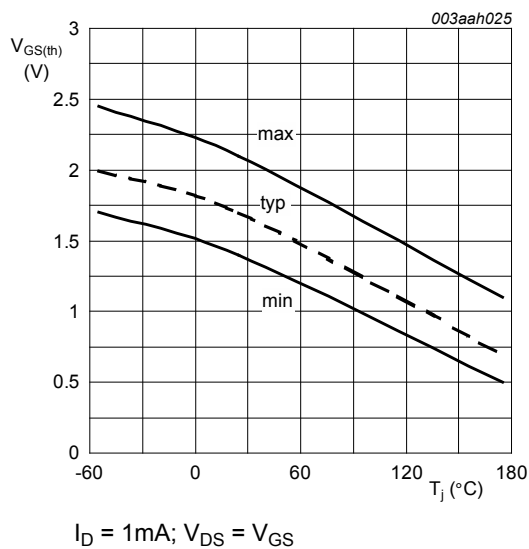


Fig. 10. Gate-source threshold voltage as a function of junction temperature

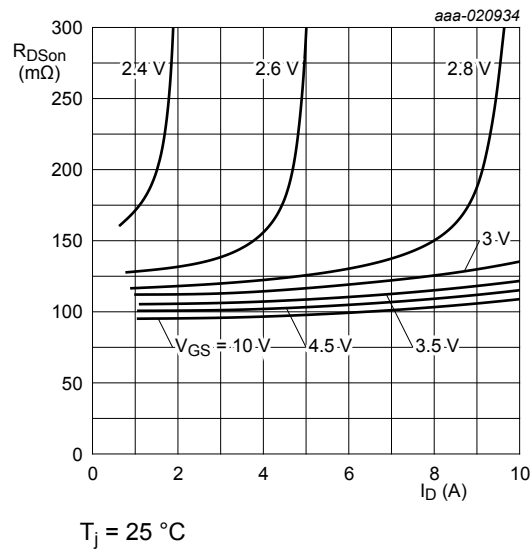


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

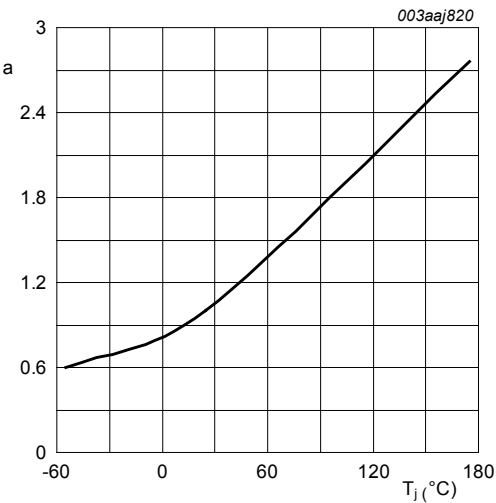
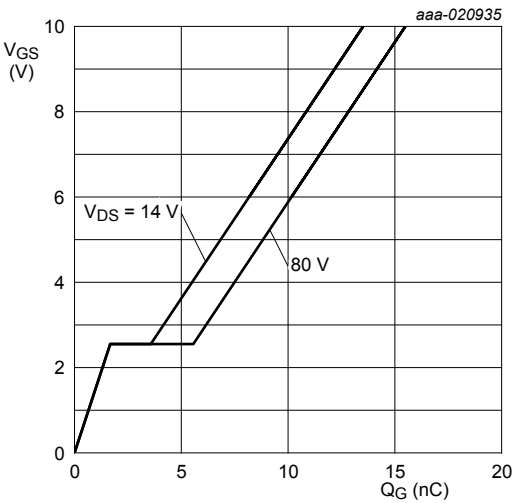


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$



$T_j = 25^{\circ}C$; $I_D = 5\text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

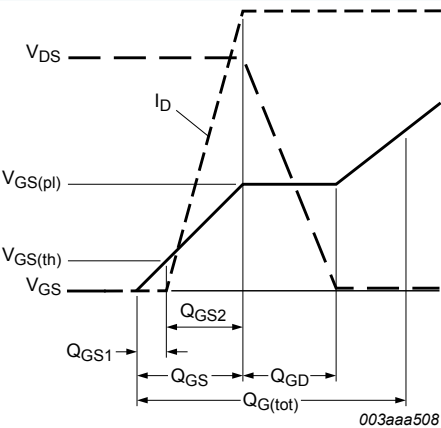
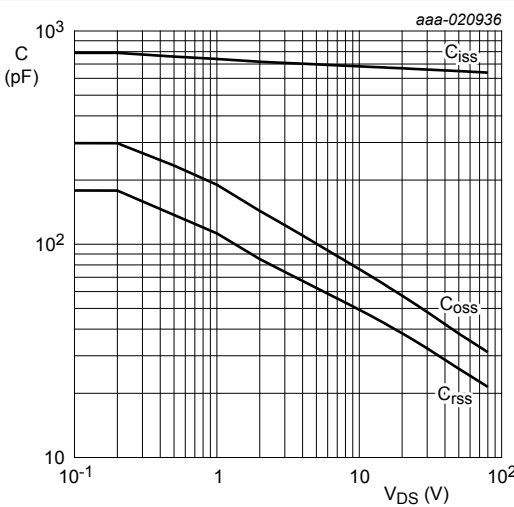
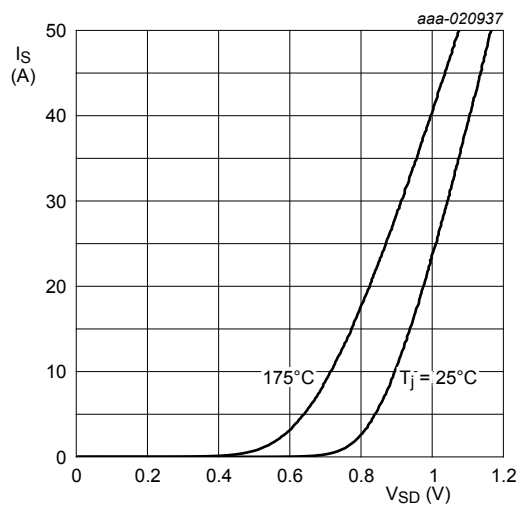


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Application information

For guidance on how to use and understand this datasheet, please refer to application note [AN11158](#) "Understanding power MOSFET datasheet parameters".

12. Package outline

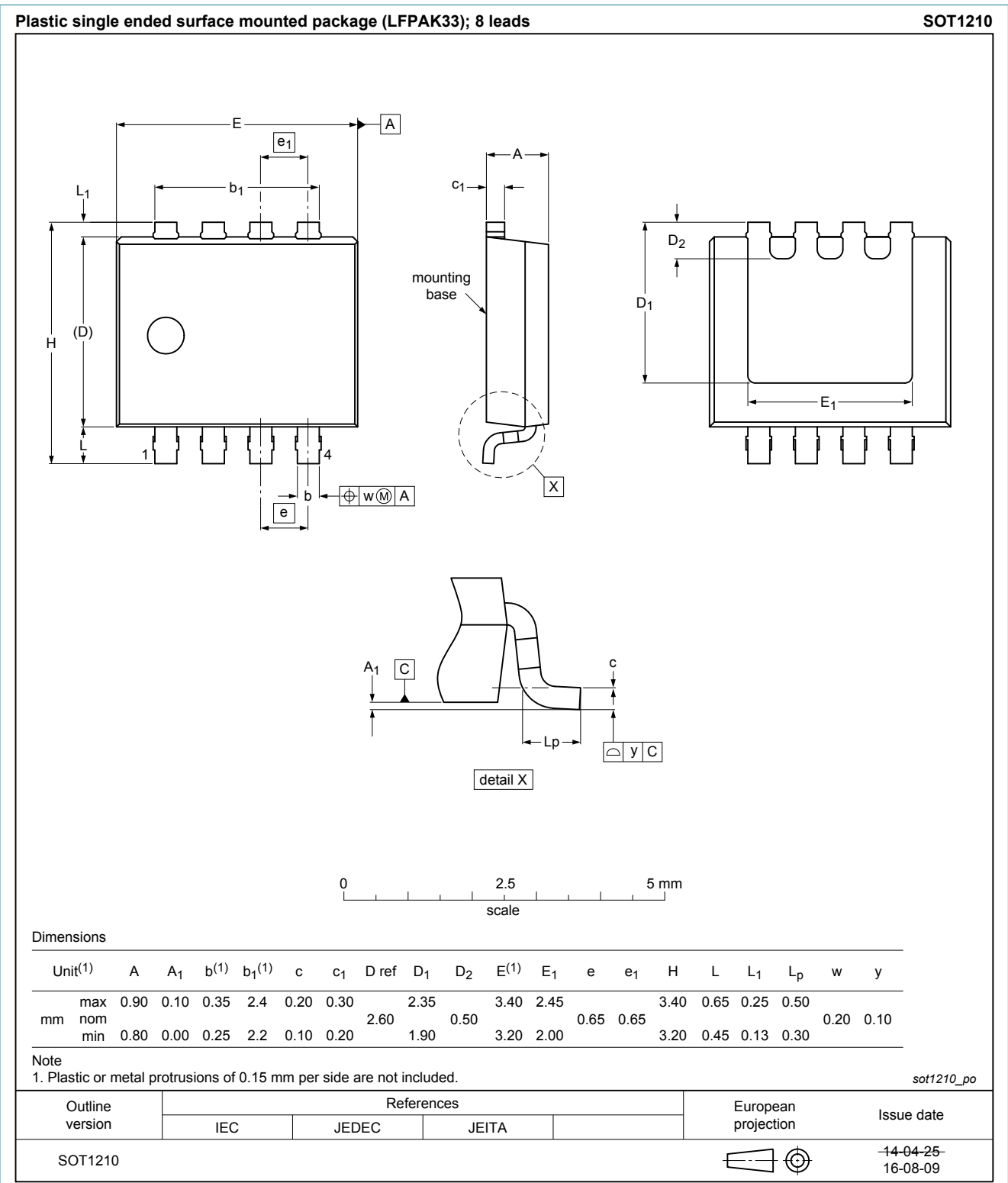


Fig. 17. Package outline LPAK33 (SOT1210)

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Document status [1][2]	Product status [3]	Definition
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